ALTERA

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About this Data Book

March 1995

This data book provides comprehensive information about Altera's FLEX 10K, FLEX 8000, MAX 9000, MAX 7000, FLASHlogic, MAX 5000, Classic, and Configuration EPROM device families, MAX+PLUS II development tools, and programming hardware devices.

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TEL : (408) 894-7104

FAX: (408) 944-0952

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Introduction

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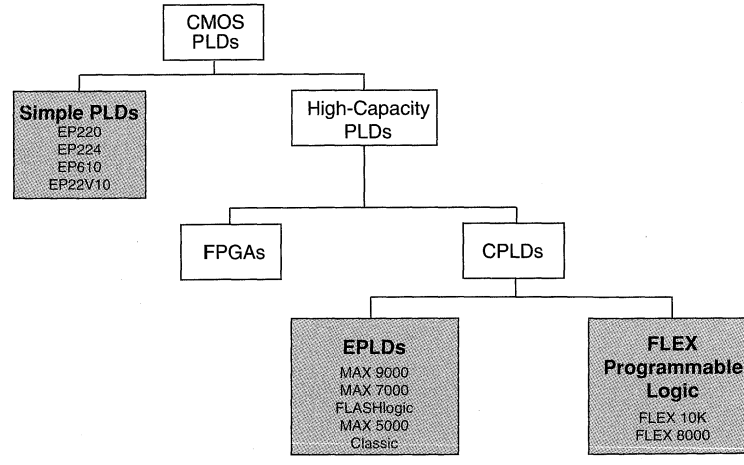
Programmable logic devices (PLDs) are digital, user-configurable integrated circuits (ICs) used to implement custom logic functions. PLDs can implement any Boolean expression or registered function with built-in logic structures. In contrast, off-the-shelf logic ICs, such as TTL devices, provide a specific logic function and cannot be modified to meet individual circuit design requirements. PLDs were once viewed as an alternative to discrete logic and custom or semi-custom devices such as ASICs. In recent years, however, PLDs have become the preferred choice. As PLD costs have decreased through high-volume manufacturing and the use of aggressive process technologies, PLD manufacturers have been able to offer devices with higher integration, higher performance, and lower cost per function than discrete devices.

The PLD Market

Programmable logic encompasses all digital logic circuits configured by the end user, including simple, low-density, 20-pin PAL/GAL devices, field-programmable gate arrays (FPGAs), and complex PLDs (CPLDs). PLDs are offered in different architectures, and a variety of memory elements are available for configuring the devices. Figure 1 shows the relative position of Altera general-purpose devices in the CMOS programmable logic device market.

Figure 1. Altera General-Purpose Logic Devices



CPLDs and FPGAs have different interconnect structures. The segmented interconnect structure of FPGAs uses varying lengths of metal lines connected by pass transistors or anti-fuses to connect logic cells. In contrast, the continuous interconnect structure of CPLDs uses continuous metal lines to provide logic cell-to-logic cell connectivity. The continuous interconnect structure eliminates the unpredictable timing associated with a segmented interconnect structure, and provides fast, fixed delay paths between logic cells. This structure makes it easier to implement a design, and thus shortens the development cycle.

Advantages of Altera PLDs

Designers generally develop a logic circuit with one of three distinctly different implementation options: discrete logic (TTL, CMOS, etc.), custom or semi-custom devices (ASICs), or PLDs. The best option is one that can meet the largest number of design requirements. Table 1 lists a number of important requirements and rates the three options according to their effectiveness in meeting these requirements.

Table 1. Device Options Rating

Requirement	PLD	Discrete Logic	ASIC
Speed	●	○	●
Density	●	○	●
Cost	◒	○	◒ *(1)*
Development time	●	◗	○
Prototyping & simulation time	◒	○	○
Manufacturing time	●	◗	○
Ease of use	●	◗	○
Future modification	●	◗	○
Inventory risk	●	●	○
Development tool support	●	○	●

Notes:
(1) Cost-effective only in high-volume production
● Very effective
◗ Adequate
○ Poor

Altera PLDs offer the general benefits of PLD technology, as well as other advantages based on innovative architectures, aggressive technologies, and the MAX+PLUS II programmable logic development environment, including:

- Higher performance
- High-density logic integration
- Greater cost-effectiveness
- Shorter development cycles with MAX+PLUS II software

Higher Performance

Performance is a function of process and architecture. Altera devices are manufactured on state-of-the-art CMOS processes, which offer the shortest possible delays. In addition, continuous interconnect structures provide fast, consistent signal delays throughout the device.

High-Density Logic Integration

Designers often seek the highest possible logic integration for their designs, usually to reduce board space and cost. Also, existing designs frequently undergo secondary development cycles that aim to reduce cost by integrating more logic into fewer devices. In both cases, PLDs with high logic integration capability offer an excellent solution. Altera devices—which range in density from 300 to 100,000 usable gates—can easily integrate existing logic, whether it be a small or a large number of discrete logic devices, PLDs, FPGAs, or even custom devices. This high integration capability provides higher performance and greater reliability, as well as lower system cost.

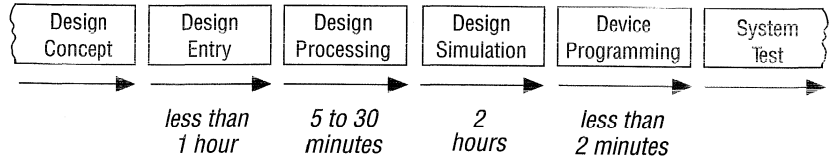
Greater Cost-Effectiveness

Altera continually strives to refine product development and manufacturing processes. The expertise accumulated over more than a decade of industry leadership has made both process technologies and the manufacturing flow highly efficient, and has enabled Altera to offer the most cost-effective, highest-performance programmable logic available.

Shorter Development Cycles with MAX+PLUS II Software

Time is the most precious resource for many design engineers. Large sums of money are lost on projects that are not completed on schedule and therefore miss a window of opportunity. Consequently, the shorter the development cycle, the better. Altera's fast, intuitive, and easy-to-use MAX+PLUS II software can shorten the development cycle considerably. Design entry, processing, verification, and device programming together take only a few hours, potentially allowing several complete design iterations in one day. Figure 2 illustrates a typical PLD development cycle in the MAX+PLUS II development environment. Times shown are representative of a relatively sophisticated 10,000-gate logic design.

Figure 2. Altera General-Purpose Logic Devices



Altera Device Families

Altera offers seven families of general-purpose PLDs: FLEX 10K, FLEX 8000, MAX 9000, MAX 7000, FLASHlogic, MAX 5000, and Classic. See Table 2. The FLEX architecture uses look-up tables (LUTs) to implement logic functions, whereas the Multiple Array MatriX (MAX), FLASHlogic, and Classic architectures use a programmable-AND/fixed-OR product-term architecture. Each family offers unique features, as well as distinct speed and utilization advantages for implementing a particular application.

Table 2. Altera Device Architecture

Device Family	Logic Cell Structure	Interconnect Structure	Reconfigurable Element
FLEX 10K	Look-up table	Continuous	SRAM
FLEX 8000	Look-up table	Continuous	SRAM
MAX 9000	Sum of products	Continuous	EEPROM
MAX 7000	Sum of products	Continuous	EEPROM
FLASHlogic	Sum of products	Continuous	SRAM/FLASH SRAM/EPROM
MAX 5000	Sum of products	Continuous	EPROM
Classic	Sum of products	Continuous	EPROM

Figure 3 compares the pin count and density of each device family.

Figure 3. Pin Count & Density in Altera Device Families

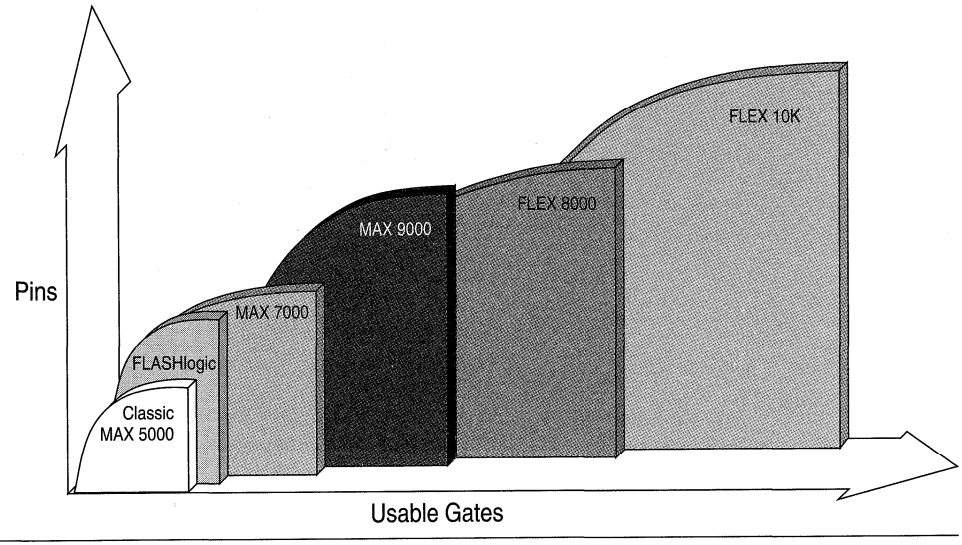
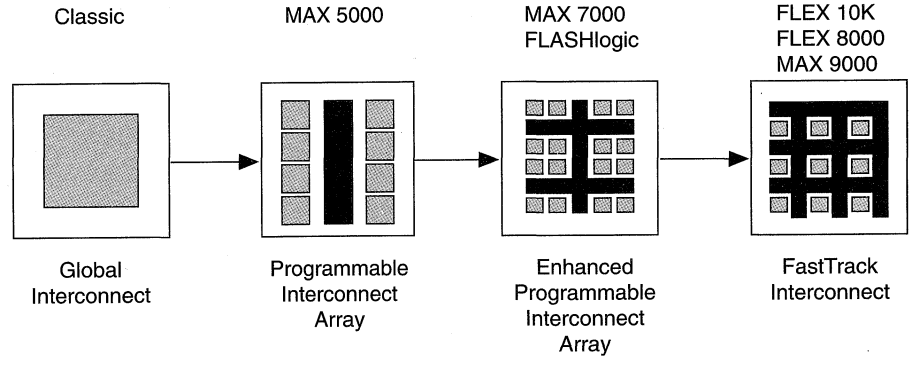


Figure 4 summarizes the architectures of Altera devices and illustrates how the interconnect structure has evolved to maintain high performance even at the highest densities.

Figure 4. Altera Architecture Evolution



All Altera device families use CMOS process technology, which provides lower power dissipation and greater reliability than bipolar technology. As part of Altera's commitment to continual improvement, Altera transfers products to advanced processes as soon as these technologies become viable and can support reliable manufacturing. This transfer generally reduces manufacturing costs and enhances performance, producing faster, more cost-effective devices. The following descriptions summarize the key features and benefits of Altera's general-purpose programmable logic device families.

FLEX 10K Family

To address the increasing levels of integration that logic systems demand, programmable logic architectures must not only increase in density, but also efficiently implement a large variety of logic circuits. The FLEX 10K family features the industry's largest programmable logic device (up to 100,000 gates). Many architectural features—including embedded array, multiple low-skew Clocks, and internal tri-state buses—provide the performance, utilization, and system-level integration required for complex logic designs. These innovations make FLEX 10K devices ideal for applications that have traditionally been reserved for gate arrays.

FLEX 8000 Family

The FLEX 8000 family is ideal for applications that require a large number of registers and I/O pins. Devices in the family range in density from 2,500 to 50,000 usable gates, with 282 to 4,752 registers and 78 to 360 user I/O pins. These features, along with the high-performance, predictable interconnect structure make FLEX 8000 devices as easy to use as product-term-based devices. In addition, the SRAM-based FLEX 8000 devices provide low standby power and are in-circuit reconfigurable, making them ideal for such applications as PC add-on cards, battery-powered instruments, and multi-purpose telecommunication cards.

MAX 9000 Family

The EEPROM-based MAX 9000 family combines the efficient macrocell of the MAX 7000 architecture with the high-performance, predictable FastTrack Interconnect of the FLEX 8000 architecture, resulting in a device family that is ideal for integrating multiple system-level functions. The MAX 9000 family ranges from 6,000 to 12,000 usable gates, 320 to 560 macrocells, and up to 216 user I/O pins. This level of density, combined with JTAG boundary-scan testing (BST) support and in-system programmability (ISP), make the MAX 9000 family an ideal choice for gate-array designs that can use the benefits of PLDs, as well as designs that can benefit from the flexibility of ISP.

MAX 7000 Family

The EEPROM-based MAX 7000 family is the fastest high-density programmable logic family in the industry. It ranges in density from 600 to 5,000 usable gates, with 32 to 256 macrocells, and 36 to 164 user I/O pins. These devices offer combinatorial propagation delays as fast as 5.0 ns and 16-bit counter frequencies of 178 MHz. Moreover, they provide very fast input register setup times, multiple system Clocks, and a programmable speed/power control. The slew rate for I/O pins can be controlled, providing an extra level of switching noise control. MAX 7000S devices also provide ISP and JTAG BST support.

FLASHlogic Family

The FLASHlogic family features architectural innovations that are ideal for implementing logic designs that require internal RAM, in-circuit reconfigurability (ICR), ISP, or JTAG BST support. The FLASHlogic family is primarily SRAM-based, but also has built-in, nonvolatile FLASH cells (EPROM cells for EPX780 and EPX740 devices), eliminating the need for an external PROM. The family ranges in density from 40 to 160 macrocells, and 30 to 120 user I/O pins. These features, combined with fast combinatorial delays as fast as 10 ns, make the FLASHlogic family ideal for microprocessor-based systems and for bus interface applications.

MAX 5000 Family

The MAX 5000 family provides a comprehensive, cost-effective solution for designs that require a high level of combinatorial logic. MAX 5000 devices provide logic densities ranging from 300 to 3,800 usable gates, and pin counts ranging from 20 to 100 pins. Because of the maturity of the devices and Altera's commitment to migrating existing families to newer, more aggressive technologies, MAX 5000 devices offer excellent cost-per-macrocell values that compare favorably to ASICs and gate arrays for high-volume production. EPROM-based MAX 5000 devices are nonvolatile and erasable.

Classic Family

The EPROM-based Classic family is Altera's original family of devices. It features densities of up to 900 usable gates and pin counts of up to 68 pins. Composed of single arrays of globally interconnected logic, the industry-standard Classic family offers a low-cost solution for low-density applications. The Classic family offers a unique "zero-power" mode, allowing the devices to draw only microamps of current at standby, which makes them ideal for low-power applications.

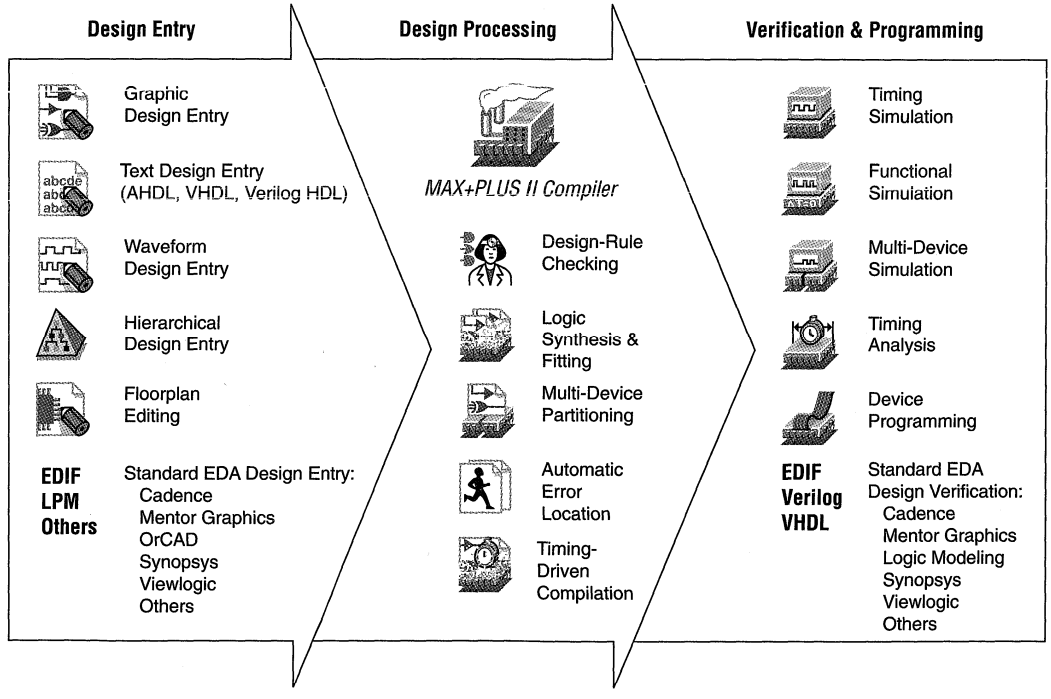
Solutions for High-Volume Production

For applications that are targeted for high-volume production, Altera offers Mask-Programmed Logic Devices (MPLDs) as low-cost alternatives to high-density PLDs. MPLDs, which are masked versions of programmable logic devices, offer a unique turn-key approach that eliminates the engineering-intensive tasks required for custom and semi-custom devices. The quick turnaround for MPLD conversion guarantees fast time-to-market.

MAX+PLUS II Development Tools

Altera achieves maximum device performance and density not only with advanced processes and innovative logic architectures, but also through state-of-the-art design tools. The MAX+PLUS II programmable logic development software provides an architecture-independent design environment that supports designs for Altera's general-purpose PLD families, ensuring easy design entry, quick processing, and uncomplicated device programming. See Figure 5.

Figure 5. MAX+PLUS II Design Environment



With MAX+PLUS II, designers no longer need to master the complexities of device architectures. MAX+PLUS II translates their design—created with familiar design entry tools such as schematic capture tools or high-level behavioral languages—into the format required by the target architecture.

Intimate architectural knowledge is built into Altera development tools, eliminating the need for designers to manually optimize their design; designs can therefore be completed much more rapidly. With MAX+PLUS II, users can take a logic circuit from design entry to device programming in a matter of hours. Design processing is typically completed in minutes, allowing several complete design iterations in a single day.

Design Entry, Processing, Verification & Device Programming

MAX+PLUS II offers a full spectrum of logic design capabilities. Designers are free to combine text, graphic, and waveform design entry methods while creating hierarchical single- or multi-device designs. The MAX+PLUS II Compiler performs minimization and logic synthesis, fits the design into one or more devices, and generates programming data. Design verification with functional and timing simulation and delay prediction for speed-critical paths are available, as well as multi-device simulation across multiple device families. Altera and a number of programming hardware manufacturers offer hardware for programming the devices.

Access to Various Platforms & Other EDA Tools

Altera is committed to supporting the logic development environments that are most familiar to circuit designers. MAX+PLUS II provides interfaces to a wide variety of other EDA tools—from companies such as Cadence, Mentor Graphics, OrCAD, Synopsys, and Viewlogic—via EDIF, LPM, Verilog HDL, and VHDL. The MAX+PLUS II Compiler runs on PC and various workstation platforms, making MAX+PLUS II the industry's only platform-independent, architecture-independent programmable logic design environment. The ACCESS alliance, which Altera has formed with industry-leading EDA tool vendors, ensures smooth interfaces between Altera products and the products of the ACCESS partners, as well as timely support of Altera devices with these tools.

Conclusion

The advanced architectures and processing technologies used in Altera devices provide the greatest performance, highest density, and greatest flexibility available in the PLD market. Regardless of an application's requirements, Altera devices provide an efficient solution with high levels of integration, high I/O capabilities, and the fastest speeds available.

The sophisticated, highly integrated MAX+PLUS II development environment completes Altera's total solution. MAX+PLUS II gives designers the ability to take full advantage of all features offered in Altera devices. MAX+PLUS II can target a project to any device family, thus offering designers architecture-independent design capabilities, regardless of their preferred design flow. Together, Altera devices and Altera development tools are the logical choice for all designs that require fast development cycles and cost-effective components.

Component Selection Guide

March 1995, ver. 2 Data Sheet

Introduction

This selection guide lists devices available from Altera:

- FLEX 10K devices
- FLEX 8000 devices
- Configuration EPROM devices
- MAX 9000 devices
- MAX 7000 devices
- MAX 7000S devices
- FLASHlogic devices
- MAX 5000 devices
- Classic devices
- System-level features
- 3.3-V devices
- Devices with 3.3-V/5.0-V I/O pins
- PCI-compliant devices
- Military-compliant devices

For detailed information on these products, refer to the appropriate sections in this data book. For a list of Altera products, refer to the *Product Index*. For information on Altera's programmable logic development systems, see the *MAX+PLUS II Selection Guide*.

The information in this selection guide is accurate as of the printing date. For the latest component information, contact your local sales representative.

FLEX 10K Devices

The FLEX 10K family is the programmable logic industry's first embedded-array programmable logic device (PLD) family, offering up to 100,000 gates in a single programmable device. The revolutionary FLEX 10K architecture offers system-level integration and megafunction support, making these devices ideal for gate array prototyping. For more information on FLEX 10K devices, refer to the *FLEX 10K Embedded-Array Programmable Logic Device Family Advance Information Brief* in this data book, or contact Altera Marketing at (408) 894-7104. See Table 1.

Table 1. FLEX 10K Devices *Note (1)*

Device	Typical Gates	Usable Gates	Configuration Element	Logic Elements (Flipflops)	Total RAM Bits	Maximum User I/O Pins
EPF10K10	10,000	7,000 to 31,000	SRAM	576 (720)	6,144	150
EPF10K20	20,000	15,000 to 63,000	SRAM	1,152 (1,344)	12,288	198
EPF10K30	30,000	22,000 to 69,000	SRAM	1,728 (1,968)	12,288	246
EPF10K40	40,000	29,000 to 93,000	SRAM	2,304 (2,576)	16,384	278
EPF10K50	50,000	36,000 to 116,000	SRAM	2,880 (3,184)	20,480	310
EPF10K70	70,000	46,000 to 118,000	SRAM	3,744 (4,096)	18,432	358
EPF10K100	100,000	62,000 to 158,000	SRAM	4,992 (5,392)	24,576	406

Note:
(1) Preliminary information is shown for some devices.

FLEX 8000 Devices

Table 2 provides information on the FLEX 8000 family of register-intensive, high-density PLDs. Low-cost FLEX 8000 devices are the ideal replacement for gate arrays with fewer than 20,000 gates. FLEX 8000 devices combine the fine-grained architecture and high register count of FPGAs with the high speed, predictable interconnect delays, and ease-of-use of EPLDs. FLEX 8000 devices are fabricated on an advanced 0.6-micron, triple-layer-metal CMOS technology with SRAM configuration elements.

Table 2. FLEX 8000 Devices *Note (1)*

Device	Package *(2)*	Temp. *(3)*	Speed Grade	Configuration Element	Logic Cells (Flipflops)	Ded. Inputs	I/O Pins	Number of Pins
EPF8282A	L, T	C	-2	SRAM	208 (282)	4	64, 74	84, 100
EPF8282A	L, T	C	-3	SRAM	208 (282)	4	64, 74	84, 100
EPF8282A	L, T	C, I	-4	SRAM	208 (282)	4	64, 74	84, 100
EPF8282AV,	L, T	C	-3	SRAM	208 (282)	4	64, 74	84, 100
Note (4)	L, T	C	-4	SRAM	208 (282)	4	64, 74	84, 100
	L, T	C, I	-5	SRAM	208 (282)	4	64, 74	84, 100
EPF8282V,	L, T	C	-3	SRAM	208 (282)	4	64, 74	84, 100
Note (4)	L, T	C, I	-4	SRAM	208 (282)	4	64, 74	84, 100
EPF8452A	L, G, Q, T	C	-2	SRAM	336 (452)	4	64, 116	84, 100, 160
EPF8452A	L, G, Q, T	C	-3	SRAM	336 (452)	4	64, 116	84, 100, 160
EPF8452A	L, G, Q, T	C, I	-4	SRAM	336 (452)	4	64, 116	84, 100, 160
EPF8452A	L, G, Q, T	C	-5	SRAM	336 (452)	4	64, 116	84, 100, 160
EPF8452A	L, G, Q, T	C	-6	SRAM	336 (452)	4	64, 116	84, 100, 160
EPF8636A	L, G, Q, R	C	-2	SRAM	504 (636)	4	64, 114, 132	84, 160, 192, 208
EPF8636A	L, G, Q, R	C	-3	SRAM	504 (636)	4	64, 114, 132	84, 160, 192, 208
EPF8636A	L, G, Q, R	C, I	-4	SRAM	504 (636)	4	64, 114, 132	84, 160, 192, 208
EPF8820A	G, R	C	-2	SRAM	672 (820)	4	116, 148	160, 192, 208
EPF8820A	G, R	C	-3	SRAM	672 (820)	4	116, 148	160, 192, 208
EPF8820A	G, R	C, I, M	-4	SRAM	672 (820)	4	116, 148	160, 192, 208
EPF81188A	G, R	C	-2	SRAM	1,008 (1,188)	4	144, 180	208, 232, 240
EPF81188A	G, R	C	-3	SRAM	1,008 (1,188)	4	144, 180	208, 232, 240
EPF81188A	G, R	C, I, M	-4	SRAM	1,008 (1,188)	4	144, 180	208, 232, 240
EPF81188A	G, R	C	-5	SRAM	1,008 (1,188)	4	144, 180	208, 232, 240
EPF81188A	G, R	C	-6	SRAM	1,008 (1,188)	4	144, 180	208, 232, 240
EPF81500A	G, R, B	C	-2	SRAM	1,296 (1,500)	4	177, 204	240, 280, 304
EPF81500A	G, R, B	C	-3	SRAM	1,296 (1,500)	4	177, 204	240, 280, 304
EPF81500A	G, R, B	C, I	-4	SRAM	1,296 (1,500)	4	177, 204	240, 280, 304
EPF8050M	G	C	-3	SRAM	4,032 (4,656)	0	360	560

Notes to table:

(1) Preliminary information is shown for some devices. Consult the *FLEX 8000 Programmable Logic Device Family Data Sheet* in this data book for more information or contact Altera for the most current device information.

(2) Package configurations (contact Altera for information on device package availability):
- B: Ball-grid array (BGA)
- G: Ceramic pin-grid array (PGA)
- L: Plastic J-lead chip carrier (PLCC)
- Q: Plastic quad flat pack (PQFP)
- R: Power quad flat pack (RQFP)
- T: Plastic thin quad flat pack (TQFP)

(3) Operating temperature:
- C: Commercial (0° C to 70° C)
- I: Industrial (–40° C to 85° C)
- M: Military (–55° C to 125° C)

(4) The EPF8282V is a 3.3-V version of the EPF8282.

Configuration EPROM Devices

Table 3 provides information on the Altera serial Configuration EPROMs that can be used to configure FLEX 8000 devices.

Table 3. Configuration EPROM for FLEX 8000 Devices *Note (1)*

Device	Package (2)	Temp. (3)	Configuration Element	Description	Number of Pins
EPC1064	P, L, T	C, I	EPROM	64K x 1-bit serial EPROM designed to configure FLEX 8000 devices.	8, 20, 32
EPC1064V	P, L, T	C, I	EPROM	64K x 1-bit serial EPROM designed to configure FLEX 8000 devices. The EPC1064V is a 3.3-V version of the EPC1064.	8, 20, 32
EPC1213	D, P, L	C, I, M	EPROM	213K x 1-bit serial EPROM designed to configure FLEX 8000 devices.	8, 20

Notes:

(1) Preliminary information is shown for some devices. Consult the *Configuration EPROM for FLEX 8000 Devices Data Sheet* in this data book for more information or contact Altera for the most current device information.

(2) Package configurations (contact Altera for information on device package availability):
- D: Ceramic dual in-line package (CerDIP)
- L: Plastic J-lead chip carrier (PLCC)
- P: Plastic dual in-line package (PDIP)
- T: Plastic thin quad flat pack (TQFP)

(3) Operating temperature:
- C: Commercial (0° C to 70° C)
- I: Industrial (–40° C to 85° C)
- M: Military (–55° C to 125° C)

MAX 9000 Devices

The MAX 9000 family of 5.0-V, high-density PLDs is based on Altera's third-generation MAX architecture. Fabricated on advanced 0.65-micron CMOS technology with EEPROM configuration elements, the MAX 9000 family provides 6,000 to 12,000 usable gates, 320 to 560 macrocells, in-system programmability (ISP), and JTAG boundary-scan testing (BST) circuitry. See Table 4.

Table 4. MAX 9000 Devices *Note (1)*

Device	Package (2)	Temp. (3)	Speed Grade	Configuration Element	Logic Cells (Flipflops)	Ded. Inputs	I/O Pins	Number of Pins
EPM9320	L, R, G	C	-12	EEPROM	320 (484)	4	56, 112, 128, 164	84, 160, 208, 280
EPM9320	L, R, G	C	-15	EEPROM	320 (484)	4	56, 112, 128, 164	84, 160, 208, 280
EPM9320	L, R, G	C, I	-20	EEPROM	320 (484)	4	56, 112, 128, 164	84, 160, 208, 280
EPM9400	L, R, G	C	-12	EEPROM	400 (580)	4	55, 135, 155, 180	84, 208, 240, 280
EPM9400	L, R, G	C	-15	EEPROM	400 (580)	4	55, 135, 155, 180	84, 208, 240, 280
EPM9400	L, R, G	C, I	-20	EEPROM	400 (580)	4	55, 135, 155, 180	84, 208, 240, 280
EPM9480	R, G	C	-12	EEPROM	480 (616)	4	113, 142, 171, 196	160, 208, 240, 280
EPM9480	R, G	C	-15	EEPROM	480 (616)	4	113, 142, 171, 196	160, 208, 240, 280
EPM9480	R, G	C, I	-20	EEPROM	480 (616)	4	113, 142, 171, 196	160, 208, 240, 280
EPM9560	W, R, G	C	-12	EEPROM	560 (772)	4	149, 187, 212	208, 240, 280, 304
EPM9560	W, R, G	C	-15	EEPROM	560 (772)	4	149, 187, 212	208, 240, 280, 304
EPM9560	W, R, G	C, I	-20	EEPROM	560 (772)	4	149, 187, 212	208, 240, 280, 304

Notes:

(1) Preliminary information is shown for some devices. Consult the *MAX 9000 Programmable Logic Device Family Data Sheet* in this data book for more information or contact Altera for the most current device information.

(2) Package configurations (contact Altera for information on device package availability):
- G: Ceramic pin-grid array (PGA)
- L: Plastic J-lead chip carrier (PLCC)
- R: Power quad flat pack (RQFP)
- W: Ceramic quad flat pack (CQFP)

(3) Operating temperature:
- C: Commercial (0° C to 70° C)
- I: Industrial (–40° C to 85° C)

MAX 7000 Devices

Table 5 provides information on the MAX 7000 family of high-density, high-speed, I/O-intensive PLDs. These devices range from fast 5-ns PAL/GAL integrators to high-speed, programmable gate array alternatives. MAX 7000 devices are fabricated on CMOS technology with EEPROM configuration elements.

Table 5. MAX 7000 Devices (Part 1 of 2) *Note (1)*

Device	Package (2)	Temp. (3)	Speed Grade	t_{PD1} (ns)	f_{CNT} (MHz)	Configuration Element	Logic Cells (Flipflops)	Ded. Inputs	I/O Pins	Number of Pins
EPM7032	L, Q, T	C	-5	5	178	EEPROM	32	4	32	44
EPM7032	L, Q, T	C	-6	6	150	EEPROM	32	4	32	44
EPM7032	L, Q, T	C	-7	7.5	125	EEPROM	32	4	32	44
EPM7032	L, Q, T	C	-10	10	100	EEPROM	32	4	32	44
EPM7032	L, Q, T	C, I	-12	12	90.9	EEPROM	32	4	32	44
EPM7032	L, Q, T	C, I	-15	15	76.9	EEPROM	32	4	32	44
EPM7032	L	C	-15T	15	76.9	EEPROM	32	4	32	44
EPM7032V	L, T, *(4)*	C	-12	12	90.9	EEPROM	32	4	32	44
EPM7032V	L, T, *(4)*	C	-15	15	76.9	EEPROM	32	4	32	44
EPM7032V	L, T, *(4)*	C, I	-20	20	66.6	EEPROM	32	4	32	44
EPM7064	L, Q, T	C	-6	6	150	EEPROM	64	4	32	44
EPM7064	L, Q, T	C	-7	7.5	125	EEPROM	64	4	32, 48, 64	44, 68, 84, 100
EPM7064	L, Q, T	C	-10	10	100	EEPROM	64	4	32, 48, 64	44, 68, 84, 100
EPM7064	L, Q, T	C	-12	12	90.9	EEPROM	64	4	32, 48, 64	44, 68, 84, 100
EPM7064	L, Q, T	C, I	-15	15	76.9	EEPROM	64	4	32, 48, 64	44, 68, 84, 100
EPM7096	L, Q	C	-7	7.5	125	EEPROM	96	4	48, 60, 72	68, 84, 100
EPM7096	L, Q	C	-10	10	100	EEPROM	96	4	48, 60, 72	68, 84, 100
EPM7096	L, Q	C	-12	12	90.9	EEPROM	96	4	48, 60, 72	68, 84, 100
EPM7096	L, Q	C, I	-15	15	76.9	EEPROM	96	4	48, 60, 72	68, 84, 100
EPM7128E	L, Q	C	-7	7.5	125	EEPROM	128	4	64, 80, 96	84, 100, 160
EPM7128E	Q	C	-10P	10	100	EEPROM	128	4	64, 80, 96	100, 160
EPM7128E	L, Q	C	-10	10	100	EEPROM	128	4	64, 80, 96	84, 100, 160
EPM7128E	L, Q	C	-12	12	90.9	EEPROM	128	4	64, 80, 96	84, 100, 160
EPM7128E	L, Q	C, I	-15	15	76.9	EEPROM	128	4	64, 80, 96	84, 100, 160
EPM7128E	L, Q	C, I	-20	20	62.5	EEPROM	128	4	64, 80, 96	84, 100, 160
EPM7160E	L, Q	C	-7	7.5	125	EEPROM	160	4	60, 80, 100	84, 100, 160
EPM7160E	Q	C	-10P	10	100	EEPROM	160	4	60, 80, 100	100, 160
EPM7160E	L, Q	C	-10	10	100	EEPROM	160	4	60, 80, 100	84, 100, 160
EPM7160E	L, Q	C	-12	12	90.9	EEPROM	160	4	60, 80, 100	84, 100, 160
EPM7160E	L, Q	C	-15	15	76.9	EEPROM	160	4	60, 80, 100	84, 100, 160
EPM7160E	L, Q	C, I	-20	20	62.5	EEPROM	160	4	60, 80, 100	84, 100, 160
EPM7192E	G, Q	C	-10	10	100	EEPROM	192	4	120	160
EPM7192E	Q	C	-12P	12	90.9	EEPROM	192	4	120	160
EPM7192E	G, Q	C	-12	12	90.9	EEPROM	192	4	120	160
EPM7192E	G, Q	C, I, M	-15	15	76.9	EEPROM	192	4	120	160
EPM7192E	G, Q	C, I, M	-20	20	62.5	EEPROM	192	4	120	160

Table 5. MAX 7000 Devices (Part 2 of 2) *Note (1)*

Device	Package (2)	Temp. (3)	Speed Grade	t_{PD1} (ns)	f_{CNT} (MHz)	Configuration Element	Logic Cells (Flipflops)	Ded. Inputs	I/O Pins	Number of Pins
EPM7256E	G, R, Q	C	-10	10	100	EEPROM	256	4	128, 160	160, 192, 208
EPM7256E	R, Q	C	-12P	12	90.9	EEPROM	256	4	128, 160	160, 192, 208
EPM7256E	G, R, Q	C	-12	12	90.9	EEPROM	256	4	128, 160	160, 192, 208
EPM7256E	G, R, Q, W	C, M	-15	15	76.9	EEPROM	256	4	128, 160	160, 192, 208
EPM7256E	G, R, Q, W	C, I, M	-20	20	62.5	EEPROM	256	4	128, 160	160, 192, 208

Notes:

(1) Preliminary information is shown for some devices. Consult the *MAX 7000 Programmable Logic Device Family Data Sheet* in this data book for more information or contact Altera for the most current device information.

(2) Package configurations (contact Altera for information on device package availability):
- G: Ceramic pin-grid array (PGA)
- L: Plastic J-lead chip carrier (PLCC)
- Q: Plastic quad flat pack (PQFP)
- R: Power quad flat pack (RQFP)
- T: Plastic thin quad flat pack (TQFP)
- W: Ceramic quad flat pack (CQFP)

(3) Operating temperature:
- C: Commercial (0° C to 70° C)
- I: Industrial (–40° C to 85° C)
- M: Military (–55° C to 125° C)

(4) The EPM7032V is a 3.3-V version of the EPM7032.

MAX 7000S Devices

The MAX 7000S devices provide a superset of the features of MAX 7000 devices (including MAX 7000E devices), offering in-system programmability (ISP), JTAG BST circuitry, and open-collector outputs. For more information on MAX 7000S devices, refer to the *MAX 7000S Programmable Logic Device Family Advance Information Brief* in this data book or contact Altera Marketing at (408) 894-7104.

FLASHlogic Devices

Table 6 provides information on the FLASHlogic family of medium-density, high-speed, feature-rich PLDs. These innovative devices are based on CMOS technology with SRAM configuration elements shadowed by EPROM or FLASH configuration elements. FLASHlogic devices feature in-circuit reconfigurability (ICR), in-system programmability (ISP), and on-board RAM.

Table 6. FLASHlogic Devices *Note (1)*

Device	Package (2)	Temp. (3)	t_{PD1} (ns)	f_{CNT} (MHz)	Configuration Element	Logic Cells (Flipflops)	Max. On-Board RAM (Bits)	Ded. Inputs	I/O Pins	Number of Pins
EPX740	L	C	10	83.3	SRAM, EPROM	40	5,120	0, 10	30, 40	44, 68
EPX740	L	C	15	50	SRAM, EPROM	40	5,120	0, 10	30, 40	44, 68
EPX740	L	C, I	12	66	SRAM, EPROM	40	5,120	0, 10	30, 40	44, 68
EPX780	L, Q	C	10	83.3	SRAM, EPROM	80	10,240	0, 22	60, 80	84, 132
EPX780	L, Q	C	12	66	SRAM, EPROM	80	10,240	0, 22	60, 80	84, 132
EPX780	L, Q	C, I	15	50	SRAM, EPROM	80	10,240	0, 22	60, 80	84, 132
EPX880	L, Q	C	10	80	SRAM, FLASH	80	10,240	0, 22	60, 104	84, 160
EPX880	L, Q	C	12	64.5	SRAM, FLASH	80	10,240	0, 22	60, 104	84, 160
EPX8160	Q	C	10	80	SRAM, FLASH	160	20,480	48	172	208
EPX8160	Q	C	12	64.5	SRAM, FLASH	160	20,480	48	172	208

Notes:

(1) Preliminary information is shown for some devices. Consult the *FLASHlogic Programmable Logic Device Family Data Sheet* in this data book for more information or contact Altera for the most current device information.

(2) Package configurations (contact Altera for information on device package availability):
- L: Plastic J-lead chip carrier (PLCC)
- Q: Plastic quad flat pack (PQFP)

(3) Operating temperature:
- C: Commercial (0° C to 70° C)
- I: Industrial (–40° C to 85° C)

MAX 5000 Devices

Table 7 provides information on the MAX 5000 family of low-cost PLDs, which are suitable for implementing functions ranging from 20-pin address decoders to 100-pin custom LSI peripherals. These devices combine the speed, ease-of-use, and familiarity of PAL devices with the density of programmable gate arrays. MAX 5000 devices are fabricated on CMOS technology with EPROM configuration elements.

Table 7. MAX 5000 Devices *Note (1)*

Device	Package (2)	Temp. (3)	Speed Grade	t_{PD1} (ns)	f_{CNT} (MHz)	Configuration Element	Logic Cells (Flipflops)	Ded. Inputs	I/O Pins	Number of Pins
EPM5032	D, P, J, L, S	C	-15	15	76.9	EPROM	32	8	16	28
EPM5032	D, P, J, L, S	C	-17	17	71.4	EPROM	32	8	16	28
EPM5032	D, P, J, L, S	C, I	-20	20	62.5	EPROM	32	8	16	28
EPM5032	D, P, J, L, S	C, I, M	-25	25	50.0	EPROM	32	8	16	28
EPM5064	J, L	C	-1	25	50.0	EPROM	64	8	28	44
EPM5064	J, L	C	-2	30	40.0	EPROM	64	8	28	44
EPM5064	J, L	C, I, M	(4)	35	33.3	EPROM	64	8	28	44
EPM5128A	J, L, G	C	-15	15	83.3	EPROM	128	8	52	68
EPM5128A	J, L, G	C, M	-20	20	66.7	EPROM	128	8	52	68
EPM5128	J, L, G	C	-1	25	50.0	EPROM	128	8	52	68
EPM5128	J, L, G	C, I, M	-2	30	40.0	EPROM	128	8	52	68
EPM5128	J, L, G	C, I, M	(4)	35	33.3	EPROM	128	8	52	68
EPM5130	J, L, G, Q, W	C	-1	25	50.0	EPROM	130	20	48, 64	84, 100
EPM5130	J, L, G, Q, W	C, I, M	-2	30	40.0	EPROM	130	20	48, 64	84, 100
EPM5130	J, L, G, Q, W	C, I, M	(4)	35	33.3	EPROM	130	20	48, 64	84, 100
EPM5192	J, L, G	C	-1	25	50.0	EPROM	192	8	64	84
EPM5192	J, L, G	C	-2	30	40.0	EPROM	192	8	64	84
EPM5192	J, L, G	C, I, M	(4)	35	33.3	EPROM	192	8	64	84

Notes:

(1) Preliminary information is shown for some devices. Consult the *MAX 5000 Programmable Logic Device Family Data Sheet* in this data book for more information or contact Altera for the most current device information.

(2) Package configurations (contact Altera for information on device package availability):
- D: Ceramic dual in-line package (CerDIP)
- G: Ceramic pin-grid array (PGA)
- J: Ceramic J-lead chip carrier (JLCC)
- L: Plastic J-lead chip carrier (PLCC)
- P: Plastic dual in-line package (PDIP)
- Q: Plastic quad flat pack (PQFP)
- S: Plastic small-outline integrated circuit (SOIC)
- W: Ceramic quad flat pack (CQFP)

(3) Operating temperature:
- C: Commercial (0° C to 70° C)
- I: Industrial (–40° C to 85° C)
- M: Military (–55° C to 125° C)

(4) This device does not have a speed grade suffix.

Classic Devices

Table 8 provides information on the industry-standard Classic family of PLDs, which offer the most comprehensive solution to high-speed, low-power logic integration. These devices provide t_{PD} as low as 7.5 ns and internal counter rates as high as 125 MHz. Classic devices are fabricated on CMOS technology with EPROM configuration elements.

Table 8. Classic Devices *Note (1)*

Device	Package (2)	Temp. (3)	Speed Grade	t_{PD1} (ns)	f_{CNT} (MHz)	Memory Element	Logic Cells (Flipflops)	Ded. Inputs	I/O Pins	Number of Pins
EP220, *(4)*	L	C	-7A	7.5	115	EPROM	8	10	8	20
EP220	D, P, L	C	-10A	10	100	EPROM	8	10	8	20
EP224, *(4)*	L	C	-7A	7.5	115	EPROM	8	10	8	24, 28
EP224	P, L	C	-10A	10	100	EPROM	8	10	8	24, 28
EP22V10	P, L	C	-7	7.5	111.1	EPROM	10	12	10	24, 28
EP22V10	P, L	C	-10	10	100	EPROM	10	12	10	24, 28
EP22V10	P, L	C, I	-15	15	83.3	EPROM	10	12	10	24, 28
EP22V10E	P, L	C	-10	10	100	EPROM	10	12	10	24, 28
EP22V10E	P, L	C	-15	15	83.3	EPROM	10	12	10	24, 28
EP610	P, L, S	C	-15	15	83.3	EPROM	16	4	16	24, 28
EP610	P, L, S	C, I	-20	20	62.5	EPROM	16	4	16	24, 28
EP610I	D, P, L	C	-10	10	100	EPROM	16	4	16	24, 28
EP610I	D, P, L	C, I	-15	15	66	EPROM	16	4	16	24, 28
EP910	D, P, J, L	C	-30	30	33.3	EPROM	24	12	24	40, 44
EP910I	L	C, I	-12	12	77	EPROM	24	12	24	40, 44
EP910I	D, P, L	C, I	-15	15	67	EPROM	24	12	24	40, 44
EP910I	D, P, L	C, I	-25	25	40	EPROM	24	12	24	40, 44
EP1810	L	C	-20	20	50.0	EPROM	48	16	48	68
EP1810	L	C, I	-25	25	40.0	EPROM	48	16	48	68
EP1810	J, L, G	C	-35	35	28.6	EPROM	48	16	48	68
EP1810	J, L, G	C, I, M	-45	45	22.2	EPROM	48	16	48	68

Notes:

(1) Preliminary information is shown for some devices. Consult the *Classic Programmable Logic Device Family Data Sheet* in this data book for more information or contact Altera for the most current device information.

(2) Package configurations (contact Altera for information on device package availability):
- D: Ceramic dual in-line package (CerDIP)
- G: Ceramic pin-grid array (PGA)
- J: Ceramic J-lead chip carrier (JLCC)
- L: Plastic J-lead chip carrier (PLCC)
- P: Plastic dual in-line package (PDIP)
- S: Plastic small-outline integrated circuit (SOIC)

(3) Operating temperature:
- C: Commercial (0° C to 70° C)
- I: Industrial (–40° C to 85° C)
- M: Military (–55° C to 125° C)

(4) For information on the EP220 and EP224, refer to the stand-alone *EP220 & EP224 Classic EPLDs Data Sheet*.

System-Level Features

Table 9 provides a list of system-level features available for each Altera device family.

Table 9. System-Level Features

Device Family	3.3-V Device *(1)*	3.3-V or 5.0-V I/O Pins	PCI Compliance *(1)*	ISP	ICR	JTAG Boundary-Scan Testing	Embedded SRAM	Slew Rate Control	Open Collector Outputs
FLEX 10K	✓	✓	✓ *(2)*		✓	✓	✓	✓	✓
FLEX 8000	✓ *(2)*	✓	✓ *(2)*		✓	✓ *(2)*		✓	
MAX 9000		✓	✓ *(2)*	✓		✓		✓	
MAX 7000	✓ *(2)*	✓	✓ *(2)*					✓	
MAX 7000S		✓	✓ *(2)*	✓		✓ *(2)*		✓	✓
FLASHlogic		✓	✓ *(2)*	✓	✓	✓	✓	✓	✓
MAX 5000									
Classic									

Notes:

(1) See "3.3-Volt Devices" and "Devices with 3.3-V/5.0-V I/O Pins" in this data sheet for a listing of specific devices that provide this feature.

(2) Certain family members provide this system-level feature. Consult the appropriate device family data sheet in this data book for more information.

3.3-V Devices

Table 10 provides information on Altera's general-purpose PLDs for 3.3-V applications. These devices are ideal for low-power systems, such as battery-operated instruments and notebook computers.

Table 10. 3.3-Volt Devices *Note (1)*

Device	Package (2)	Temp. (3)	Speed Grade	Configuration Element	Logic Cells (Flipflops)	Ded. Inputs	I/O Pins	Number of Pins
EPF8282AV	L, T	C	-3	SRAM	208 (282)	4	64, 74	84, 100
EPF8282AV	L, T	C	-4	SRAM	208 (282)	4	64, 74	84, 100
EPF8282AV	L, T	C, I	-5	SRAM	208 (282)	4	64, 74	84, 100
EPF8282V	L, T	C	-3	SRAM	208 (282)	4	64, 74	84, 100
EPF8282V	L, T	C, I	-4	SRAM	208 (282)	4	64, 74	84, 100
EPM7032V	L, T	C	-12	EEPROM	32 (32)	4	32	44
EPM7032V	L, T	C	-15	EEPROM	32 (32)	4	32	44
EPM7032V	L, T	C	-20	EEPROM	32 (32)	4	32	44

Notes:

(1) Preliminary information is shown for some devices. Consult individual device data sheets in this data book for more information or contact Altera for the most current device information.

(2) Package configurations (contact Altera for information on device package availability):
- L: Plastic J-lead chip carrier (PLCC)
- T: Plastic thin quad flat pack (TQFP)

(3) Operating temperature:
- C: Commercial (0° C to 70 ° C)
- I: Industrial (–40° C to 85° C)

Devices with 3.3-V/5.0-V I/O Pins

Table 11 provides information on Altera devices with 3.3-V or 5.0-V I/O pins. These devices—ideal for 3.3-V, 5.0-V, and mixed-voltage systems—have two sets of V_{CC} pins: one for internal and input operation and another for I/O output drivers.

Table 11. Devices with 3.3-V/5.0-V I/O Pins

Device Family	Mixed-Voltage Devices
FLEX 10K	All devices
FLEX 8000	EPF8636A (except 84-pin PLCC packages), EPF8820A, EPF8820, EPF81188A, EPF81188, EPF81500A, and EPF81500
MAX 9000	All devices
MAX 7000	All devices except 44-pin packages
FLASHlogic	All devices

PCI-Compliant Devices

Altera offers devices that meet the 33-MHz peripheral component interconnect (PCI) bus standard. See Table 12. Refer to *Application Brief 140 (PCI Compliance of Altera Devices)* and *Application Note 41 (PCI Bus Applications in Altera Devices)* for more information.

Table 12. PCI-Compliant Devices *Note (1)*

Device	Package (2)	Temp. (3)	Speed Grade	Configuration Element	Logic Cells (Flipflops)	Ded. Inputs	I/O Pins	Number of Pins
EPM9320	R	C	-12	EEPROM	320 (448)	4	112, 128	160, 208
EPM9400	R	C	-12	EEPROM	400 (555)	4	135, 155	208, 240
EPM9480	R	C	-12	EEPROM	480 (651)	4	113, 142, 171	160, 208, 240
EPM9560	R	C	-12	EEPROM	560 (772)	4	149, 187, 212	208, 240, 304
EPF8282A	T	C	A-2	SRAM	208 (282)	4	74	100
EPF8282A	T	C	A-3	SRAM	208 (282)	4	74	100
EPF8452A	Q, T	C	A-2	SRAM	336 (452)	4	116	160
EPF8452A	Q, T	C	A-3	SRAM	336 (452)	4	116	160
EPF8636A	R, Q	C	A-2	SRAM	504 (636)	4	132	160, 208
EPF8636A	R, Q	C	A-3	SRAM	504 (636)	4	132	160, 208
EPF8820A	R	C	A-2	SRAM	672 (820)	4	148	208
EPF8820A	R	C	A-3	SRAM	672 (820)	4	148	208
EPF81188A	R	C	A-2	SRAM	1,008 (1,188)	4	180	240
EPF81188A	R	C	A-3	SRAM	1,008 (1,188)	4	180	240
EPF81500A	R	C	A-2	SRAM	1,296 (1,500)	4	204	304
EPF81500A	R	C	A-3	SRAM	1,296 (1,500)	4	204	304
EPM7032	Q, T	C	-5	EEPROM	32	4	32	44
EPM7032	Q, T	C	-6	EEPROM	32	4	32	44
EPM7032	Q, T	C	-7	EEPROM	32	4	32	44
EPM7064	Q	C	-6	EEPROM	64	4	32, 64	44, 100
EPM7064	Q	C	-7	EEPROM	64	4	32, 64	44, 100
EPM7096	Q	C	-6	EEPROM	96	4	72	100
EPM7096	Q	C	-7	EEPROM	96	4	72	100
EPM7128E	Q	C	-7	EEPROM	128	4	80, 96	100, 160
EPM7128E	Q	C	-10P	EEPROM	128	4	80, 96	100, 160
EPM7160E	Q	C	-7	EEPROM	160	4	80, 100	100, 160
EPM7160E	Q	C	-10P	EEPROM	160	4	80, 100	100, 160
EPM7192E	Q	C	-12P	EEPROM	192	4	120	160
EPM7256E	Q, R	C	-12P	EEPROM	256	4	128, 160	160, 208
EPX880	Q	C	-10	SRAM, FLASH	80	22	104	160
EPX8160	Q	C	-10	SRAM, FLASH	160	48	120	208

Notes to table:

(1) Preliminary information is shown for some devices. Consult individual device data sheets in this data book for more information or contact Altera for the most current device information.

(2) Package configurations (contact Altera for information on device package availability):
- Q: Plastic quad flat pack (PQFP)
- R: Power quad flat pack (RQFP)
- T: Plastic thin quad flat pack (TQFP)

(3) Operating temperature:
- C: Commercial (0° C to 70 ° C)

Military-Compliant Devices

Tables 13 through 17 provide information on Altera's military-compliant FLEX 8000, Configuration EPROM, MAX 7000, MAX 5000, and Classic devices. For more information on Altera's military-qualified devices, consult the *Military Products Data Sheet* in this data book.

Table 13. Military-Qualified FLEX 8000 Devices *Note (1)*

Device	Package (2)	Assurance (3)	Speed Grade	Configuration Element	Logic Cells (Flipflops)	Ded. Inputs	I/O Pins	Number of Pins
EPF8820	G, W	883B	-3	SRAM	672 (820)	4	148	192, 208
9463401MXC	G	DESC	-3	SRAM	672 (820)	4	148	192
9463401MYA	W	DESC	-3	SRAM	672 (820)	4	148	208
EPF81188	G	883B	-3	SRAM	1,008 (1,188)	4	180	232
9473301MXC	G	DESC	-3	SRAM	1,008 (1,188)	4	180	232

Table 14. Military-Qualified Configuration EPROMs for FLEX 8000 Devices *Note (1)*

Device	Package (2)	Assurance (3)	Configuration Element	Description	Number of Pins
EPC1213	D	883B	EPROM	213K × 1-bit serial EPROM designed to configure FLEX 8000 devices	8
9474501MPA	D	DESC	EPROM		8

Table 15. Military-Qualified MAX 7000 Devices *Note (1)*

Device	Package (2)	Assurance (3)	t_{PD1} (ns)	f_{CNT} (MHz)	Configuration Element	Logic Cells (Flipflops)	Ded. Inputs	I/O Pins	Number of Pins
EPM7192E	G	883B	15	76.9	EEPROM	192	4	120	160
EPM7192E	G	833B	20	62.5	EEPROM	192	4	120	160
9316802MXC	G	DESC	15	76.9	EEPROM	192	4	120	160
9316801MXC	G	DESC	20	62.5	EEPROM	192	4	120	160
EPM7256E	G, W	883B	15	76.9	EEPROM	256	4	128, 160	192, 208
EPM7256E	G, W	883B	20	62.5	EEPROM	256	4	128, 160	192, 208
9324702MXC	G	DESC	15	76.9	EEPROM	256	4	128	192
9324701MXC	G	DESC	20	62.5	EEPROM	256	4	128	192
9324702MYA	W	DESC	15	76.9	EEPROM	256	4	160	208
9324701MYA	W	DESC	20	62.5	EEPROM	256	4	160	208

Table 16. Military-Qualified MAX 5000 Devices *Note (1)*

Device	Package (2)	Assurance (3)	t_{PD1} (ns)	f_{CNT} (MHz)	Configuration Element	Logic Cells (Flipflops)	Ded. Inputs	I/O Pins	Number of Pins
EPM5032	D	833B	25	50.0	EPROM	32	8	16	28
9061102XA	D	DESC	25	50.0	EPROM	32	8	16	28
EPM5128	G	883B	30	40.0	EPROM	128	8	52	68
EPM5128	G	883B	35	33.3	EPROM	128	8	52	68
8946801XC	G	DESC	35	33.3	EPROM	128	8	52	68
8946804XC	G	DESC	20	66.7	EPROM	128	8	52	68
EPM5130	G, W	833B	30	40.0	EPROM	128	20	64	100
EPM5130	G, W	833B	35	33.3	EPROM	128	20	64	100
9314402MZC	G	DESC	30	40.0	EPROM	128	20	64	100
9314401MZC	G	DESC	35	33.3	EPROM	128	20	64	100
9314402MXA	W	DESC	30	40.0	EPROM	128	20	64	100
9314401MXA	W	DESC	35	33.3	EPROM	128	20	64	100
EPM5192	G	883B	30	40.0	EPROM	192	8	64	84
EPM5192	G	883B	35	33.3	EPROM	192	8	64	84
9206202MYC	G	DESC	20	66.7	EPROM	192	8	64	84
9206201MYC	G	DESC	30	40.0	EPROM	192	8	64	84
9206204MYC	G	DESC	40	33.3	EPROM	192	8	64	84

Table 17. Military-Qualified Classic Devices *Note (1)*

Device	Package (2)	Assurance (3)	t_{PD1} (ns)	f_{CNT} (MHz)	Configuration Element	Logic Cells (Flipflops)	Ded. Inputs	I/O Pins	Number of Pins
EP600I	D	833B	55	22.2	EPROM	16	4	16	24
8686401LA	D	DESC	55	22.2	EPROM	16	4	16	24
EP610	D	833B	35	28.6	EPROM	16	4	16	24
8947601LA	D	DESC	35	28.6	EPROM	16	4	16	24
EP1800I	G	833B	90	16.1	EPROM	48	16	48	68
8854901XA	G	DESC	90	16.1	EPROM	48	16	48	68
EP1810	G	833B	45	22.2	EPROM	48	16	48	68
8946901YC	G	DESC	45	22.2	EPROM	48	16	48	68

Notes to tables:

(1) All military-qualified devices are rated to military temperatures (–55° C to 125° C). Preliminary data is shown for some other parameters. Consult individual device data sheets in this data book for more information, or contact Altera for the most current device information.

(2) Package configurations (contact Altera for availability of device package options):
- D: Ceramic dual in-line package (CerDIP)
- G: Ceramic pin-grid array (PGA)
- W: Windowed ceramic quad flat pack (CQFP)

(3) Product assurance levels:
- 833B: Processed to MIL-STD-883, current revision.
- DESC: DESC Standard Microcircuit Drawing (SMD). Consult Altera or DESC for availability.

Notes:

March 1995

FLEX 10K Embedded-Array Programmable Logic Device Family


ALTERA
FLEX®
EPF10K10
EPF10K70
EPF10K50
EPF10K30
EPF10K20
EPF10K100
EPF10K40

FLEX 10K

Embedded-Array Programmable Logic Device Family

March 1995, ver. 1 — Advance Information Brief

Features

Preliminary Information

- High-density, embedded-array programmable logic device family
  - 10,000 to 100,000 typical gates (see Table 1)
  - 720 to 5,392 registers
- Fabricated on a 0.5-micron, CMOS SRAM process
- First embedded-array device in the programmable logic industry
- In-circuit reconfigurable (ICR)
- Input/output registers on all I/O pins
- Fast, efficient megafunction implementation, including memory, digital signal processing (DSP), specialized arithmetic logic, microprocessors, and microcontrollers
- Dedicated carry chain that implements fast adders and counters
- Dedicated cascade chain for efficient implementation of high-speed, high-fan-in logic functions
- Internal tri-state bus support for system integration
- Multiple Clock trees for low Clock skew in multi-Clock systems
- Programmable output slew-rate to reduce switching noise
- Built-in Joint Test Action Group (JTAG) boundary-scan test (BST) circuitry
- 3.3-V or 5.0-V operation
- Software support provided by Altera's MAX+PLUS II development system on 486- and Pentium-based PCs, and Sun SPARCstation, HP 9000 Series 700, and IBM RISC System/6000 workstations
- Available in a variety of package options with 84 to 562 pins

Table 1. FLEX 10K Device Family

Features	EPF10K10	EPF10K20	EPF10K30	EPF10K40	EPF10K50	EPF10K70	EPF10K100
Typical gates (logic and RAM)	10,000	20,000	30,000	40,000	50,000	70,000	100,000
Usable gates	7,000 to 31,000	15,000 to 63,000	22,000 to 69,000	29,000 to 93,000	36,000 to 116,000	46,000 to 118,000	62,000 to 158,000
Logic elements	576	1,152	1,728	2,304	2,880	3,744	4,992
RAM bits	6,144	12,288	12,288	16,384	20,480	18,432	24,576
Flipflops	720	1,344	1,968	2,576	3,184	4,096	5,392
Maximum user I/O pins	150	198	246	278	310	358	406

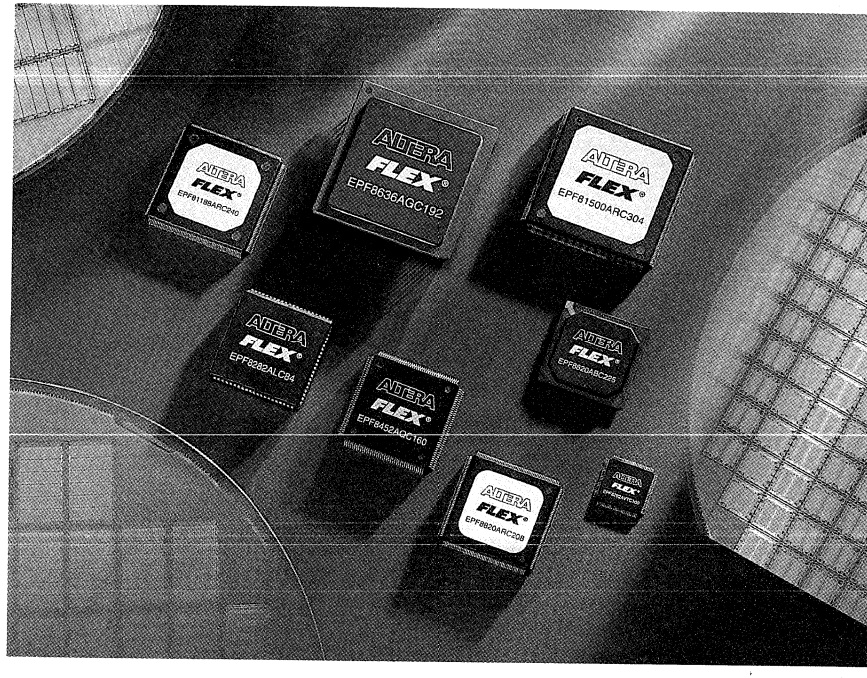
For additional information on FLEX 10K devices, contact Altera Marketing at (408) 894-7104.

Notes:

March 1995

FLEX 8000 Programmable Logic Device Family

EPF8050M: FLEX 8000M Programmable Logic Device


ALTERA
FLEX®
EPF8636AGC192
EPF81500ARC304
EPF8282ALC84
EPF8452AQC160
EPF8820ARC208

Includes FLEX 8000A

FLEX 8000

Programmable Logic Device Family

March 1995, ver. 6 | Data Sheet

Features...

- Low-cost, high-density, register-rich CMOS programmable logic device family
  - 2,500 to 16,000 usable gates
  - 282 to 1,500 registers (see Table 1)
- FLEX 8000 devices fabricated on a 0.8-micron SRAM process
- Higher-speed FLEX 8000A devices fabricated on a 0.6-micron SRAM process
- Supports in-circuit reconfiguration
- FastTrack continuous routing structure for fast, predictable interconnect delays
- Dedicated carry chain that can implement fast adders and counters
- Dedicated cascade chain for efficient implementation of high-speed, high-fan-in logic functions
- Full compliance with the Peripheral Component Interconnect (PCI) standard for FLEX 8000A devices
- Low power consumption (less than 1 mA in standby mode)
- 3.3-V or 5.0-V operation
  - Full 3.3-V EPF8282V
  - 3.3-V or 5.0-V I/O for EPF8636A and larger devices

Table 1. FLEX 8000 Device Features

Feature	EPF8282 EPF8282V EPF8282A EPF8282AV	EPF8452 EPF8452A	EPF8636A	EPF8820 EPF8820A	EPF81188 EPF81188A	EPF81500 EPF81500A
Available gates	5,000	8,000	12,000	16,000	24,000	32,000
Usable gates	2,500	4,000	6,000	8,000	12,000	16,000
Flipflops	282	452	636	820	1,188	1,500
Logic Elements	208	336	504	672	1,008	1,296
Max. user I/O pins	78	120	136	152	184	208
JTAG BST circuitry	Yes	No	Yes	Yes	No	Yes
Packages *Note (1)*	84-pin PLCC 100-pin TQFP	84-pin PLCC 160-pin PQFP 160-pin PGA 100-pin TQFP	84-pin PLCC 160-pin PQFP 192-pin PGA 208-pin RQFP	160-pin PQFP 192-pin PGA 208-pin RQFP 225-pin BGA	208-pin PQFP 232-pin PGA 240-pin RQFP	240-pin RQFP 280-pin PGA 304-pin RQFP

Note:
(1) Contact Altera for information on package availability.

...and More Features

- Built-in Joint Test Action Group (JTAG) boundary-scan test (BST) circuitry
- Programmable output slew-rate control to reduce switching noise
- Available in a variety of packages with 84 to 304 pins (see Table 1)
- Software design support provided by the Altera MAX+PLUS II development system for 486- and Pentium-based PCs and Sun SPARCstation, HP 9000 Series 700, and IBM RISC System/6000 workstations

General Description

Altera's Flexible Logic Element MatriX (FLEX) family combines the benefits of both erasable programmable logic devices (EPLDs) and field-programmable gate arrays (FPGAs). The fine-grained architecture and high register count characteristic of FPGAs are combined with the high speed and predictable interconnect delays of EPLDs to make the FLEX 8000 device family ideal for a wide range of applications. Logic is implemented with compact 4-input look-up tables (LUTs) and programmable registers. High performance is provided by a fast, continuous network of routing resources.

FLEX 8000 devices provide a large number of storage elements for applications such as digital signal processing, wide data-path manipulation, and data transformation. These devices are an excellent choice for bus interfaces, TTL integration, coprocessor functions, and high-speed controllers. The high-pin-count packages can integrate multiple 32-bit buses into a single device. Table 2 shows the performance of FLEX 8000 devices as shown in benchmarks of typical applications.

Table 2. FLEX 8000 Performance *Note (1)*

		FLEX 8000A Devices			FLEX 8000 Devices		
Application	Logic Elements Used	A-2 Speed Grade	A-3 Speed Grade	A-4 Speed Grade	-2 Speed Grade	-3 Speed Grade	Unit
16-bit loadable counter	16	125	95	83	71	45	MHz
16-bit up/down counter	16	125	95	83	71	45	MHz
16-bit prescaled counter	24	270	232	185	142	115	MHz
24-bit accumulator	24	87	67	58	50	32	MHz
16-bit address decode	4	4.2	4.9	6.3	7.8	12.0	ns
16-to-1 multiplexer	10	6.6	7.9	9.5	12.7	18.0	ns

Note:
(1) The A-6 speed grade yields the same results as the -3 speed grade.

All FLEX 8000 device packages provide four dedicated inputs for synchronous control signals with large fan-outs. Each I/O pin has an associated register on the periphery of the device. As outputs, these registers provide fast Clock-to-output times; as inputs, they offer quick setup times.

The logic and interconnections in the FLEX 8000 architecture are configured with CMOS SRAM elements. FLEX 8000 devices are configured at system power-up with data stored in an Altera serial Configuration EPROM device or provided by a system controller. Altera offers the EPC1213 and EPC1064 Configuration EPROMs, which configure FLEX 8000 devices via a serial data stream. Configuration data can also be stored in an industry-standard 32K × 8-bit or larger EPROM or downloaded from system RAM. After a FLEX 8000 device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Because reconfiguration requires less than 100 ms, real-time changes can be made during system operation.

The FLEX 8000 family is supported by Altera's MAX+PLUS II development system, a single, integrated package that offers schematic, text—including the Altera Hardware Description Language (AHDL)—and waveform design entry; compilation and logic synthesis; simulation and timing analysis; and device programming. MAX+PLUS II provides EDIF 2 0 0 and 3 0 0, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and workstation-based EDA tools. MAX+PLUS II runs on 486- and Pentium-based PCs, and Sun SPARCstation, HP 9000 Series 700, and IBM RISC System/6000 workstations.

For more information, go to the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* in this data book.

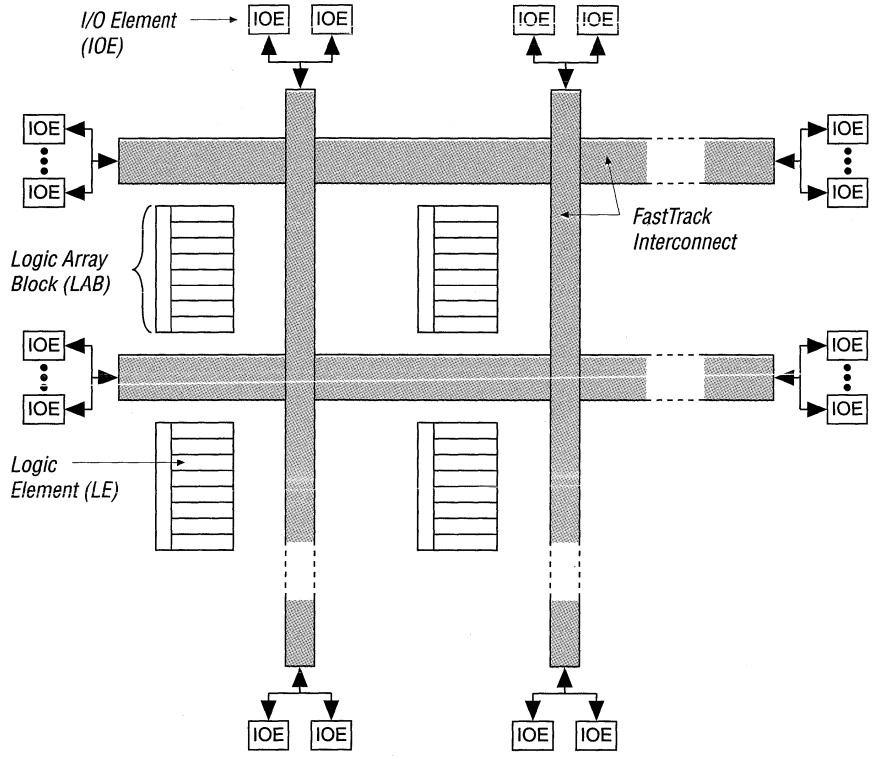
Functional Description

The FLEX 8000 architecture incorporates a large matrix of compact building blocks called logic elements (LEs). Each LE contains a 4-input LUT that provides combinatorial logic capability and a programmable register that offers sequential logic capability. The fine-grained structure of the LE provides highly efficient logic implementation.

LEs are grouped into sets of eight to create Logic Array Blocks (LABs). Each FLEX 8000 LAB is an independent structure with common inputs, interconnections, and control signals. The LAB architecture provides a coarse-grained structure for high device performance and easy routing.

Figure 1 shows a block diagram of the FLEX 8000 architecture. Each group of eight LEs is combined into an LAB; LABs are arranged into rows and columns. The I/O pins are supported by I/O elements (IOEs) located at the ends of rows and columns. Each IOE contains a bidirectional I/O buffer and a flipflop that can be used as either an input or output register.

Figure 1. FLEX 8000 Device Block Diagram

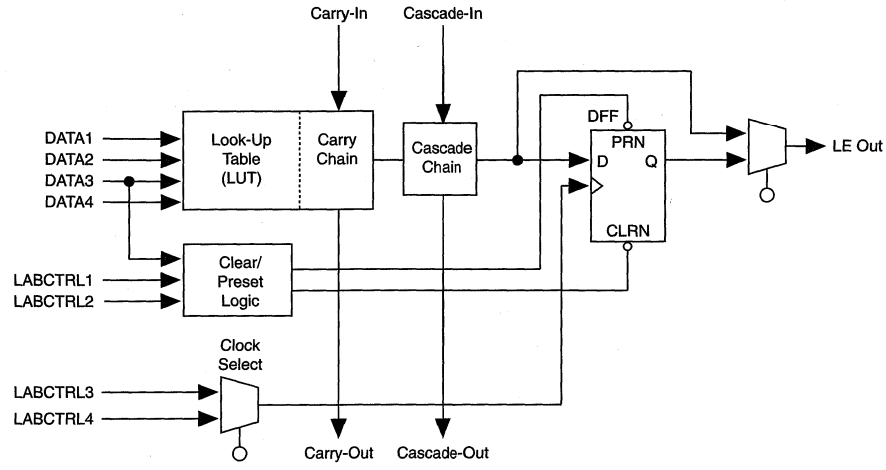


Signal interconnections within FLEX 8000 devices and to and from device pins are provided by the FastTrack Interconnect, a series of fast, continuous channels that run the entire length and width of the device. IOEs are located at the end of each row (horizontal) and column (vertical) FastTrack Interconnect path.

Logic Element

The logic element (LE) is the smallest unit of logic in the FLEX 8000 architecture, with a compact size that provides efficient logic utilization. Each LE contains a four-input LUT, a programmable flipflop, a carry chain, and a cascade chain. Figure 2 shows a block diagram of the LE.

Figure 2. FLEX 8000 Logic Element (LE)



The LUT is a function generator that can quickly compute any function of four variables. The programmable flipflop in the LE can be configured for D, T, JK, or SR operation. The Clock, Clear, and Preset control signals on the flipflop can be driven by dedicated input pins, general-purpose I/O pins, or any internal logic. For purely combinatorial functions, the flipflop is bypassed and the output of the LUT goes directly to the output of the LE.

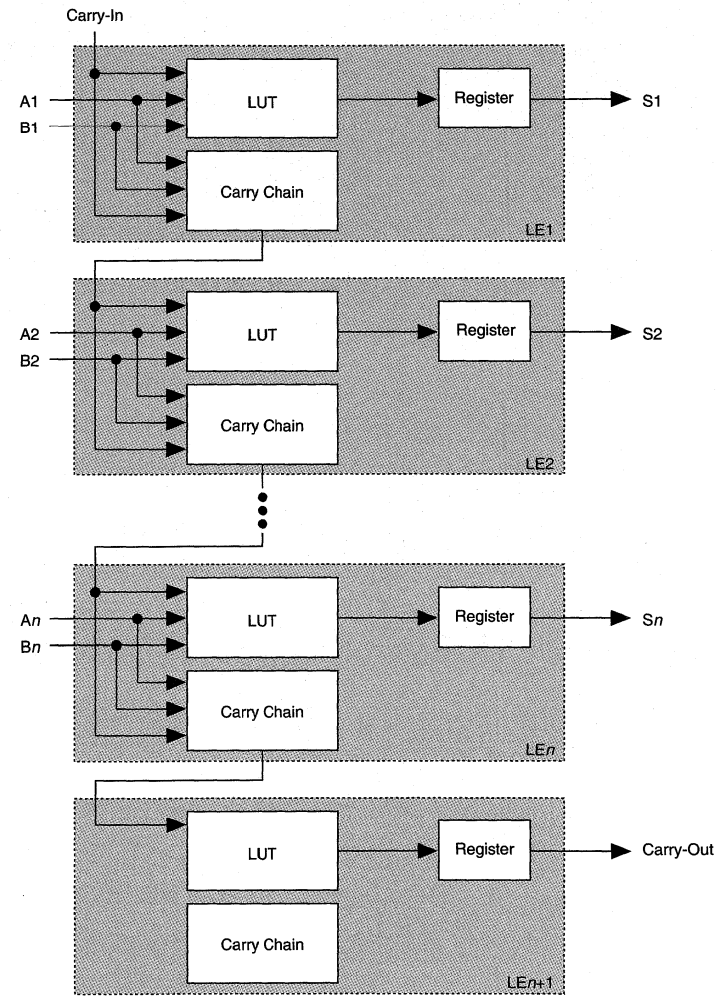
The FLEX 8000 architecture provides two dedicated high-speed data paths—carry chains and cascade chains—that connect adjacent LEs without using local interconnect paths. The carry chain supports high-speed counters and adders; the cascade chain implements wide-input functions with minimum delay. Carry and cascade chains connect all LEs in an LAB and all LABs in the same row. Heavy use of carry and cascade chains can reduce the routing resources available for implementing other logic. Therefore, the use of carry and cascade chains should be limited to speed-critical portions of a design.

Carry Chain

The carry chain provides a very fast (less than 1 ns) carry-forward function between LEs. The carry-in signal from a lower-order bit moves forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the FLEX 8000 architecture to implement high-speed counters and adders of arbitrary width. The MAX+PLUS II Compiler can create carry chains automatically during design processing; designers can also insert carry chain logic manually during design entry.

Figure 3 shows how an *n*-bit full adder can be implemented in *n*+1 LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register is typically bypassed for simple adders, but can be used for an accumulator function. Another portion of the LUT and the carry chain logic generate the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it can be used as a general-purpose signal. In addition to mathematical functions, carry chain logic supports very fast counters and comparators.

Figure 3. Carry Chain Operation



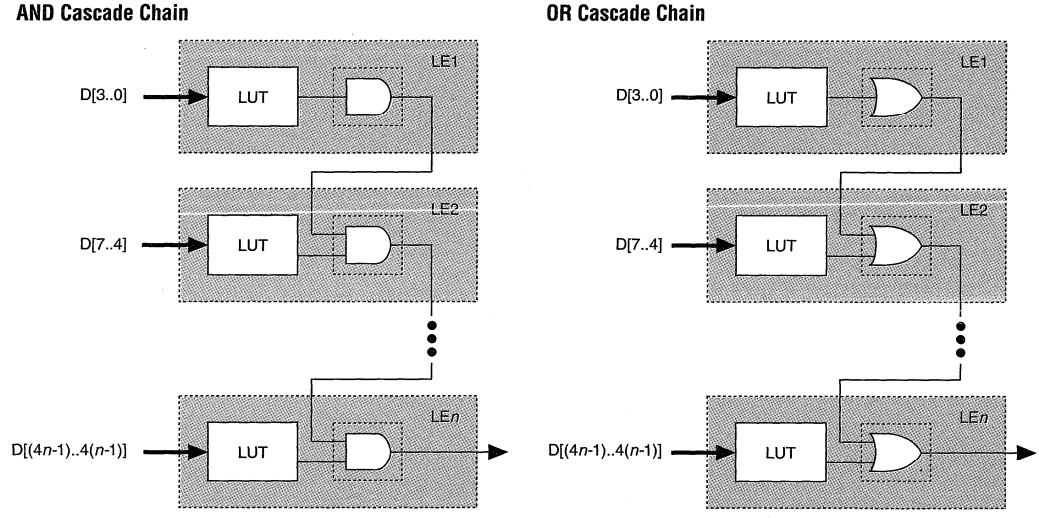
Cascade Chain

With the cascade chain, the FLEX 8000 architecture can implement functions that have a very wide fan-in. Adjacent LUTs can be used to compute portions of the function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via De Morgan's inversion) to connect the outputs of

adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a delay of approximately 1 ns per LE. The MAX+PLUS II Compiler can create cascade chains automatically during design processing; designers can also insert cascade chain logic manually during design entry.

Figure 4 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in. These examples show functions of $4n$ variables implemented with n LEs. For a device with an A-2 speed grade, the LUT delay is approximately 1.6 ns; the cascade chain delay is 0.6 ns. With the cascade chain, 4.2 ns is needed to decode a 16-bit address.

Figure 4. Cascade Chain Operation

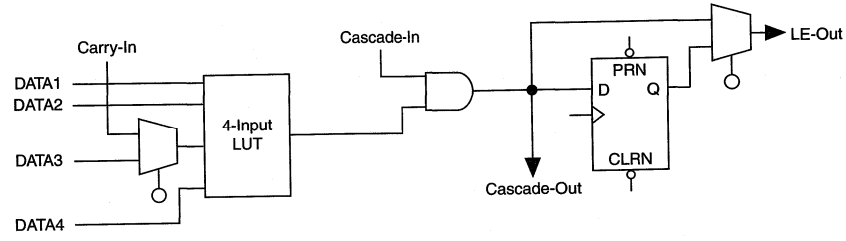


Logic Element Operating Modes

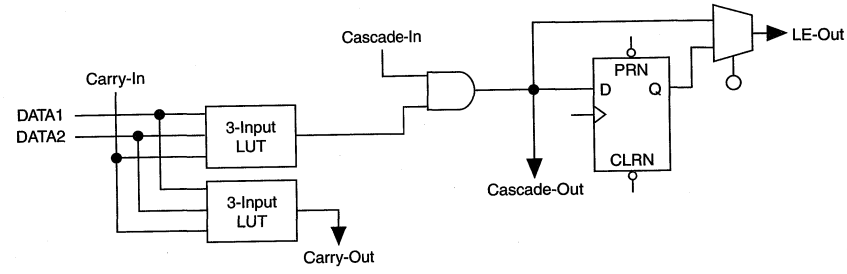
The FLEX 8000 logic element can operate in one of four modes, each of which uses LE resources differently. See Figure 5. In each mode, seven of the ten available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. The three remaining inputs to the LE provide Clock, Clear, and Preset control for the register. The MAX+PLUS II software automatically chooses the appropriate mode for each application. Design performance can also be enhanced by designing for the operating mode that supports the desired application.

Figure 5. FLEX 8000 Logic Element Operating Modes

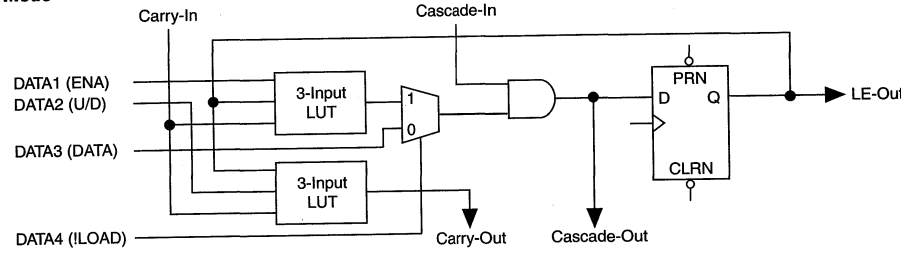
Normal Mode



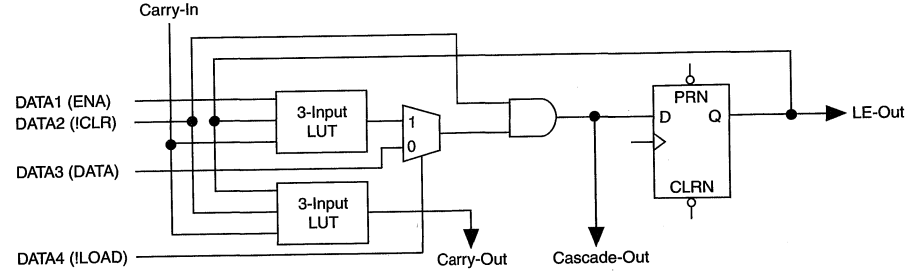
Arithmetic Mode



Up/Down Counter Mode



Clearable Counter Mode



Normal Mode

The Normal mode is suitable for general logic applications and wide decode functions that can take advantage of a cascade chain. In Normal mode, four data inputs from the LAB local interconnect and the carry-in are the inputs to a 4-input LUT. Using a configurable SRAM bit, the MAX+PLUS II Compiler automatically selects the carry-in or the DATA3 signal as an input. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. The LE-out signal—the data output of the LE—is either the combinatorial output of the LUT and cascade chain, or the data (Q) output of the programmable register.

Arithmetic Mode

The Arithmetic mode offers two 3-input LUTs that are ideal for implementing adders, accumulators, and comparators. One LUT provides a 3-bit function; the other generates a carry bit. As shown in Figure 5, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, in an adder, this output would be the sum of three bits: A, B, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The Arithmetic mode also supports a cascade chain.

Up/Down Counter Mode

The Up/Down Counter mode offers counter enable, synchronous up/down control, and data loading options. These control signals are generated by the data inputs from the LAB local interconnect, the carry-in signal, and output feedback from the programmable register. Two 3-input LUTs are used: one generates the counter data, the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading. Data can also be loaded asynchronously with the Clear and Preset register control signals, without using the LUT resources.

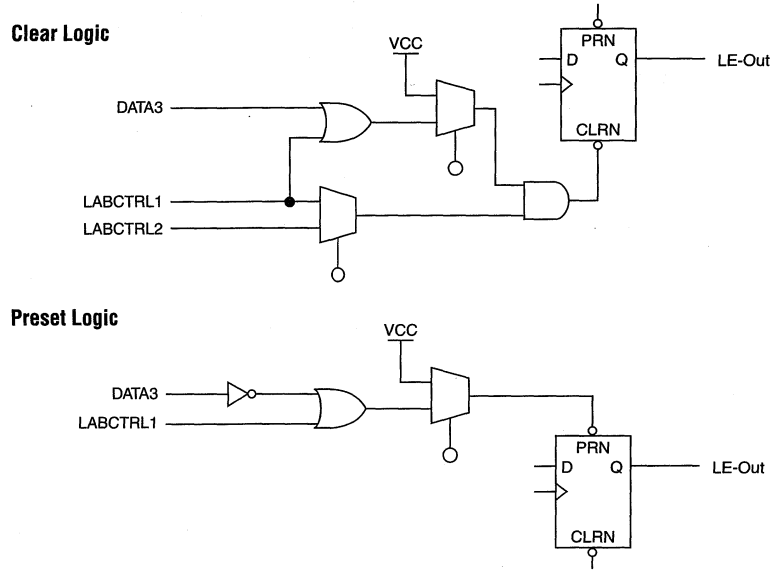
Clearable Counter Mode

The Clearable Counter mode is similar to the Up/Down Counter mode, but supports a synchronous Clear instead of the up/down control. The Clear function is substituted for the cascade-in signal in the Up/Down Counter mode. Two 3-input LUTs are used: one generates the counter data, the other generates the fast carry bit. Synchronous loading is provided by a 2-to-1 multiplexer, the output of which is ANDed with a synchronous Clear.

Clear/Preset Logic Control

Logic for the programmable register's Clear and Preset functions is controlled by the DATA3, LABCTRL1, and LABCTRL2 inputs to the LE. See Figure 6.

Figure 6. Logic Element Clear & Preset Logic

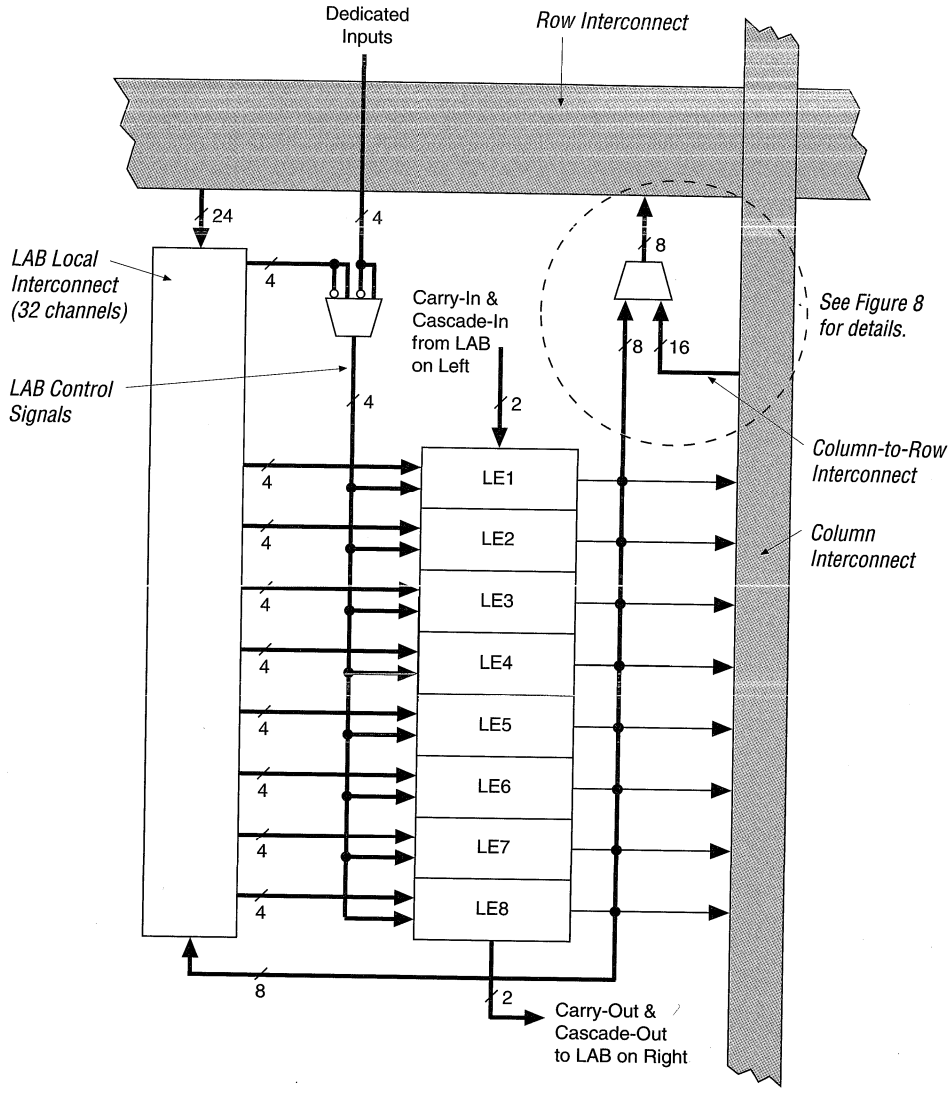


The Clear function is controlled by DATA3, LABCTRL1, and LABCTRL2; the Preset function is controlled by DATA3 and LABCTRL1. The MAX+PLUS II Compiler automatically selects the best control signal implementation during compilation. Since the Clear and Preset functions are active low, the Compiler automatically assigns a logic high to an unused Clear and/or Preset. Preset control can also be provided by using a Clear and inverting the output of the register. Inversion control is available for the inputs to both LEs and IOEs. If a register is cleared by only one of the two LABCTRL signals, the DATA3 input is not required and can be used for one of the LE operating modes.

Logic Array Block

A Logic Array Block (LAB) consists of eight LEs, their associated carry and cascade chains, LAB control signals, and the LAB local interconnect. The LAB provides the coarse-grained structure of the FLEX 8000 architecture. This structure enables FLEX 8000 devices to provide efficient routing, high device utilization, and high performance. Figure 7 shows a block diagram of the FLEX 8000 LAB.

Figure 7. Logic Array Block (LAB)



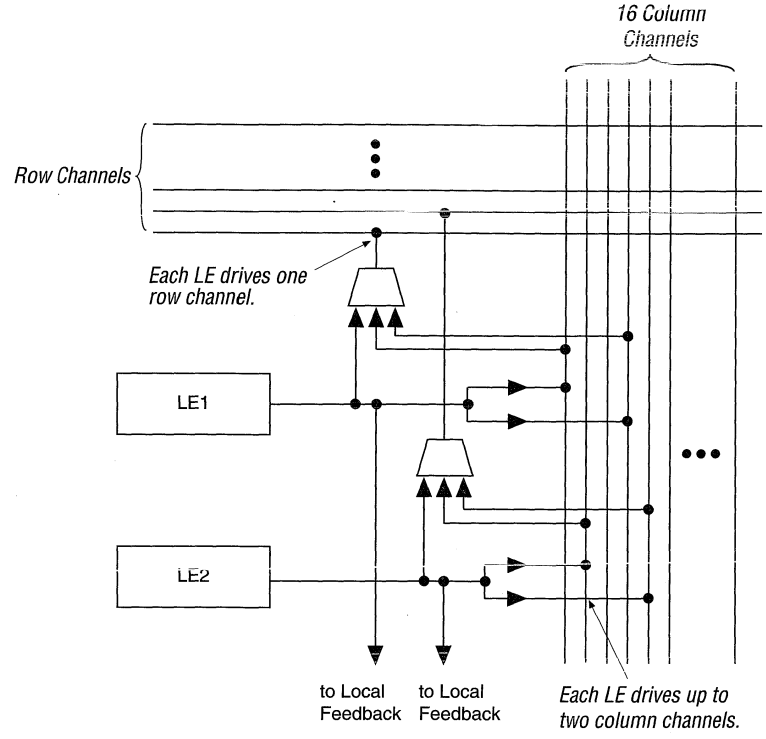
Each LAB provides four control signals that can be used in all eight LEs. Two of these signals can be used as Clocks, the other two for Clear/Preset control. The LAB control signals can be driven directly from a dedicated input pin, an I/O pin, or any internal signal via the LAB local interconnect. The dedicated inputs are typically used for global Clock, Clear, or Preset signals because they provide synchronous control with very low skew across the device. FLEX 8000 devices support up to four individual global Clock, Clear, or Preset control signals. If logic is required on a control signal, it can be generated in one or more LEs in any LAB and driven into the local interconnect of the target LAB. Programmable inversion is available for all four LAB control signals.

FastTrack Interconnect

In the FLEX 8000 architecture, connections between LEs and device I/O pins are provided by the FastTrack Interconnect, a series of continuous horizontal and vertical routing channels that traverse the entire FLEX 8000 device. This device-wide routing structure provides predictable performance even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

The LABs within FLEX 8000 devices are arranged into a matrix of columns and rows. Each row of LABs has a dedicated row interconnect that routes signals both into and out of the LABs in the row. The row interconnect can then drive I/O pins or feed other LABs in the device. Figure 8 shows how an LE drives the row and column interconnect.

Figure 8. LAB Connections to Row & Column Interconnect



Each LE in an LAB can drive up to 2 separate column interconnect channels. Therefore, all 16 available column channels can be driven by the LAB. The column channels run vertically across the entire device, and share access to LABs in the same column but in different rows. The MAX+PLUS II Compiler chooses which LEs must be connected to a column channel. A row interconnect channel can be fed by the output of the LE or by 2 column channels. These 3 signals feed a multiplexer that connects to a specific row channel. Each LE is connected to one 3-to-1 multiplexer. In an LAB, the multiplexers provide all 16 column channels with access to 8 row channels.

Each column of LABs has a dedicated column interconnect that routes signals out of the LABs into the column. The column interconnect can then drive I/O pins or feed into the row interconnect to route the signals to other LABs in the device. A signal from the column interconnect, which can be either the output of an LE or an input from an I/O pin, must transfer to the row interconnect before it can enter an LAB. Table 3 summarizes the FastTrack Interconnect resources available in each FLEX 8000 device.

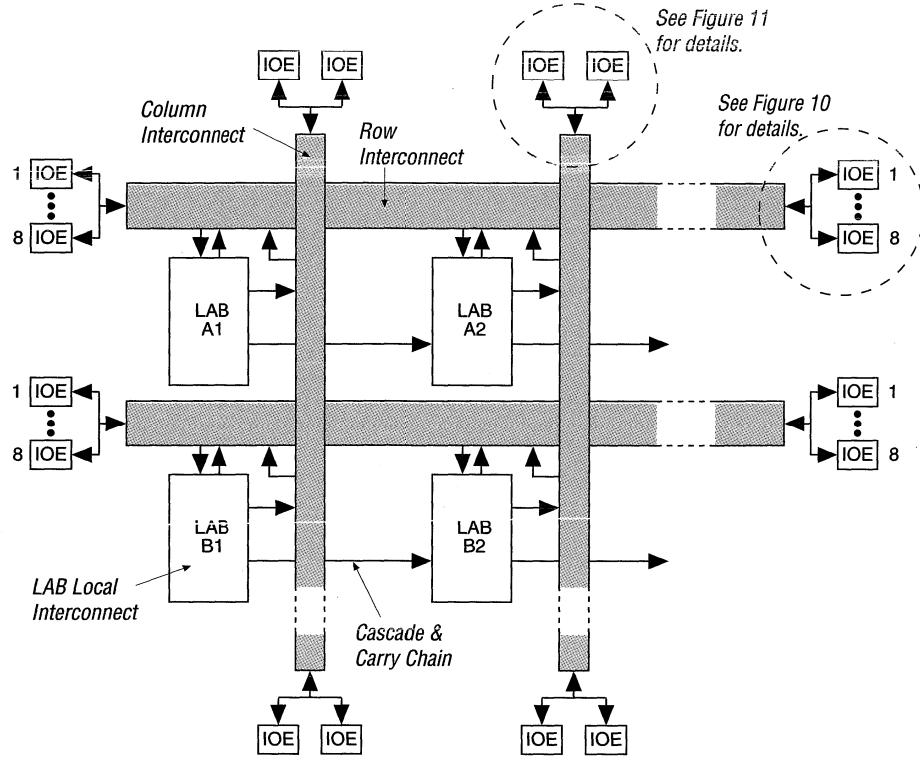
Table 3. FLEX 8000 FastTrack Interconnect Resources

Device	Rows	Channels per Row	Columns	Channels per Column
EPF8282 EPF8282V EPF8282A EPF8282AV	2	168	13	16
EPF8452 EPF8452A	2	168	21	16
EPF8636A	3	168	21	16
EPF8820 EPF8820A	4	168	21	16
EPF81188 EPF81188A	6	168	21	16
EPF81500 EPF81500A	6	216	27	16

Figure 9 shows the interconnection of four adjacent LABs, with row, column, and local interconnects, as well as the associated cascade and carry chains.

Figure 9. FLEX 8000 Device Interconnect Resources

Each LAB is named according to its physical row (A, B, C, etc.) and column (1, 2, 3, etc.) position within the device.

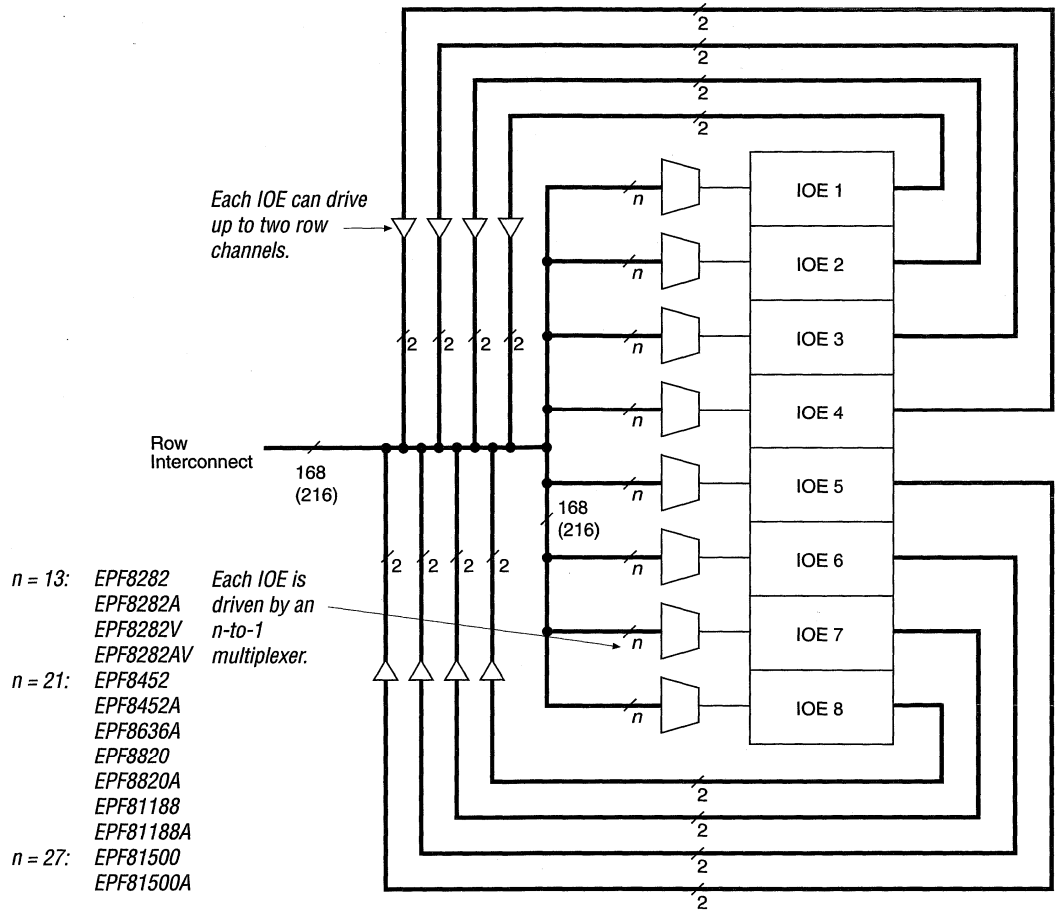


Row-to-IOE Connections

Figure 10 illustrates the connection between row interconnect channels and IOEs. An input signal from an IOE can drive two separate row channels. When an IOE is used as an output, the signal is driven by an *n*-to-1 multiplexer that selects the row channels. The size of the multiplexer varies with the number of columns in a device. EPF81500 and EPF81500A devices use a 27-to-1 multiplexer; EPF81188, EPF81188A, EPF8820, EPF8820A, EPF8636A, EPF8452, and EPF8452A devices use a 21-to-1 multiplexer; and EPF8282, EPF8282A, EPF8282V and EPF8282AV devices use a 13-to-1 multiplexer. Eight IOEs are connected to each side of the row channels.

Figure 10. FLEX 8000 Row-to-IOE Connection

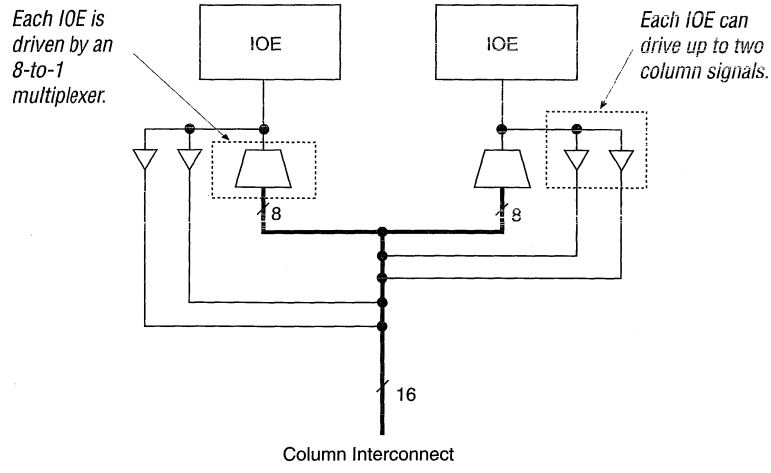
Numbers in parentheses are for EPF81500 & EPF81500A devices.



Column-to-IOE Connections

Two IOEs are located at the top and bottom of the column channels (see Figure 11). When an IOE is used as an input, it can drive up to 2 separate column channels. The output signal to an IOE can choose from 8 of the 16 column channels through an 8-to-1 multiplexer.

Figure 11. FLEX 8000 Column-to-IOE Connection

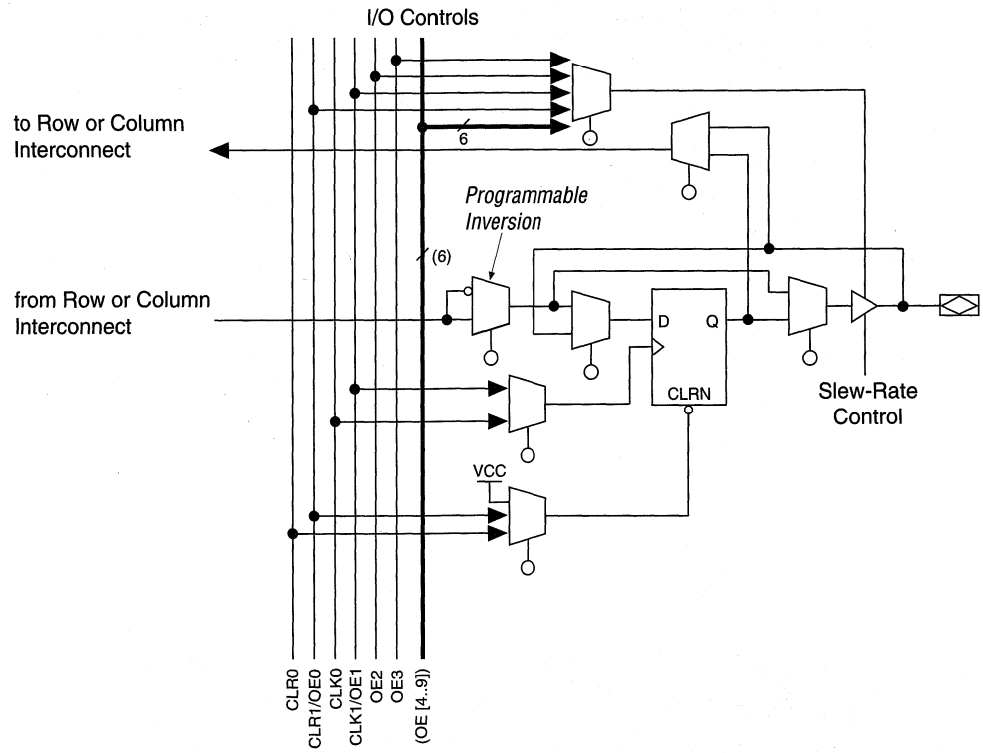


In addition to the general-purpose I/O pins, FLEX 8000 devices have four dedicated input pins. These dedicated inputs provide low-skew, device-wide signal distribution, and are typically used for global Clock, Clear, and Preset control signals. The signals from the dedicated inputs are available as control signals for all LABs and I/O elements in the device. The dedicated inputs can also be used as general-purpose data inputs because they can feed the local interconnect of each LAB in the device.

Figure 12 shows the IOE block diagram. Signals enter the FLEX 8000 device either from the I/O pins that provide general-purpose input capability or from the four dedicated inputs. The IOEs are located at the ends of the row and column interconnect channels.

Figure 12. I/O Element (IOE)

Numbers in parentheses are for EPF81500 and EPF81500A devices only.



I/O pins can be used as input, output, or bidirectional pins. Each I/O pin has a register that can be used either as an input register for external data that requires fast setup times, or as an output register for data that requires fast Clock-to-output performance. The MAX+PLUS II Compiler uses the programmable inversion option to automatically invert signals from the row and column interconnect when appropriate.

The output buffer in each IOE has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A slow slew rate reduces system noise and adds a maximum delay of 4 ns. The fast slew rate should be used for speed-critical outputs in systems that are adequately protected against noise. Designers can specify the slew rate on a pin-by-pin basis during design entry or assign a default slew rate to all pins on a global basis.

The Clock, Clear, and Output Enable controls for the IOEs are provided by a network of I/O control signals. These signals can be supplied by either the dedicated input pins or internal logic. The IOE control-signal paths are designed to minimize the skew across the device. All control-signal sources are buffered onto high-speed drivers that drive the signals around the periphery of the device. This "peripheral bus" can be configured to provide up to four Output Enable signals (ten in the EPF81500 and EPF81500A), and up to two Clock or Clear signals. Figure 12 illustrates how two Output Enable signals are shared with one Clock (CLK1) and one Clear (CLR1) signal.

The signals for the peripheral bus can be generated by any of the 4 dedicated inputs or signals on the row interconnect channels, as shown in Figure 13. The number of row channels used correlates to the number of columns in the FLEX 8000 device. EPF8282, EPF8282A, EPF8282V, and EPF8282AV devices, for example, use 13 channels; EPF8452, EPF8452A, EPF8636A, EPF8820, EPF8820A, EPF81188, and EPF81188A devices use 21 channels; and EPF81500 and EPF81500A devices use 27 channels. The first LE in each LAB is the source of the row channel signal. The 6 peripheral control signals (12 in EPF81500 and EPF81500A devices) can be accessed by every I/O element.

Figure 13. FLEX 8000 Peripheral Bus

Numbers in parentheses are for EPF81500 and EPF81500A devices.

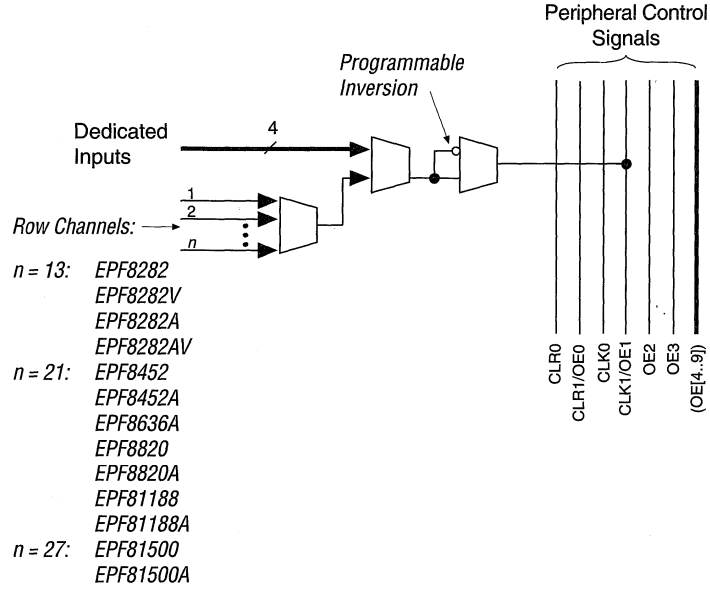


Table 4 lists the source of the peripheral control signal for each FLEX 8000 device by row.

Table 4. Row Sources of Peripheral Control Signals

Peripheral Control Signal	EPF8282 EPF8282V EPF8282A EPF8282AV	EPF8452 EPF8452A	EPF8636A	EPF8820 EPF8820A	EPF81188 EPF81188A	EPF81500 EPF81500A
CLK0	Row A	Row A	Row A	Row A	Row E	Row E
CLK1/OE1	Row B	Row B	Row C	Row C	Row B	Row B
CLR0	Row A	Row A	Row B	Row B	Row F	Row F
CLR1/OE0	Row B	Row B	Row C	Row D	Row C	Row C
OE2	Row A	Row A	Row A	Row A	Row D	Row A
OE3	Row B	Row B	Row B	Row B	Row A	Row A
OE4	–	–	–	–	–	Row B
OE5	–	–	–	–	–	Row C
OE6	–	–	–	–	–	Row D
OE7	–	–	–	–	–	Row D
OE8	–	–	–	–	–	Row E
OE9	–	–	–	–	–	Row F

3.3-V or 5.0-V I/O Operation

Many members of the FLEX 8000 family, including the EPF81500, EPF81500A, EPF81188, EPF81188A, EPF8820, EPF8820A, and EPF8636A devices (except the 84-pin PLCC EPF8636A), can be set for 3.3-V or 5.0-V operation. These devices have one set of V_{CC} pins for internal operation and input buffers (V_{CCINT}), and another set for I/O output drivers (V_{CCIO}).

The V_{CCINT} pins must always be connected to a 5.0-V power supply. With a 5.0-V V_{CCINT} level, input voltages are at TTL levels and are therefore compatible with 3.3-V and 5.0-V inputs. The V_{CCIO} pins can be connected to either a 3.3-V or 5.0-V power supply, depending on the output requirements. When the V_{CCIO} pins are connected to a 5.0-V power supply, the output levels are compatible with 5.0-V systems. When the V_{CCIO} pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V systems. Devices operating with a V_{CCIO} levels lower than 4.75 V incur a nominal additional timing delay, therefore the t_{OD2} parameter is used in place of t_{OD1}.

JTAG Operation

The EPF8282, EPF8282A, EPF8282V, EPF8282AV, EPF8636A, EPF8820, EPF8820A, EPF81500, and EPF81500A devices provide Joint Test Action Group (JTAG) boundary-scan testing circuitry. For detailed information on JTAG operation in these FLEX 8000 devices, refer to *Application Note 39 (JTAG Boundary-Scan Testing in Altera Devices).*

Timing Model

The continuous, high-performance FastTrack Interconnect routing resources ensure predictable performance and accurate simulation analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and hence have unpredictable performance. Timing simulation and delay prediction are available with the MAX+PLUS II Simulator and Timing Analyzer, or with industry-standard EDA tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time prediction, and system-level performance analysis.

Tables 5 through 8 describe the FLEX 8000 timing parameters and their symbols.

Table 5. FLEX 8000 Internal Timing Parameters *Note (1)*

Symbol	Parameter
t_{IOD}	IOE register data delay
t_{IOC}	IOE register control signal delay
t_{IOE}	Output enable delay
t_{IOCO}	IOE register clock-to-output delay
t_{IOCOMB}	IOE combinatorial delay
t_{IOSU}	IOE register setup time before clock
t_{IOH}	IOE register hold time after clock
t_{IOCLR}	IOE register clear delay
t_{IN}	Input pad and buffer delay
t_{OD1}	Output buffer and pad delay, slow slew rate = off, V_{CCIO} = 5.0 V, C1 = 35 pF, *Note (2)*
t_{OD2}	Output buffer and pad delay, slow slew rate = off, V_{CCIO} = 3.3 V, C1 = 35 pF, *Note (3)*
t_{OD3}	Output buffer and pad delay, slow slew rate = on, C1 = 35 pF, *Note (4)*
t_{XZ}	Output buffer disable delay, C1 = 5 pF
t_{ZX1}	Output buffer enable delay, slow slew rate = off, V_{CCIO} = 5.0 V, C1 = 35 pF
t_{ZX2}	Output buffer enable delay, slow slew rate = off, V_{CCIO} = 3.3 V, C1 = 35 pF, *Note (3)*
t_{ZX3}	Output buffer enable delay, slow slew rate = on, C1 = 35 pF, *Note (4)*

Table 6. FLEX 8000 Logic Element Timing Parameters *Note (1)*

Symbol	Parameter
t_{LUT}	LUT delay for data-in
t_{CLUT}	LUT delay for carry-in
t_{RLUT}	LUT delay for LE register feedback
t_{GATE}	Cascade gate delay
t_{CASC}	Cascade chain routing delay
t_{CICO}	Carry-in to carry-out delay
t_{CGEN}	Data-in to carry-out delay
t_{CGENR}	LE register feedback to carry-out delay
t_{C}	LE register control signal delay
t_{CH}	Clock high time
t_{CL}	Clock low time
t_{CO}	LE register clock-to-output delay
t_{COMB}	Combinatorial delay
t_{SU}	LE register setup time before clock
t_{H}	LE register hold time after clock
t_{PRE}	LE register preset delay
t_{CLR}	LE register clear delay

Table 7. FLEX 8000 Interconnect Timing Parameters *Note (1)*

Symbol	Parameter
$t_{LABCASC}$	Cascade delay between LEs in different LABs
$t_{LABCARRY}$	Carry delay between LEs in different LABs
t_{LOCAL}	LAB local interconnect delay
t_{ROW}	Row interconnect routing delay, *Note (5)*
t_{COL}	Column interconnect routing delay
t_{DIN_C}	Dedicated input to LE control delay
t_{DIN_D}	Dedicated input to LE data delay, *Note (5)*
t_{DIN_IO}	Dedicated input to IOE control delay

Table 8. FLEX 8000 External Reference Timing Characteristics *Note (6)*

Symbol	Parameter
t_{DRR}	Register-to-register delay via 4 LEs, 3 row interconnects, and 4 local interconnects, *Note (7)*

Notes to tables:

(1) Internal timing parameters cannot be measured explicitly. They are worst-case delays based on testable and guaranteed external parameters. Internal parameters should be used for estimating device performance. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.

(2) V_{CCIO} = 5.0 V ± 5% for commercial use.
V_{CCIO} = 5.0 V ± 10% for industrial and military use.

(3) V_{CCIO} = 3.3 V ± 10% for all temperature grades.

(4) For t_{OD3} and t_{ZX3} parameters, V_{CCIO} = 3.3 V or 5.0 V.

(5) The t_{ROW} and t_{DIN_D} delays are worst-case values for typical applications. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.

(6) External reference timing characteristics are factory-tested, guaranteed worst-case values. A representative subset of signal paths is tested to approximate typical device applications.

(7) Contact Altera Applications at (800) 800-EPLD for more information on test conditions.

The FLEX 8000 timing model in Figure 14 shows the delays that correspond to various paths and functions in the circuit. This model contains three distinct parts: the LE; the IOE; and the interconnect, including the row and column FastTrack Interconnect, LAB local interconnect, and carry and cascade interconnect paths. Each parameter shown in Figure 14 is expressed as a worst-case value in the "Timing Parameters" tables in this data sheet. Hand-calculations that use the FLEX 8000 timing model and these timing parameters can be used to estimate FLEX 8000 device performance. Timing simulation or timing analysis after compilation is required to determine the final worst-case performance.

Figure 14. FLEX 8000 Timing Model

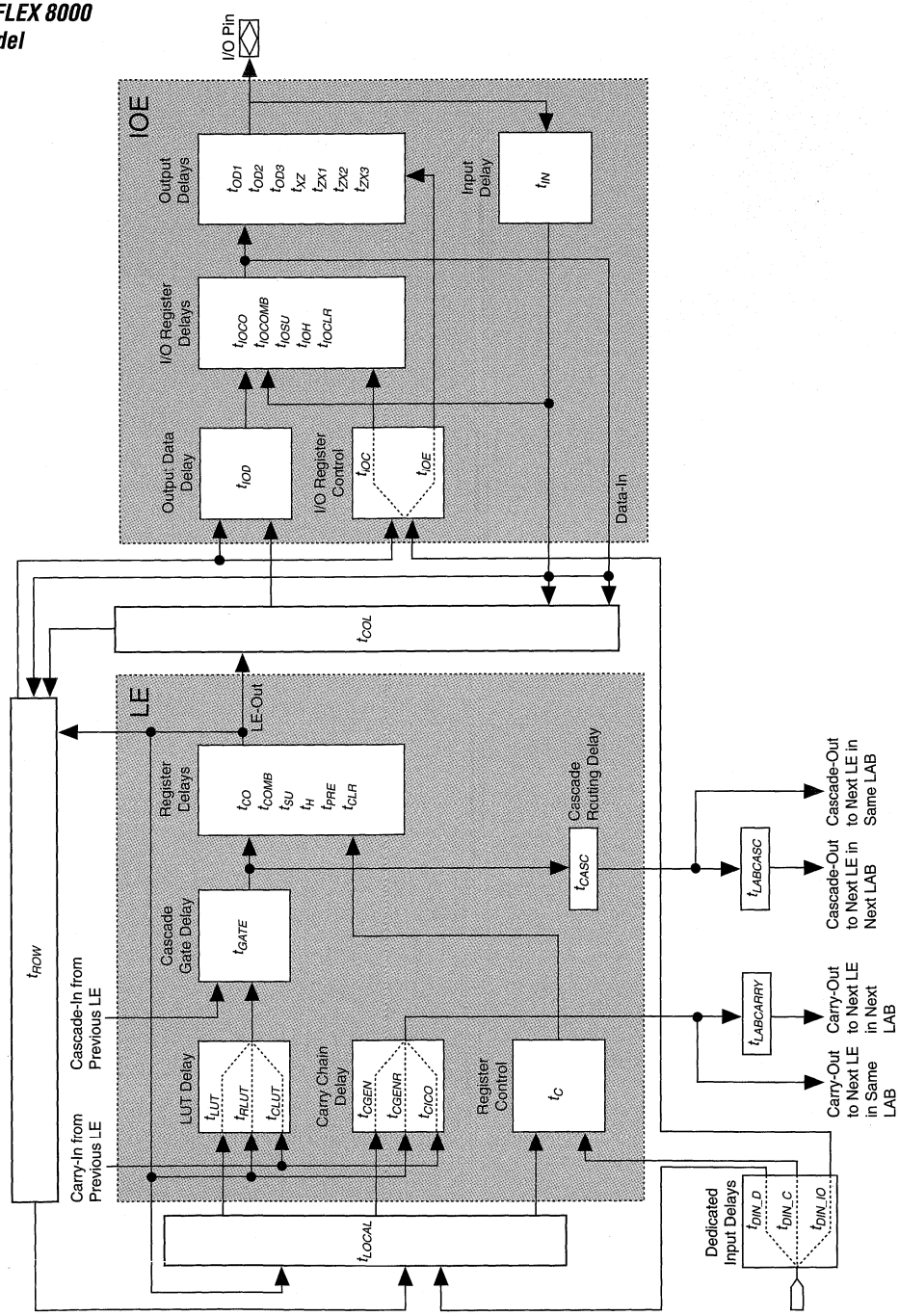


Table 9 summarizes the interconnect paths shown in Figure 14.

Table 9. FLEX 8000 Timing Model Interconnect Paths

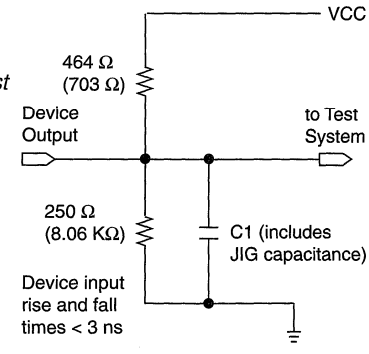
Source	Destination	Total Delay
LE-out	LE in same LAB	t_{LOCAL}
LE-out	LE in same row, different LAB	$t_{ROW} + t_{LOCAL}$
LE-out	LE in different row	$t_{COL} + t_{ROW} + t_{LOCAL}$
LE-out	IOE on column	t_{COL}
LE-out	IOE on row	t_{ROW}
IOE on row	LE in same row	$t_{ROW} + t_{LOCAL}$
IOE on column	Any LE	$t_{COL} + t_{ROW} + t_{LOCAL}$

Generic Testing

Each FLEX 8000 device is functionally tested and guaranteed. Complete testing of each configurable SRAM bit and all logic functionality ensures 100% configuration yield. AC test measurements for FLEX 8000 devices are made under conditions equivalent to those shown in Figure 15. Multiple test patterns can be used to configure devices during all stages of the production flow.

Figure 15. FLEX 8000 AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in parentheses are for 3.3-V devices.



FLEX 8000 5.0-V Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*Note (2)*	–2.0	7.0	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

FLEX 8000 5.0-V Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers		4.75 (4.50)	5.25 (5.50)	V
V_{CCIO}	Supply voltage for output buffers, 5.0-V operation	*Note (3)*	4.75 (4.50)	5.25 (5.50)	V
	Supply voltage for output buffers, 3.3-V operation		3.00	3.60	V
V_I	Input voltage		0	V_{CCINT}	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

FLEX 8000 5.0-V Device DC Operating Conditions *Notes (4), (5)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CCINT} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	5.0-V high-level TTL output voltage	I_{OH} = –4 mA DC, V_{CCIO} = 4.75 V	2.4			V
	3.3-V high-level TTL output voltage	I_{OH} = –4 mA DC, V_{CCIO} = 3.00 V	2.4			V
V_{OL}	5.0-V low-level TTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 4.75 V			0.45	V
	3.3-V low-level TTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 3.00 V			0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or GND	–40		40	µA
I_{CC0}	V_{CC} supply current (standby)	V_I = GND, No load		500		µA

FLEX 8000 5.0-V Device Capacitance *Note (6)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF

Notes to tables:

(1) See *Operating Requirements for Altera Devices* in this data book.

(2) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.

(3) Numbers in parentheses are for military- and industrial-temperature-range versions.

(4) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.

(5) Operating conditions:
V_{CCINT} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CCINT} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CCINT} = 5 V ± 10%, T_A = –55° C to 125° C for military use.

(6) Capacitance is sample-tested only.

FLEX 8000 3.3-V Device Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*Note (2)*	–2.0	7.0	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

FLEX 8000 3.3-V Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	3.0	3.6	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

FLEX 8000 3.3-V Device DC Operating Conditions *Note (2)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level output voltage	I_{OH} = 0.1 mA DC	V_{CC} – 0.2			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC			0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or GND	–40		40	µA
I_{CC0}	V_{CC} supply current (standby)	V_I = GND, No load, *Note (3)*		300		µA

FLEX 8000 3.3-V Device Capacitance *Note (4)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.

(2) Operating conditions:
V_{CCIO} = 3.3 V ± 10% for commercial use.
V_{CCIO} = 3.3 V ± 10% for industrial use.
V_{CCIO} = 3.3 V ± 10% for military use.

(3) Typical values are for T_A = 25° C and V_{CC} = 3.3 V.

(4) Capacitance is sample-tested only.

Figure 16 shows the typical output drive characteristics of 5.0-V FLEX 8000 devices with 5.0-V V_{CCIO}. The output driver is compatible with the PCI local bus specification.

Figure 16. Output Drive Characteristics for 5.0-V Devices, 5.0-V V_{CCIO}

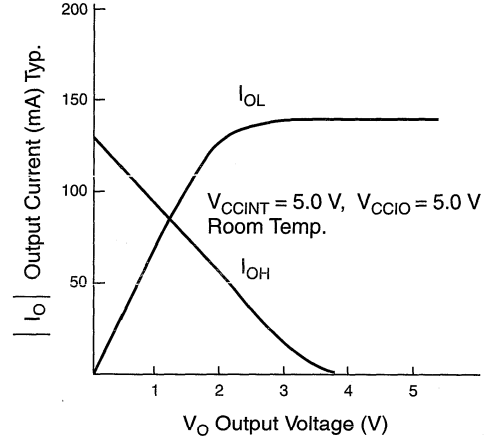


Figure 17 shows the typical output drive characteristics of 5.0-V FLEX 8000 devices with 3.3-V V_{CCIO}. The output driver is compatible with the PCI local bus specification.

Figure 17. Output Drive Characteristics for 5.0-V Devices, 3.3-V V_{CCIO}

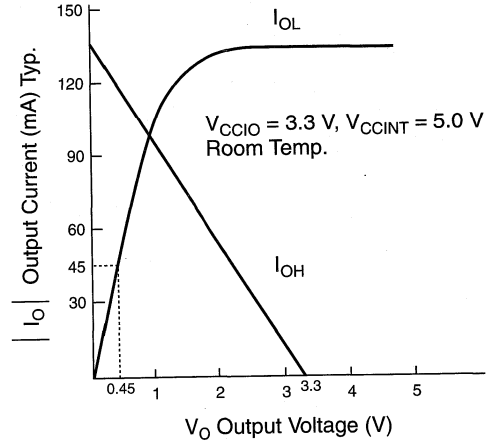
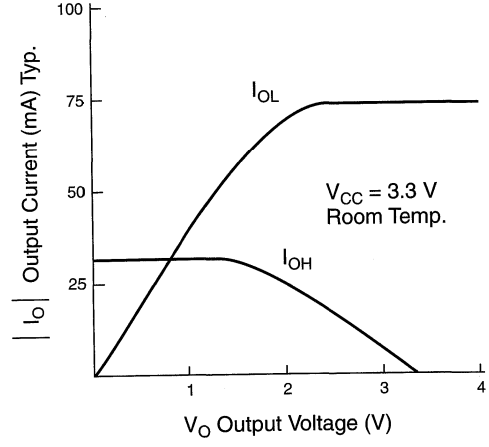


Figure 18 shows the typical output drive characteristics of EPF8282V I/O pins.

Figure 18. EPF8282V Typical Output Drive Characteristics



EPF8282 Internal Timing Parameters *Note (1)*

EPF8282 I/O Element Timing Parameters

Parameter	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		-2 Speed Grade		-3 Speed Grade		
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
t_{IOD}		0.7		0.8		0.9		1.0		2.0	ns
t_{IOC}		1.7		1.8		1.9		1.0		2.0	ns
t_{IOE}		1.7		1.8		1.9		1.0		2.0	ns
t_{IOCO}		1.0		1.0		1.0		1.0		1.0	ns
t_{IOCOMB}		0.3		0.2		0.1		0.0		0.0	ns
t_{IOSU}	1.4		1.6		1.8		2.0		2.0		ns
t_{IOH}	0.0		0.0		0.0		0.0		0.0		ns
t_{IOCLR}		1.2		1.2		1.2		1.3		1.3	ns
t_{IN}		1.5		1.6		1.7		1.8		2.8	ns
t_{OD1}		1.1		1.4		1.7		2.5		3.0	ns
t_{OD2}		1.6		1.9		2.2		–		–	ns
t_{OD3}		4.6		4.9		5.2		6.5		7.0	ns
t_{XZ}		1.4		1.6		1.8		2.5		3.0	ns
t_{ZX1}		1.4		1.6		1.8		2.5		3.0	ns
t_{ZX2}		1.9		2.1		2.3		–		–	ns
t_{ZX3}		4.9		5.1		5.3		6.5		7.0	ns

EPF8282 Interconnect Timing Parameters

Parameter	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		-2 Speed Grade		-3 Speed Grade		
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
$t_{LABCASC}$		0.3		0.3		0.4		0.5		0.9	ns
$t_{LABCARRY}$		0.3		0.3		0.4		0.5		0.6	ns
t_{LOCAL}		0.5		0.6		0.8		1.0		1.0	ns
t_{ROW}		4.2		4.2		4.2		4.2		4.2	ns
t_{COL}		2.5		2.5		2.5		2.5		2.5	ns
t_{DIN_C}		5.0		5.0		5.5		6.0		7.0	ns
t_{DIN_D}		7.2		7.2		7.2		7.2		8.2	ns
t_{DIN_IO}		5.0		5.0		5.5		7.0		8.0	ns

EPF8282 Logic Element Timing Parameters											
Parameter	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		-2 Speed Grade		-3 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{LUT}		2.0		2.5		3.2		4.1		5.1	ns
t_{CLUT}		0.0		0.0		0.0		0.2		1.0	ns
t_{RLUT}		0.9		1.1		1.5		1.9		3.4	ns
t_{GATE}		0.0		0.0		0.0		0.0		0.0	ns
t_{CASC}		0.6		0.7		0.9		1.1		2.0	ns
t_{CICO}		0.4		0.5		0.6		0.7		1.1	ns
t_{CGEN}		0.4		0.5		0.7		0.7		1.4	ns
t_{CGENR}		0.9		1.1		1.5		1.7		2.4	ns
t_{C}		1.6		2.0		2.5		2.8		3.1	ns
t_{CH}	1.7		1.7		2.7		3.5		4.3		ns
t_{CL}	1.7		1.7		2.7		3.5		4.3		ns
t_{CO}		0.4		0.5		0.6		0.4		0.9	ns
t_{COMB}		0.4		0.5		0.6		0.4		0.9	ns
t_{SU}	0.8		1.1		1.2		1.5		1.7		ns
t_{H}	0.9		1.1		1.5		2.3		4.0		ns
t_{PRE}		0.6		0.7		0.8		0.7		1.2	ns
t_{CLR}		0.6		0.7		0.8		0.7		1.2	ns

EPF8282 External Reference Timing Characteristics *Note (1)*

Parameter	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		-2 Speed Grade		-3 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{DRR}		15.8		19.8		24.8		29.3		35.5	ns

Note:
(1) Internal and external timing parameters for EPF8282A devices are preliminary.

EPF8282V Internal Timing Parameters

EPF8282V I/O Element Timing Parameters					
Parameter	-3 Speed Grade		-4 Speed Grade		
	Min	Max	Min	Max	Unit
t_{IOD}		2.2		3.5	ns
t_{IOC}		2.0		3.4	ns
t_{IOE}		2.0		3.4	ns
t_{IOCO}		2.0		3.0	ns
t_{IOCOMB}		0.0		0.0	ns
t_{IOSU}	2.8		4.7		ns
t_{IOH}	0.2		0.1		ns
t_{IOCLR}		2.3		3.5	ns
t_{IN}		3.4		5.4	ns
t_{OD1}		4.1		5.6	ns
t_{OD2}		–		–	ns
t_{OD3}		7.1		9.6	ns
t_{XZ}		4.3		6.7	ns
t_{ZX1}		4.3		6.7	ns
t_{ZX2}		–			ns
t_{ZX3}		8.3			ns

EPF8282V Interconnect Timing Parameters					
Parameter	-3 Speed Grade		-4 Speed Grade		
	Max	Min	Min	Max	Unit
$t_{LABCASC}$		1.3		2.0	ns
$t_{LABCARRY}$		0.8		1.2	ns
t_{LOCAL}		1.5		1.5	ns
t_{ROW}		6.3		6.3	ns
t_{COL}		3.8		3.8	ns
t_{DIN_C}		8.0		10.3	ns
t_{DIN_D}		10.8		12.3	ns
t_{DIN_IO}		9.0		12.3	ns

EPF8282V Logic Element Timing Parameters					
Parameter	-3 Speed Grade		-4 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Unit**
t_{LUT}		7.3		14.3	ns
t_{CLUT}		1.4		1.3	ns
t_{RLUT}		5.1		7.3	ns
t_{GATE}		0.0		0.0	ns
t_{CASC}		2.8		4.2	ns
t_{CICO}		1.5		2.2	ns
t_{CGEN}		2.2		4.5	ns
t_{CGENR}		3.7		6.0	ns
t_{C}		4.7		9.5	ns
t_{CH}		6.0		10.5	ns
t_{CL}		6.0		10.5	ns
t_{CO}		0.9		0.9	ns
t_{COMB}		0.9		0.9	ns
t_{SU}	2.4		4.4		ns
t_{H}	4.6		6.8		ns
t_{PRE}		1.3		1.6	ns
t_{CLR}		1.3		1.6	ns

EPF8282V External Reference Timing Characteristics

Parameter	-3 Speed Grade		-4 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Unit**
t_{DRR}		50.1		80.4	ns

EPF8452 Internal Timing Parameters *Note (1)*

EPF8452 I/O Element Timing Parameters													
Parameter	A-3 Speed Grade		A-4 Speed Grade		A-5 Speed Grade		A-6 Speed Grade		-2 Speed Grade		-3 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IOD}		0.8		0.9		1.0		2.0		1.0		2.0	ns
t_{IOC}		1.8		1.9		2.0		2.0		1.0		2.0	ns
t_{IOE}		1.8		1.9		2.0		2.0		1.0		2.0	ns
t_{IOCO}		1.0		1.0		1.0		1.0		1.0		1.0	ns
t_{IOCOMB}		0.2		0.1		0.0		0.0		0.0		0.0	ns
t_{IOSU}	1.6		1.8		2.0		2.0		2.0		2.0		ns
t_{IOH}	0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{IOCLR}		1.2		1.2		1.2		1.2		1.2		1.2	ns
t_{IN}		1.6		1.7		1.8		2.8		1.8		2.8	ns
t_{OD1}		1.4		1.7		2.0		2.0		2.0		2.0	ns
t_{OD2}		1.9		2.2		2.5		3.0		3.0		3.0	ns
t_{OD3}		4.9		5.2		5.5		6.0		6.0		6.0	ns
t_{XZ}		1.6		1.8		2.0		2.0		2.0		2.0	ns
t_{ZX1}		1.6		1.8		2.0		2.0		2.0		2.0	ns
t_{ZX2}		2.1		2.3		2.5		3.0		3.0		3.0	ns
t_{ZX3}		5.1		5.3		5.5		6.0		6.0		6.0	ns

EPF8452 Interconnect Timing Parameters													
Parameter	A-3 Speed Grade		A-4 Speed Grade		A-5 Speed Grade		A-6 Speed Grade		-2 Speed Grade		-3 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
$t_{LABCASC}$		0.4		0.4		0.5		0.9		0.5		0.9	ns
$t_{LABCARRY}$		0.4		0.4		0.5		0.6		0.5		0.6	ns
t_{LOCAL}		0.5		0.7		0.9		1.0		1.0		1.0	ns
t_{ROW}		5.0		5.0		5.0		5.0		5.0		5.0	ns
t_{COL}		3.0		3.0		3.0		3.0		3.0		3.0	ns
t_{DIN_C}		5.0		5.5		6.0		7.0		6.0		7.0	ns
t_{DIN_D}		7.0		7.5		8.0		9.0		8.0		9.0	ns
t_{DIN_IO}		5.0		5.5		6.0		9.0		8.0		9.0	ns

EPF8452 Logic Element Timing Parameters													
Parameter	A-3 Speed Grade		A-4 Speed Grade		A-5 Speed Grade		A-6 Speed Grade		-2 Speed Grade		-3 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{LUT}		2.3		3.0		3.7		5.1		4.1		5.1	ns
t_{CLUT}		0.2		0.1		0.1		1.0		0.2		1.0	ns
t_{RLUT}		1.6		1.6		1.9		3.4		1.9		3.4	ns
t_{GATE}		0.0		0.0		0.0		0.0		0.0		0.0	ns
t_{CASC}		0.7		0.9		1.1		2.0		1.1		2.0	ns
t_{CICO}		0.5		0.6		0.7		1.1		0.7		1.1	ns
t_{CGEN}		0.9		0.8		0.9		1.4		0.7		1.4	ns
t_{CGENR}		1.4		1.5		1.8		2.4		1.7		2.4	ns
t_{C}		1.8		2.4		2.9		3.1		2.8		3.1	ns
t_{CH}	1.7		2.7		3.4		4.3		3.5		4.3		ns
t_{CL}	1.7		2.7		3.4		4.3		3.5		4.3		ns
t_{CO}		0.5		0.6		0.7		0.9		0.4		0.9	ns
t_{COMB}		0.5		0.6		0.7		0.9		0.4		0.9	ns
t_{SU}	1.0		1.1		1.2		1.7		1.5		1.7		ns
t_{H}	1.1		1.4		1.8		4.0		2.3		4.0		ns
t_{PRE}		0.7		0.8		0.9		1.2		0.7		1.2	ns
t_{CLR}		0.7		0.8		0.9		1.2		0.7		1.2	ns

EPF8452 External Reference Timing Characteristics *Note (1)*

Parameter	A-3 Speed Grade		A-4 Speed Grade		A-5 Speed Grade		A-6 Speed Grade		-2 Speed Grade		-3 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{DRR}		20.0		25.0		30.0		38.2		32.0		38.2	ns

Note:
(1) Internal and external timing parameters for EPF8452A devices are preliminary.

EPF8636A Internal Timing Parameters *Note (1)*

EPF8636A I/O Element Timing Parameters							
Parameter	A-3 Speed Grade		A-4 Speed Grade		A-5 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IOD}		0.8		0.9		1.0	ns
t_{IOC}		1.8		1.9		2.0	ns
t_{IOE}		1.8		1.9		2.0	ns
t_{IOCO}		1.0		1.0		1.0	ns
t_{IOCOMB}		0.2		0.1		0.0	ns
t_{IOSU}	1.6		1.8		2.0		ns
t_{IOH}	0.0		0.0		0.0		ns
t_{IOCLR}		1.2		1.2		1.2	ns
t_{IN}		1.6		1.7		1.8	ns
t_{OD1}		1.4		1.7		2.0	ns
t_{OD2}		1.9		2.2		2.5	ns
t_{OD3}		4.9		5.2		5.5	ns
t_{XZ}		1.6		1.8		2.0	ns
t_{ZX1}		1.6		1.8		2.0	ns
t_{ZX2}		2.1		2.3		2.5	ns
t_{ZX3}		5.1		5.3		5.5	ns

EPF8636A Interconnect Timing Parameters							
Parameter	A-3 Speed Grade		A-4 Speed Grade		A-5 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
$t_{LABCASC}$		0.4		0.4		0.5	ns
$t_{LABCARRY}$		0.4		0.4		0.5	ns
t_{LOCAL}		0.5		0.7		0.9	ns
t_{ROW}		5.0		5.0		5.0	ns
t_{COL}		3.0		3.0		3.0	ns
t_{DIN_C}		5.0		5.5		6.0	ns
t_{DIN_D}		7.0		7.5		8.0	ns
t_{DIN_IO}		5.0		5.5		6.0	ns

EPF8636A Logic Element Timing Parameters							
Parameter	A-3 Speed Grade		A-4 Speed Grade		A-5 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{LUT}		2.3		3.0		3.7	ns
t_{CLUT}		0.2		0.1		0.1	ns
t_{RLUT}		1.6		1.6		1.9	ns
t_{GATE}		0.0		0.0		0.0	ns
t_{CASC}		0.7		0.9		1.1	ns
t_{CICO}		0.5		0.6		0.7	ns
t_{CGEN}		0.9		0.8		0.9	ns
t_{CGENR}		1.4		1.5		1.8	ns
t_{C}		1.8		2.4		2.9	ns
t_{CH}	1.7		2.7		3.4		ns
t_{CL}	1.7		2.7		3.4		ns
t_{CO}		0.5		0.6		0.7	ns
t_{COMB}		0.5		0.6		0.7	ns
t_{SU}	1.0		1.1		1.2		ns
t_{H}	1.1		1.4		1.8		ns
t_{PRE}		0.7		0.8		0.9	ns
t_{CLR}		0.7		0.8		0.9	ns

EPF8636A External Reference Timing Characteristics *Note (1)*

Parameter	A-3 Speed Grade		A-4 Speed Grade		A-5 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{DRR}		20.0		25.0		30.0	ns

Note:
(1) Internal and external timing parameters for EPF8636A devices are preliminary.

EPF8820 Internal Timing Parameters *Note (1)*

EPF8820 I/O Element Timing Parameters											
Parameter	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		-2 Speed Grade		-3 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IOD}		0.7		0.8		0.9		1.0		2.0	ns
t_{IOC}		1.7		1.8		1.9		1.0		2.0	ns
t_{IOE}		1.7		1.8		1.9		1.0		2.0	ns
t_{IOCO}		1.0		1.0		1.0		1.0		1.0	ns
t_{IOCOMB}		0.3		0.2		0.1		0.0		0.0	ns
t_{IOSU}	1.4		1.6		1.8		2.0		2.0		ns
t_{IOH}	0.0		0.0		0.0		0.0		0.0		ns
t_{IOCLR}		1.2		1.2		1.2		1.2		1.2	ns
t_{IN}		1.5		1.6		1.7		1.8		2.8	ns
t_{OD1}		1.1		1.4		1.7		2.0		2.0	ns
t_{OD2}		1.6		1.9		2.2		3.0		3.0	ns
t_{OD3}		4.6		4.9		5.2		6.0		6.0	ns
t_{XZ}		1.4		1.6		1.8		2.0		2.0	ns
t_{ZX1}		1.4		1.6		1.8		2.0		2.0	ns
t_{ZX2}		1.9		2.1		2.3		3.0		3.0	ns
t_{ZX3}		4.9		5.1		5.3		6.0		6.0	ns

EPF8820 Interconnect Timing Parameters											
Parameter	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		-2 Speed Grade		-3 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
$t_{LABCASC}$		0.3		0.3		0.4		0.5		0.9	ns
$t_{LABCARRY}$		0.3		0.3		0.4		0.5		0.6	ns
t_{LOCAL}		0.5		0.6		0.8		1.0		1.0	ns
t_{ROW}		5.0		5.0		5.0		5.0		5.0	ns
t_{COL}		3.0		3.0		3.0		3.0		3.0	ns
t_{DIN_C}		5.0		5.0		5.5		6.0		7.0	ns
t_{DIN_D}		7.0		7.0		7.5		8.0		9.0	ns
t_{DIN_IO}		5.0		5.0		5.5		8.0		9.0	ns

EPF8820 Logic Element Timing Parameters											
Parameter	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		-2 Speed Grade		-3 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{LUT}		2.0		2.5		3.2		4.1		5.1	ns
t_{CLUT}		0.0		0.0		0.0		0.2		1.0	ns
t_{RLUT}		0.9		1.1		1.5		1.9		3.4	ns
t_{GATE}		0.0		0.0		0.0		0.0		0.0	ns
t_{CASC}		0.6		0.7		0.9		1.1		2.0	ns
t_{CICO}		0.4		0.5		0.6		0.7		1.1	ns
t_{CGEN}		0.4		0.5		0.7		0.7		1.4	ns
t_{CGENR}		0.9		1.1		1.5		1.7		2.4	ns
t_{C}		1.6		2.0		2.5		2.8		3.1	ns
t_{CH}	1.7		1.7		2.7		3.5		4.3		ns
t_{CL}	1.7		1.7		2.7		3.5		4.3		ns
t_{CO}		0.4		0.5		0.6		0.4		0.9	ns
t_{COMB}		0.4		0.5		0.6		0.4		0.9	ns
t_{SU}	0.8		1.1		1.2		1.5		1.7		ns
t_{H}	0.9		1.1		1.5		2.3		4.0		ns
t_{PRE}		0.6		0.7		0.8		0.7		1.2	ns
t_{CLR}		0.6		0.7		0.8		0.7		1.2	ns

EPF8820 External Reference Timing Characteristics *Note (1)*

Parameter	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		-2 Speed Grade		-3 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{DRR}		16.0		20.0		25.0		32.0		38.2	ns

Note:
(1) Internal and external timing parameters for EPF8820A devices are preliminary.

EPF81188 Internal Timing Parameters *Note (1)*

EPF81188 I/O Element Timing Parameters															
Parameter	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		A-5 Speed Grade		A-6 Speed Grade		-2 Speed Grade		-3 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IOD}		0.7		0.8		0.9		1.0		2.0		1.0		2.0	ns
t_{IOC}		1.7		1.8		1.9		2.0		2.0		1.0		2.0	ns
t_{IOE}		1.7		1.8		1.9		2.0		2.0		1.0		2.0	ns
t_{IOCO}		1.0		1.0		1.0		1.0		1.0		1.0		1.0	ns
t_{IOCOMB}		0.3		0.2		0.1		0.0		0.0		0.0		0.0	ns
t_{IOSU}	1.4		1.6		1.8		2.0		2.0		2.0		2.0		ns
t_{IOH}	0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{IOCLR}		1.2		1.2		1.2		1.2		1.2		1.2		1.2	ns
t_{IN}		1.5		1.6		1.7		1.8		2.8		1.8		2.8	ns
t_{OD1}		1.1		1.4		1.7		2.0		2.0		2.0		2.0	ns
t_{OD2}		1.6		1.9		2.2		2.5		3.0		3.0		3.0	ns
t_{OD3}		4.6		4.9		5.2		5.5		6.0		6.0		6.0	ns
t_{XZ}		1.4		1.6		1.8		2.0		2.0		2.0		2.0	ns
t_{ZX1}		1.4		1.6		1.8		2.0		2.0		2.0		2.0	ns
t_{ZX2}		1.9		2.1		2.3		2.5		2.5		3.0		3.0	ns
t_{ZX3}		4.9		5.1		5.3		5.5		5.5		6.0		6.0	ns

EPF81188 Interconnect Timing Parameters															
Parameter	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		A-5 Speed Grade		A-6 Speed Grade		-2 Speed Grade		-3 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
$t_{LABCASC}$		0.3		0.3		0.4		0.5		0.9		0.5		0.9	ns
$t_{LABCARRY}$		0.3		0.3		0.4		0.5		0.6		0.5		0.6	ns
t_{LOCAL}		0.5		0.6		0.8		1.0		1.0		1.0		1.0	ns
t_{ROW}		5.0		5.0		5.0		5.0		5.0		5.0		5.0	ns
t_{COL}		3.0		3.0		3.0		3.0		3.0		3.0		3.0	ns
t_{DIN_C}		5.0		5.0		5.5		6.0		7.0		6.0		7.0	ns
t_{DIN_D}		7.0		7.0		7.5		8.0		8.0		8.0		9.0	ns
t_{DIN_IO}		5.0		5.0		5.5		6.0		9.0		8.0		9.0	ns

EPF81188 Logic Element Timing Parameters															
Parameter	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		A-5 Speed Grade		A-6 Speed Grade		-2 Speed Grade		-3 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{LUT}		2.0		2.5		3.2		3.9		5.1		4.1		5.1	ns
t_{CLUT}		0.0		0.0		0.0		0.0		1.0		0.2		1.0	ns
t_{RLUT}		0.9		1.1		1.5		1.8		3.4		1.9		3.4	ns
t_{GATE}		0.0		0.0		0.0		0.0		0.0		0.0		0.0	ns
t_{CASC}		0.6		0.7		0.9		1.1		2.0		1.1		2.0	ns
t_{CICO}		0.4		0.5		0.6		0.7		1.1		0.7		1.1	ns
t_{CGEN}		0.4		0.5		0.7		0.8		1.4		0.7		1.4	ns
t_{CGENR}		0.9		1.1		1.5		1.8		2.4		1.7		2.4	ns
t_{C}		1.6		2.0		2.5		3.0		3.1		2.8		3.1	ns
t_{CH}	1.7		1.7		2.7		3.4		4.3		3.5		4.3		ns
t_{CL}	1.7		1.7		2.7		3.4		4.3		3.5		4.3		ns
t_{CO}		0.4		0.5		0.6		0.7		0.9		0.4		0.9	ns
t_{COMB}		0.4		0.5		0.6		0.7		0.9		0.4		0.9	ns
t_{SU}	0.8		1.1		1.2		1.3		1.7		1.5		1.7		ns
t_{H}	0.9		1.1		1.5		1.9		4.0		2.3		4.0		ns
t_{PRE}		0.6		0.7		0.8		0.9		1.2		0.7		1.2	ns
t_{CLR}		0.6		0.7		0.8		0.9		1.2		0.7		1.2	ns

EPF81188 External Reference Timing Characteristics *Note (1)*

Parameter	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		A-5 Speed Grade		A-6 Speed Grade		-2 Speed Grade		-3 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{DRR}		16.0		20.0		25.0		30.0		38.2		32.0		38.2	ns

Note:
(1) Internal and external timing parameters for EPF81188A devices are preliminary.

EPF81500 Internal Timing Parameters *Note (1)*

EPF81500 I/O Element Timing Parameters

Parameter	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		-2 Speed Grade		-3 Speed Grade		
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
t_{IOD}		0.7		0.8		0.9		1.0		2.0	ns
t_{IOC}		1.7		1.8		1.9		1.0		2.0	ns
t_{IOE}		1.7		1.8		1.9		1.0		2.0	ns
t_{IOCO}		1.0		1.0		1.0		1.0		1.0	ns
t_{IOCOMB}		0.3		0.2		0.1		0.0		0.0	ns
t_{IOSU}	1.4		1.6		1.8		2.0		2.0		ns
t_{IOH}	0.0		0.0		0.0		0.0		0.0		ns
t_{IOCLR}		1.2		1.2		1.2		1.2		1.2	ns
t_{IN}		1.5		1.6		1.7		1.8		1.8	ns
t_{OD1}		1.1		1.4		1.7		2.0		2.0	ns
t_{OD2}		1.6		1.9		2.2		3.0		3.0	ns
t_{OD3}		4.6		4.9		5.2		6.0		6.0	ns
t_{XZ}		1.4		1.6		1.8		2.0		2.0	ns
t_{ZX1}		1.4		1.6		1.8		2.0		2.0	ns
t_{ZX2}		1.9		2.1		2.3		3.0		3.0	ns
t_{ZX3}		4.9		5.1		5.3		6.0		6.0	ns

EPF81500 Interconnect Timing Parameters

Parameter	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		-2 Speed Grade		-3 Speed Grade		
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
$t_{LABCASC}$		0.3		0.3		0.4		0.5		0.9	ns
$t_{LABCARRY}$		0.3		0.3		0.4		0.5		0.6	ns
t_{LOCAL}		0.5		0.6		0.8		1.0		1.0	ns
t_{ROW}		6.2		6.2		6.2		6.2		6.2	ns
t_{COL}		3.0		3.0		3.0		3.0		3.0	ns
t_{DIN_C}		5.0		5.0		5.5		6.0		7.0	ns
t_{DIN_D}		8.2		8.2		8.7		9.2		10.20	ns
t_{DIN_IO}		5.0		5.0		5.5		8.0		9.0	ns

EPF81500 Logic Element Timing Parameters											
Parameter	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		-2 Speed Grade		-3 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{LUT}		2.0		2.5		3.2		4.1		5.1	ns
t_{CLUT}		0.0		0.0		0.0		0.2		1.0	ns
t_{RLUT}		0.9		1.1		1.5		1.9		3.4	ns
t_{GATE}		0.0		0.0		0.0		0.0		0.0	ns
t_{CASC}		0.6		0.7		0.9		1.1		2.0	ns
t_{CICO}		0.4		0.5		0.6		0.7		1.1	ns
t_{CGEN}		0.4		0.5		0.7		0.7		1.4	ns
t_{CGENR}		0.9		1.1		1.5		1.7		2.4	ns
t_{C}		1.6		2.0		2.5		2.8		3.1	ns
t_{CH}	1.7		1.7		2.7		3.5		4.3		ns
t_{CL}	1.7		1.7		2.7		3.5		4.3		ns
t_{CO}		0.4		0.5		0.6		0.4		0.9	ns
t_{COMB}		0.4		0.5		0.6		0.4		0.9	ns
t_{SU}	0.8		1.1		1.2		1.5		1.7		ns
t_{H}	0.9		1.1		1.5		2.3		4.0		ns
t_{PRE}		0.6		0.7		0.8		0.7		1.2	ns
t_{CLR}		0.6		0.7		0.8		0.7		1.2	ns

EPF81500 External Reference Timing Characteristics *Note (1)*

Parameter	A-2 Speed Grade		A-3 Speed Grade		A-4 Speed Grade		-2 Speed Grade		-3 Speed Grade		
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{DRR}		16.1		20.1		25.1		34.0		40.2	ns

Note:
(1) Internal and external timing parameters for EPF81500A devices are preliminary.

Calculating the Supply Current

The V_{CC} supply current for FLEX 8000 devices, I_{CC}, can be calculated with the following equation:

$$I_{CC} = I_{CCSTANDBY} + I_{CCOUTPUT} + I_{CCACTIVE}$$

Typical $I_{CCSTANDBY}$ values are shown as I_{CC0} in the "FLEX 8000 5.0-V Device DC Operating Conditions" and "FLEX 8000 3.3-V Device DC Operating Conditions" tables earlier in this data sheet. The $I_{CCOUTPUT}$ value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Operating Requirements for Altera Devices* in this data book. The $I_{CCACTIVE}$ value depends on the switching frequency and the application logic. This value can be calculated based on the amount of current that each LE typically consumes

The following equation shows the general formula for calculating $I_{CCACTIVE}$:

$$I_{CCACTIVE} = K \times F \times N \times 0.125 \times \frac{\mu A}{MHz \times LE}$$

In this equation, F is the maximum operating frequency in MHz; N is the number of LEs used in the device. The total is multiplied by 0.125, which is based on a 16-bit counter in which 2 out of 16 (12.5%) of the output bits switch on each Clock edge.

Table 10 shows the value of the constant (K) for FLEX 8000 devices.

Table 10. Current Consumed per LE

Device	K
5.0-V FLEX 8000 devices	75
3.3-V FLEX 8000 devices	60
5.0-V FLEX 8000A devices	75 *Note (1)*

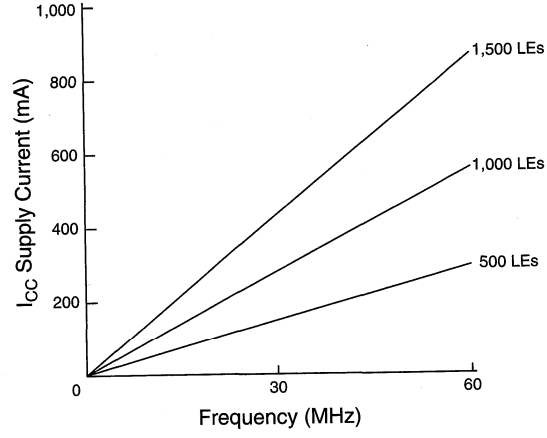
Note:
(1) This information is preliminary.

Figure 19 shows the relationship between I_{CC} and operating frequency for several LE utilization values.

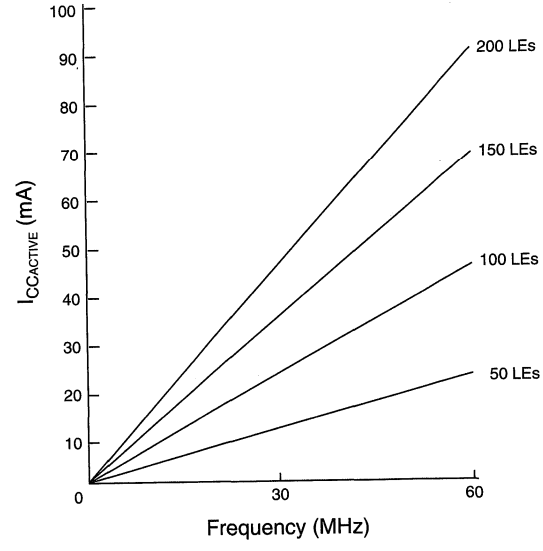
Figure 19. FLEX 8000 $I_{CCACTIVE}$ vs. Operating Frequency

5.0-V FLEX 8000 Devices & 5.0-V FLEX 8000A Devices

Information on 5.0-V FLEX 8000A devices is preliminary.



3.3-V FLEX 8000 Devices



Configuration & Operation

The FLEX 8000 architecture supports several configuration schemes to load a design into the device(s) on the circuit board. This data sheet summarizes the device operating modes and available device configuration schemes.

Go to *Application Note 33 (Configuring FLEX 8000 Devices)* and *Application Note 38 (Configuring Multiple FLEX 8000 Devices)* for detailed descriptions of device configuration options; device configuration pins; and information on configuring FLEX 8000 devices, including sample schematics, timing diagrams, and configuration parameters.

Operating Modes

The FLEX 8000 architecture uses SRAM elements that requires configuration data to be loaded whenever the device powers up and begins operation. The process of physically loading the SRAM programming data into the device is called *configuration*. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The configuration and initialization processes together are called *command mode*; normal device operation is called *user mode*.

SRAM elements allow FLEX 8000 devices to be reconfigured in-circuit with new programming data that is loaded into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different programming data, reinitializing the device, and resuming user-mode operation. The entire reconfiguration process requires less than 100 ms and can be used to dynamically reconfigure an entire system. In-field upgrades can be performed by distributing new configuration files.

Configuration Schemes

The configuration data for a FLEX 8000 device can be loaded with one of six configuration schemes, chosen on the basis of the target application. Both active and passive schemes are available. In the active configuration schemes, the FLEX 8000 device functions as the controller, directing the loading operation, controlling external EPROM devices, and completing the loading process. The Clock source for all active configuration schemes is an oscillator on the FLEX 8000 device that operates between 2 MHz and 6 MHz. In the passive configuration schemes, an external controller guides the FLEX 8000 device, which operates as a slave. Table 11 shows the source of data for each of the six configuration schemes.

Table 11. Configuration Schemes

Configuration Scheme	Acronym	Data Source
Active serial	AS	Altera Configuration EPROM
Active parallel up	APU	Parallel EPROM
Active parallel down	APD	Parallel EPROM
Passive serial	PS	Serial data path
Passive parallel synchronous	PPS	Intelligent host
Passive parallel asynchronous	PPA	Intelligent host

Device Pin-Outs

Tables 12 through 14 show the pin names and numbers for the dedicated pins in each FLEX 8000 device package.

Table 12. FLEX 8000 84-, 100- & 160-Pin Package Pin-Outs (Part 1 of 2)

Pin Name	84-Pin PLCC EPF8452 EPF8452A EPF8636A	84-Pin PLCC EPF8282 EPF8282A	100-Pin TQFP EPF8282 EPF8282A	160-Pin PGA EPF8452 EPF8452A	160-Pin PQFP EPF8820A *Note (1)*	160-Pin PQFP EPF8452 EPF8452A
nSP *(1)*	75	75	75	R1	1	120
MSEL0 *(1)*	74	74	74	P2	2	117
MSEL1 *(1)*	53	53	51	A1	44	84
nSTATUS *(1)*	32	32	24	C13	82	37
nCONFIG *(1)*	33	33	25	A15	81	40
DCLK *(1)*	10	10	100	P14	125	1
CONF_DONE *(1)*	11	11	1	N13	124	4
nWS	30	30	22	F13	87	30
nRS	48	48	42	C6	89	71
RDCLK	49	49	45	B5	110	73
nCS	29	29	21	D15	118	29
CS	28	28	19	E15	121	27
RDYnBUSY	77	77	77	P3	100	125
CLKUSR	50	50	47	C5	107	76
ADD17	51	51	49	B4	40	78
ADD16	55	36	28	E2	39	91
ADD15	56	56	55	D1	38	92
ADD14	57	57	57	E1	37	94
ADD13	58	58	58	F3	36	95
ADD12	60	60	59	F2	32	96
ADD11	61	61	60	F1	30	97
ADD10	62	62	61	G2	28	98
ADD9	63	63	62	G1	26	99
ADD8	64	64	64	H1	22	101
ADD7	65	65	65	H2	20	102
ADD6	66	66	66	J1	18	103
ADD5	67	67	67	J2	16	104
ADD4	69	69	68	K2	11	105
ADD3	70	70	69	K1	10	106
ADD2	71	71	71	K3	8	109
ADD1	72	76	76	M1	7	110
ADD0	76	78	78	N3	6	123
DATA7	2	3	90	P8	140	144
DATA6	4	4	91	P10	139	150

Table 12. FLEX 8000 84-, 100- & 160-Pin Package Pin-Outs (Part 2 of 2)

Pin Name	84-Pin PLCC EPF8452 EPF8452A EPF8636A	84-Pin PLCC EPF8282 EPF8282A	100-Pin TQFP EPF8282 EPF8282A	160-Pin PGA EPF8452 EPF8452A	160-Pin PQFP EPF8820A *Note (1)*	160-Pin PQFP EPF8452 EPF8452A
DATA5	6	6	92	R12	138	152
DATA4	7	7	95	R13	136	154
DATA3	8	8	97	P13	135	157
DATA2	9	9	99	R14	133	159
DATA1	13	13	4	N15	132	11
DATA0	14	14	5	K13	129	12
TDI *(2)*	45 *(3)*	55	54	–	17	–
TDO *(2)*	27 *(3)*	27	18	–	102	–
TCLK *(2)*	44 *(3)*	72	72	–	27	–
TMS *(2)*	43 *(3)*	20	11	–	29	–
nTRST *(1)*	52 *(4)*	52	50	–	45	–
Dedicated Inputs	12, 31, 54, 73	12, 31, 54, 73	3, 23, 53, 73	C3, D14, N2, R15	14, 33, 94, 113	5, 36, 85, 116
VCCINT	17, 38, 59, 80	17, 38, 59, 80	6, 20, 37, 56, 70, 87	B2, C4, D3, D8, D12, G3, G12, H4, H13, J3, J12, M4, M7, M9, M13, N12	3, 24, 46, 92, 114, 160	21, 41, 53, 67, 80, 81, 100, 121, 133, 147, 160
VCCIO	–	–	–	–	23, 47, 57, 69, 79, 104, 127, 137, 149, 159	–
GND	5, 26, 47, 68	5, 26, 47, 68	2, 13, 30, 44, 52, 63, 80, 94	C12, D4, D7, D9, D13, G4, G13, H3, H12, J4, J13, L1, M3, M8, M12, M15, N4	12, 13, 34, 35, 51, 63, 75, 80, 83, 93, 103, 115, 126, 131, 143, 155	13, 14, 28, 46, 60, 75, 93, 107, 108, 126, 140, 155
No Connect (N.C.)	–	–	–	–	–	2, 3, 38, 39, 70, 82, 83, 118, 119, 148
Total User I/O Pins	64	64	74	116	116	116

Table 13. FLEX 8000 160-, 192-, 208- & 225-Pin Package Pin-Outs (Part 1 of 3)

Pin Name	160-Pin PQFP EPF8636A *Note (1)*	192-Pin PGA EPF8636A EPF8820 EPF8820A	208-Pin RQFP EPF8636A	208-Pin RQFP EPF8820 EPF8820A	208-Pin PQFP EPF81188A *Note (1)*	225-Pin BGA EPF8820 EPF8820A
nSP *(1)*	1	R15	207	207	5	A15
MSEL0 *(1)*	3	T15	4	4	21	B14
MSEL1 *(1)*	38	T3	49	49	33	R15
nSTATUS *(1)*	83	B3	108	108	124	P2
nCONFIG *(1)*	81	C3	103	103	107	R1
DCLK *(1)*	120	C15	158	158	154	B2
CONF_DONE *(1)*	118	B15	153	153	138	A1
nWS	89	C5	114	114	118	L4
nRS	50	B5	66	116	121	K5
RDCLK	48	C11	64	137	137	F1
nCS	91	B13	116	145	142	D1
CS	93	A16	118	148	144	C1
RDYnBUSY	155	A8	201	127	128	J3
CLKUSR	44	A10	59	134	134	G2
ADD17	43	R5	57	43	46	M14
ADD16	33	U3	43	42	45	L12
ADD15	31	T5	41	41	44	M15
ADD14	29	U4	39	40	39	L13
ADD13	27	R6	37	39	37	L14
ADD12	24	T6	31	35	36	K13
ADD11	23	R7	30	33	31	K15
ADD10	22	T7	29	31	30	J13
ADD9	21	T8	28	29	29	J15
ADD8	20	U9	24	25	26	G14
ADD7	19	U10	23	23	25	G13
ADD6	18	U11	22	21	24	G11
ADD5	17	U12	21	19	18	F14
ADD4	13	R12	14	14	17	E13
ADD3	11	U14	12	13	16	D15
ADD2	9	U15	10	11	10	D14
ADD1	7	R13	8	10	9	E12
ADD0	157	U16	203	9	8	C15
DATA7	137	H17	178	178	177	A7
DATA6	132	G17	172	176	175	D7

Table 13. FLEX 8000 160-, 192-, 208- & 225-Pin Package Pin-Outs (Part 2 of 3)

Pin Name	160-Pin PQFP EPF8636A *Note (1)*	192-Pin PGA EPF8636A EPF8820 EPF8820A	208-Pin RQFP EPF8636A	208-Pin RQFP EPF8820 EPF8820A	208-Pin PQFP EPF81188A *Note (1)*	225-Pin BGA EPF8820 EPF8820A
DATA5	129	F17	169	174	172	A6
DATA4	127	E17	165	172	170	A5
DATA3	124	G15	162	171	168	B5
DATA2	122	F15	160	167	166	E6
DATA1	115	E16	149	165	163	D5
DATA0	113	C16	147	162	161	C4
TDI *(2)*	55	R11	72	20	–	F15
TDO *(2)*	95	B9	120	129	–	J2
TCLK *(2)*	57	U8	74	30	–	J14
TMS *(2)*	59	U7	76	32	–	J12
nTRST *(1)*	40	R3	54	54	–	P14
Dedicated Inputs	6, 35, 87, 116	A5, U5, U13, A13	7, 45, 112, 150	17, 36, 121, 140	13, 41, 116, 146	F4, L1, K12, E15
VCCINT (5.0 V)	4, 5, 26, 85, 106	C8, C9, C10, R8, R9, R10, R14	5, 6, 33, 110, 137,	5, 6, 27, 48, 119, 141	4, 20, 35, 48, 50, 102, 114, 131, 147	F5, F10, E1, L2, K4, M12, P15, H13, H14, B15, C13
VCCIO (5.0 V or 3.3 V)	25, 41, 60, 70, 80, 107, 121, 140, 149, 160	D3, D4, D9, D14, D15, G4, G14, L4, L14, P4, P9, P14	32, 55, 78, 91, 102, 138, 159, 182, 193, 206	26, 55, 69, 87, 102, 131, 159, 173, 191, 206	3, 19, 34, 49, 69, 87, 106, 123, 140, 156, 174, 192	H3, H2, P6, R6, P10, N10, R14, N13, H15, H12, D12, A14, B10, A10, B6, C6, A2, C3, M4, R2

Table 13. FLEX 8000 160-, 192-, 208- & 225-Pin Package Pin-Outs (Part 3 of 3)

Pin Name	160-Pin PQFP EPF8636A *Note (1)*	192-Pin PGA EPF8636A EPF8820 EPF8820A	208-Pin RQFP EPF8636A	208-Pin RQFP EPF8820 EPF8820A	208-Pin PQFP EPF81188A *Note (1)*	225-Pin BGA EPF8820 EPF8820A
GND	15, 16, 36, 37, 45, 51, 75, 84, 86, 96, 97, 117, 126, 131, 154	C4, D7, D8, D10, D11, H4, H14, K4, K14, P7, P8, P10, P11	19, 20, 46, 47, 60, 67, 96, 109, 111, 124, 125, 151, 164, 171, 200	15, 16, 37, 38, 60, 78, 96, 109, 110, 120, 130, 142, 152, 164, 182, 200	11, 12, 27, 28, 42, 43, 60, 78, 96, 105, 115, 122, 132, 139, 148, 155, 159, 165, 183, 201	B1, D4, E14, F7, F8, F9, F12, G6, G7, G8, G9, G10, H1, H4, H5, H6, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, K6, K7, K8, K9, K11, L15, N3, P1
No Connect (N.C.)	2, 39, 82, 119	C6, C12, C13, C14, E3, E15, F3, J3, J4, J14, J15, N3, N15, P3, P15, R4, *Note (6)*	1, 2, 3, 16, 17, 18, 25, 26, 27, 34, 35, 36, 50, 51, 52, 53, 104, 105, 106, 107, 121, 122, 123, 130, 131, 132, 139, 140, 141, 154, 155, 156, 157, 208	1, 2, 3, 50, 51, 52, 53, 104, 105, 106, 107, 154, 155, 156, 157, 208	1, 2, 51, 52, 53, 54, 103, 104, 157, 158, 207, 208	–
Total User I/O Pins	114	132, *Note (7)*	132	148	144	148

Table 14. FLEX 8000 232-, 240-, 280 & 304-Pin Package Pin-Outs (Part 1 of 3)

Pin Name	232-Pin PGA EPF81188 EPF81188A	240-Pin QFP EPF81188 EPF81188A	240-Pin RQFP EPF81500A	280-Pin PGA EPF81500A	304-Pin RQFP EPF81500 EPF81500A
nSP *(1)*	C14	237	237	W1	304
MSEL0 *(1)*	G15	21	19	N1	26
MSEL1 *(1)*	L15	40	38	H3	51
nSTATUS *(1)*	L3	141	142	G19	178
nCONFIG *(1)*	R4	117	120	B18	152
CONF_DONE *(1)*	G3	160	161	M16	204
DCLK *(1)*	C4	184	183	U18	230
nWS	P1	133	134	F18	167
nRS	N1	137	138	G18	171
RDCLK	G2	158	159	M17	202
nCS	E2	166	167	N16	212
CS	E3	169	170	N18	215
RDYnBUSY	K2	146	147	J17	183
CLKUSR	H2	155	156	K19	199
ADD17	R15	58	56	E3	73
ADD16	T17	56	54	E2	71
ADD15	P15	54	52	F4	69
ADD14	M14	47	45	G1	60
ADD13	M15	45	43	H2	58
ADD12	M16	43	41	H1	56
ADD11	K15	36	34	J3	47
ADD10	K17	34	32	K3	45
ADD9	J14	32	30	K4	43
ADD8	J15	29	27	L1	34
ADD7	H17	27	25	L2	32
ADD6	H15	25	23	M1	30
ADD5	F16	18	16	N2	20
ADD4	F15	16	14	N3	18
ADD3	F14	14	12	N4	16
ADD2	D15	7	5	U1	8
ADD1	B17	5	3	U2	6
ADD0	C15	3	1	V1	4
DATA7	A7	205	199	W13	254
DATA6	D8	203	197	W14	252
DATA5	B7	200	196	W15	250

Table 14. FLEX 8000 232-, 240-, 280 & 304-Pin Package Pin-Outs (Part 2 of 3)

Pin Name	232-Pin PGA EPF81188 EPF81188A	240-Pin QFP EPF81188 EPF81188A	240-Pin RQFP EPF81500A	280-Pin PGA EPF81500A	304-Pin RQFP EPF81500 EPF81500A
DATA4	C7	198	194	W16	248
DATA3	D7	196	193	W17	246
DATA2	B5	194	190	V16	243
DATA1	A3	191	189	U16	241
DATA0	A2	189	187	V17	239
TDI *(8)*	–	–	63	B1	80
TDO *(8)*	–	–	117	C17	149
TCLK *(8)*	–	–	116	A19	148
TMS *(8)*	–	–	64	C2	81
nTRST *(8)*	–	–	115	A18	145
Dedicated Inputs	C1, C17, R1, R17	10, 51, 130, 171	8, 49, 131, 172	F1, F16, P3, P19	12, 64, 164, 217
VCCINT (5.0 V)	E4, H4, L4, P12, L14, H14, E14, R14, U1	20, 42, 64, 66, 114, 128, 150, 172, 236	18, 40, 60, 62, 91, 114, 129, 151, 173, 209	B17, D3, D15, E8, E10, E12, E14, R7, R9, R11, R13, R14, T14	24, 54, 77, 144, 79, 115, 162, 191, 218, 266, 301
VCCIO (5.0 V or 3.3 V)	N10, M13, M5, K13, K5, H13, H5, F5, E10, E8, N8, F13	19, 41, 65, 81, 99, 116, 140, 162, 186, 202, 220, 235	17, 39, 61, 78, 94, 108, 130, 152, 174, 191, 205, 221, 235	D14, E7, E9, E11, E13, R6, R8, R10, R12, T13, T15	22, 53, 78, 99, 119, 137, 163, 193, 220, 244, 262, 282, 300
GND	A1, D6, E11, E7, E9, G4, G5, G13, G14, J5, J13, K4, K14, L5, L13, N4, N7, N9, N11, N14	8, 9, 30, 31, 52, 53, 72, 90, 108, 115, 129, 139, 151, 161, 173, 185, 187, 193, 211, 229	6, 7, 28, 29, 50, 51, 71, 95, 101, 118, 119, 140, 141, 162, 163, 184, 185, 186, 198, 208, 228	D4, D5, D16, E4, E5, E6, E15, E16, F5, F15, G5, G15, H5, H15, J5, J15, K5, K15, L5, L15, M5, M15, N5, N15, P4, P5, P15, P16, R4, R5, R15, R16, T4, T5, T16, U17	9, 11, 36, 38, 65, 67, 90, 108, 116, 128, 150, 151, 175, 177, 206, 208, 231, 232, 237, 253, 265, 273, 291

Table 14. FLEX 8000 232-, 240-, 280 & 304-Pin Package Pin-Outs (Part 3 of 3)

Pin Name	232-Pin PGA EPF81188 EPF81188A	240-Pin QFP EPF81188 EPF81188A	240-Pin RQFP EPF81500A	280-Pin PGA EPF81500A	304-Pin RQFP EPF81500 EPF81500A
No Connect (N.C.)	–	61, 62, 119, 120, 181, 182, 239, 240	–	–	10, 21, 23, 25, 35, 37, 39, 40, 41, 42, 52, 55, 66, 68, 146, 147, 161, 173, 174, 176, 187, 188, 189, 190, 192, 194, 195, 205, 207, 219, 221, 233, 234, 235, 236, 302, 303
Total User I/O Pins	180	180	204	204	204

Notes to Tables 12 through 14:

(1) Perform a complete thermal analysis before committing a design to this device package. See *Operating Requirements for Altera Devices* in this data book for more information.
(2) Dedicated pin (not available as a user I/O pin).
(3) If the device is not configured to use the JTAG BST circuitry, this pin is available as a user I/O pin.
(4) Dedicated JTAG pins are available for EPF8636A devices only. No dedicated JTAG pins are available for EPF8452 and EPF8452A devices.
(5) Pin 52 is a V_{CC} pin on EPF8452 and EPF8452A devices only.
(6) These pins are No Connect pins for EPF8636A devices only.
(7) EPF8636A devices have 130 user I/O pins; EPF8820 devices have 148 user I/O pins.
(8) These pins are dedicated JTAG pins and are not available as user I/O pins.

Notes:

EPF8050M

FLEX 8000M Programmable Logic Device

March 1995, ver. 3 | Data Sheet

Features

Preliminary Information

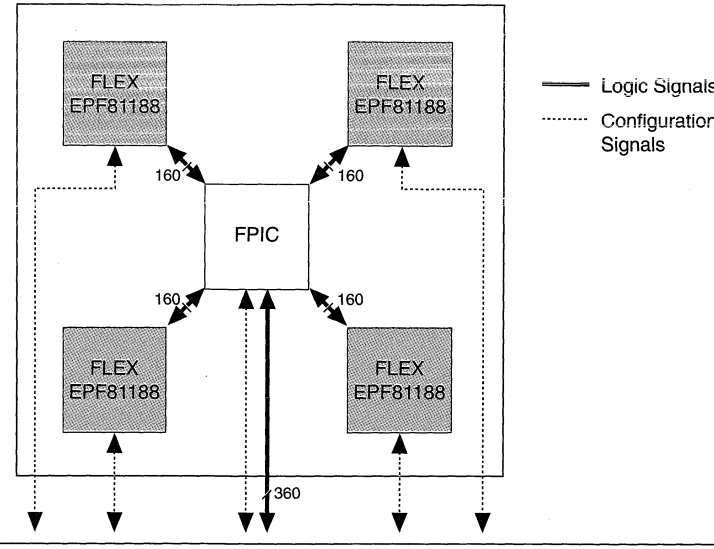
- Ideal for ASIC prototyping
  - Combination of four EPF81188 devices and one Field Programmable InterConnect (FPIC) device
  - 50,000 usable gates
  - 4,656 flipflops
  - 360 user I/O pins
  - Up to 30-MHz in-system operation
- Combination of three innovations
  - FLEX 8000 architecture
  - Programmable interconnect
  - Multi-Chip Module (MCM) packaging
- SRAM-based EPF81188 and FPIC devices
  - In-circuit reconfigurability
  - Incremental reconfiguration of each individual device within the EPF8050M
  - Low standby power
- Available in a 560-pin ceramic pin-grid array (PGA) package
  - 2.26-inch square
  - 50-mil staggered pin pitch
  - On-board decoupling capacitors (3.3 µF total)
  - Separate configuration pins for each EPF81188 and the FPIC device
- Software design support—including automatic partitioning, logic synthesis and place-and-route—with Altera's MAX+PLUS II development system for 486- and Pentium-based PCs and compatible computers, as well as for Sun SPARCstations

Architecture Description

The Altera EPF8050M device combines four EPF81188 devices and one Field Programmable Interconnect (FPIC) device to create a 50,000-gate programmable logic device (PLD). It is available in a 560-pin ceramic PGA package with 360 user I/O pins. The EPF8050M supports all FLEX 8000 architectural features. Figure 1 shows a block diagram for the EPF8050M, including connectivity between the EPF81188 devices and the I/O pins.

All logic signals for the EPF81188 devices are routed via the FPIC, providing a symmetric routing structure within the EPF8050M. The FPIC allows each EPF81188 I/O pin to be routed to any pin on any other EPF81188 device(s), or to any EPF8050M I/O pin. With this routing flexibility, the EPF8050M can be treated as four EPF81188 devices with 100% routable interconnect.

Figure 1. EPF8050M Architecture Block Diagram



A total of 1,000 pins are connected through the routing structure: 156 I/O pins and 4 dedicated inputs on each EPF81188, and 360 I/O pins on the EPF8050M. Each signal routed through the FPIC device is connected to a maximum of 5 pins (one pin for each EPF81188, and one pin for the EPF8050M).

Normally, 180 I/O pins are available on each EPF81188. For the EPF8050M, 24 pins were removed from each EPF81188 to fit into the interconnect structure. MAX+PLUS II automatically limits each EPF81188 to 160 user pins (4 dedicated inputs and 156 I/O pins).

The EPF81188 and FPIC dedicated configuration pins are routed directly to dedicated EPF8050M pins. This feature allows independent configuration and testing of all active EPF8050M components, as well as in-circuit reconfiguration during system operation.

Go to the *FLEX 8000 Programmable Logic Device Family Data Sheet* in this data book for details on the FLEX 8000 architecture.

Package Description

The EPF8050M is available in a 2.26-inch square, 560-pin ceramic PGA package. The pins are spaced on 50-mil centers to allow for high pin density. For package dimensions, see "Pin-Out Information" on page 112 in this data sheet. For information on compatible zero-insertion-force (ZIF) sockets, see "Socket Information" on page 115 in this data sheet.

The EPF8050M contains six power planes that are routed to separate pins to help designers manage the power-supply switching effects in their system: V_{CCIO}, V_{CCINT}, GND_{IO}, and GND_{INT} for the EPF81188 devices, and V_{CC} and GND for the FPIC. V_{CCIO} and GND_{IO} are used for I/O switching planes; V_{CCINT} and GND_{INT} are used for internal quiet planes. If separate planes are available on the target system board, the user should connect them to the appropriate EPF8050M planes. If only two power planes are available on the target board, then all V_{CC} pins must be tied together and all GND pins must be tied together. Ten 0.33-µF decoupling capacitors are mounted on the MCM substrate (four each for the V_{CCIO}/GND_{IO} and V_{CCINT}/GND_{INT} power planes, and two for the FPIC power planes).

The EPF81188 devices are placed in ceramic ball-grid array (BGA) packages, mounted on the top of the MCM substrate, and covered with an anodized aluminum lid. The FPIC device is mounted to the bottom of the substrate with a controlled collapse chip connection (C4) or "bump-mount" process. The FPIC and passive components are covered with a ceramic lid. Standoffs on the MCM pins ensure that the bottom-side lid does not make contact with the PC board or socket.

Interconnect Description

The programmable interconnect used in the EPF8050M is a 1,000-point programmable switch. This switch provides routing between the EPF81188 devices and the EPF8050M pins.

The programmable interconnect is highly successful at routing designs and highly tolerant of internal pin changes. Whenever possible, external EPF8050M pin assignments are preserved when the design is recompiled.

The signal path through the interconnect uses pass transistors and is passive. This path is bidirectional, eliminating the need for complex logic for Output Enable and tri-state control circuitry. The resistive passive routing incurs a delay, and the worst-case delay for the interconnect (total delay for the FPIC and the EPF8050M package) is incorporated in the simulation model for the EPF8050M.

Applications

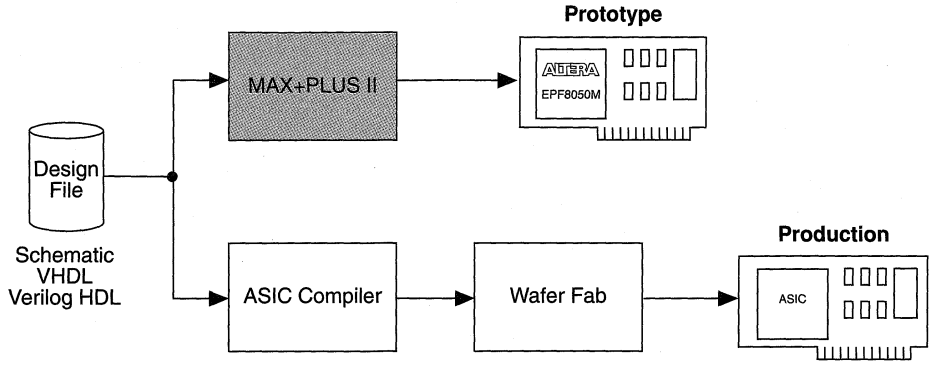
When designers use custom logic solutions such as gate arrays and ASICs to reduce cost and device count, they must ensure that designs are verified before committing them to silicon. The time required to develop and manufacture a second revision of a custom device often delays a product's market introduction.

Most designers use simulation to verify custom logic designs, analyzing a large number of test cases on a software model of the design. However, simulation is slow and typically does not exhaustively test the design. In contrast, hardware prototyping of a design is much faster than software simulation and can provide exhaustive coverage of in-circuit test conditions. Unfortunately, hardware prototyping tools are often expensive and have limited flexibility, preventing most designers from performing in-circuit prototyping of their custom logic circuits.

The EPF8050M is ideal for prototyping custom logic because it combines the best of both simulation and hardware prototyping. With MAX+PLUS II design tools, engineers can enter and simulate logic designs using either functional or timing simulation models. After simulation, the user can configure the EPF8050M and perform in-circuit hardware verification of the design.

With 50,000 usable gates, the EPF8050M is appropriate for more than 50% of today's gate array designs, and is ideally suited for gate array prototyping. The EPF8050M allows faster operating speeds than most hardware prototyping systems at a significantly reduced size and cost. It can be tested in-system, often at speeds comparable to the final system requirements. An ASIC manufactured after functional verification with an EPF8050M is more likely to function properly on first silicon. Figure 2 shows the design flow for EPF8050M and ASIC devices. The same source schematic, VHDL, or Verilog HDL file can be used for either branch of the design flow.

Figure 2. EPF8050M/ASIC Design Flow



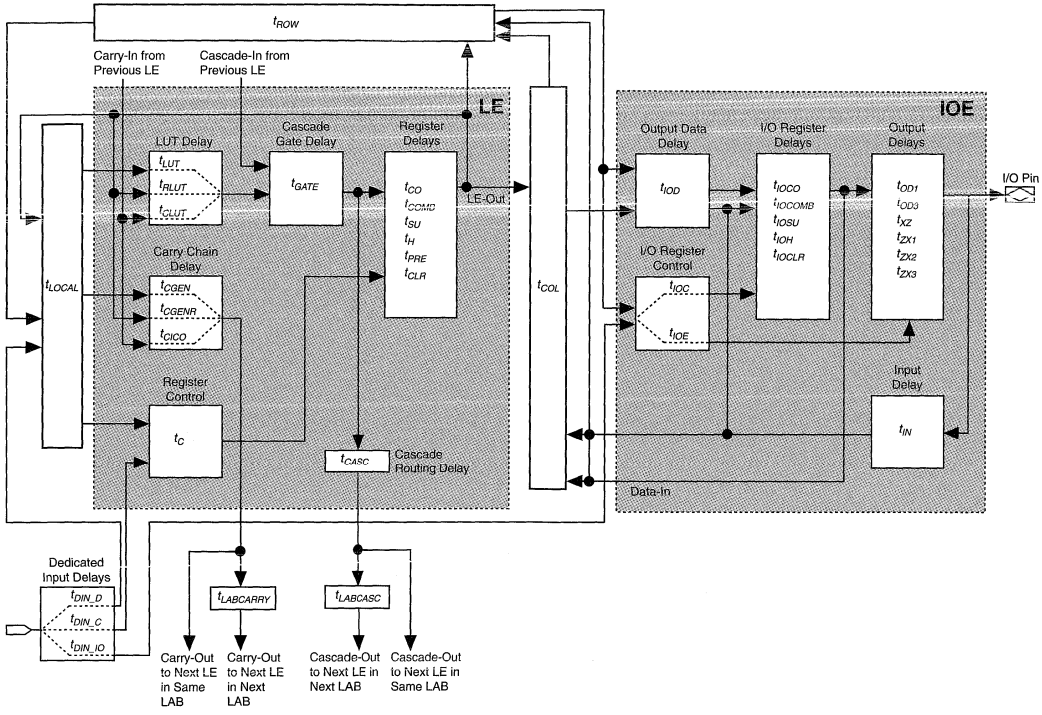
Reconfigurable hardware products (RHPs) can use the EPF8050M to pack the maximum programmable logic per square inch into advanced products that require in-circuit reconfigurability. Each EPF81188 and the FPIC can be reconfigured independently while in the target system.

Timing Model

The continuous, high-performance FastTrack Interconnect routing resources in the EPF81188 devices ensure predictable performance and accurate simulation analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and hence have unpredictable performance. Timing simulation and delay prediction are available with the MAX+PLUS II Simulator and Timing Analyzer, or with industry-standard CAE tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time analysis, and system-level performance analysis.

The FLEX 8000 timing model in Figure 3 shows the delays that correspond to various paths and functions in the circuit.

Figure 3. FLEX 8000 Timing Model



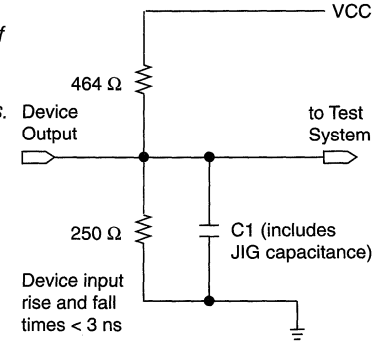
This model contains three distinct parts: the logic element (LE); the I/O element (IOE); and the interconnect, including the row and column FastTrack Interconnect, Logic Array Block (LAB) local interconnect, and carry and cascade interconnect paths. Each parameter shown in Figure 3 is expressed as a worst-case value in the "EPF8050M Internal Timing Characteristics" tables that begin on page 102 in this data sheet. Delays through the interconnect and the MCM interconnect are included in the input and output delays. Hand-calculations that use the FLEX 8000 timing model and these timing parameters can be used to estimate EPF8050M device performance. Timing simulation or timing analysis after compilation is required to determine final worst-case performance.

Generic Testing

The EPF8050M is fully tested and guaranteed. All EPF81188 devices and the FPIC device are fully tested before and after they are mounted into the EPF8050M package. This testing procedure ensures that each active component is tested individually, and as part of the entire system. Complete testing of each configurable SRAM bit and all logic functionality ensures 100% configuration yield. AC test measurements for the EPF81188 devices are made under conditions equivalent to those shown in Figure 4. Multiple test patterns can be used to configure devices during all stages of the production flow.

Figure 4. EPF8050M AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result.



Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND *Note (1)*	–2.0	7.0	V
V_I	DC input voltage		–2.0	7.0	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–10	90	° C
T_{AMB}	Ambient temperature	Under bias	–10	90	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	With respect to GND	4.75	5.25	V
V_{CCIO}	Supply voltage for output buffers		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

DC Operating Conditions *Note (2)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level TTL output voltage	I_{OL} = 4 mA DC			0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or GND	–40		40	µA
I_{CC0}	V_{CC} supply current (standby)	V_I = GND, No load, *Note (3)*		4		mA

EPF8050M Internal Timing Characteristics *Note (4)*

EPF8050M I/O Element Timing Parameters			EPF8050M-3		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_{IOD}	IOE register data delay			2.0	ns
t_{IOC}	IOE register control signal delay			2.0	ns
t_{IOE}	Output enable delay			2.0	ns
t_{IOCO}	IOE register clock-to-output delay			1.0	ns
t_{IOCOMB}	IOE combinatorial delay			0.0	ns
t_{IOSU}	IOE register setup time before clock		2.0		ns
t_{IOH}	IOE register hold time after clock		0.0		ns
t_{IOCLR}	IOE register clear delay			1.2	ns
t_{IN}	Input pad and buffer delay			8.8	ns
t_{OD1}	Output buffer and pad delay Slow slew rate = off, V_{CCIO} = 5.0 V	*Note (5)*		8.0	ns
t_{OD3}	Output buffer and pad delay Slow slew rate = on, V_{CCIO} = 5.0 V	*Note (5)*		12.0	ns
t_{XZ}	Output buffer disable delay			8.0	ns
t_{ZX}	Output buffer enable delay			8.0	ns

EPF8050M Logic Element Timing Parameters			EPF8050M-3		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_{LUT}	LUT delay for data-in			5.1	ns
t_{CLUT}	LUT delay for carry-in			1.0	ns
t_{RLUT}	LUT delay for LE register feedback			3.4	ns
t_{GATE}	Cascade gate delay			0.0	ns
t_{CASC}	Cascade chain routing delay			2.0	ns
t_{CICO}	Carry-in to carry-out delay			1.1	ns
t_{CGEN}	Data-in to carry-out delay			1.4	ns
t_{CGENR}	LE register feedback to carry-out delay			2.4	ns
t_{C}	LE register control signal delay			3.1	ns
t_{CH}	Clock high time		4.3		ns
t_{CL}	Clock low time		4.3		ns
t_{CO}	LE register clock-to-output delay			0.9	ns
t_{COMB}	Combinatorial delay			0.9	ns
t_{SU}	LE register setup time before clock		1.7		ns
t_{H}	LE register hold time after clock		4.0		ns
t_{PRE}	LE register preset delay			1.2	ns
t_{CLR}	LE register clear delay			1.2	ns

EPF8050M Interconnect Timing Parameters			EPF8050M-3		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
$t_{LABCASC}$	Cascade delay between LEs in different LABs			0.9	ns
$t_{LABCARRY}$	Carry delay between LEs in different LABs			0.6	ns
t_{LOCAL}	LAB local interconnect delay			1.0	ns
t_{ROW}	Row interconnect routing delay	*Note (6)*		5.0	ns
t_{COL}	Column interconnect routing delay			3.0	ns
t_{DIN_C}	Dedicated input to LE control delay			13.0	ns
t_{DIN_D}	Dedicated input to LE data delay	*Note (6)*		15.0	ns
t_{DIN_IO}	Dedicated input to IOE control delay			15.0	ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.

(2) Operating conditions: $V_{CC} = 5.0\ V \pm 5\%$, $T_A = 0°\ C$ to $70°\ C$ for commercial use.

(3) Unconfigured devices draw approximately 1 A.

(4) Internal timing parameters cannot be measured explicitly. The values in these tables are worst-case delays based on testable external parameters. These internal parameters should be used for estimating device performance. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.

(5) Operating conditions: $V_{CCIO} = 5.0\ V \pm 5\%$ for commercial use.

(6) The t_{ROW} and t_{DIN_D} delays are worst-case values for typical applications. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.

Software Support

The EPF8050M device is supported by the Altera MAX+PLUS II development system. Designing with the EPF8050M requires the EPF8050M migration product (PLSM-8KM) and a MAX+PLUS II system that supports FLEX 8000 devices and multi-device partitioning.

The FLEX 8000 family is supported by Altera's MAX+PLUS II development system, a single, integrated package that offers schematic, text—including the Altera Hardware Description Language (AHDL)—and waveform design entry; compilation and logic synthesis; simulation and timing analysis; and device programming. MAX+PLUS II provides EDIF 2 0 0 and 3 0 0, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and workstation-based EDA tools. MAX+PLUS II runs on 486- and Pentium-based PCs, and Sun SPARCstation, HP 9000 Series 700, and IBM RISC System/6000 workstations.

Go to the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* in this data book for more information.

MAX+PLUS II fits cleanly into an ASIC design flow. MAX+PLUS II and the target ASIC silicon compiler can share the same source file, minimizing the time required for design entry and processing. Designs entered with a specific ASIC library do not need to be modified because they can be directly mapped into MAX+PLUS II using Library Mapping Files (**.lmf**).

Go to *ApplicationBrief 96* (*Generating Library Mapping Files*) for more information.

During design processing, MAX+PLUS II automatically partitions an EPF8050M design into the four EPF81188 devices. Functional hardware emulation of the ASIC design can then be performed with the EPF8050M. Once the design is validated, the source file can be targeted at an ASIC technology library with a high level of confidence that the first silicon will work as expected.

Device Configuration

The FLEX 8000 architecture uses SRAM cells to store the configuration data for the device. These SRAM cells must be loaded each time the circuit powers up and begins operation. The process of physically loading data into the device is called *configuration*. After configuration, the device resets its registers, enables its I/O pins, and begins operation as a logic device. This reset operation is called *initialization*. Together, the configuration and initialization processes are called *command mode*; normal in-circuit device operation is called *user mode*.

The EPF8050M contains five SRAM-based devices, each of which must be loaded with configuration data. The EPF8050M supports both active and passive configuration schemes. In an active scheme, the devices receive their data from a parallel EPROM. In a passive scheme, an external host provides the data and Clock cycles to the EPF81188 and FPIC devices.

The configuration data for the EPF81188 devices is approximately 180K bits long; the configuration data for the FPIC is approximately 64K bits long. Since configuration data for the FPIC has a shorter bitstream than for the EPF81188 devices, the FPIC data is pre-padded with 1's so that all five devices complete configuration simultaneously.

Go to *Application Note 33 (Configuring FLEX 8000 Devices)* and *Application Note 38 (Configuring Multiple FLEX 8000 Devices)* for complete information on configuring FLEX 8000 devices. Go to the *FLEX 8000 Programmable Logic Device Family Data Sheet* for more information on FLEX 8000 architecture.

Active Configuration

An active configuration circuit uses a stand-alone configuration controller (typically a small PLD) to manage the configuration process and a parallel EPROM to store the configuration data. The serial configuration data for each of the EPF81188 devices and the FPIC device in the EPF8050M are stored in the bits in the parallel EPROM's 8-bit data word. The serial configuration data used to program the EPROM is stored in a Hexadecimal (Intel-format) File (**.hex**) that is created by the MCMFIT software. The first 6 bits in each EPROM word contain configuration data, as shown in Table 1.

Table 1. Configuration Bit Patterns

Data Bit	EPF8050M Destination		
	Device	Pin Name	Pin Number
Bit 0	FPIC	DIN	BC35
Bit 1	EPF81188 #1	DATA0	B4
Bit 2	EPF81188 #2	DATA0	D42
Bit 3	EPF81188 #3	DATA0	BB40
Bit 4	EPF81188 #4	DATA0	AY2
Bit 5	FPIC	PROGRAM	BC37
Bits 6 & 7	Unused	–	–

The multi-device active serial bit-slice (MD-ASB) configuration circuit is shown in Figure 5. In this scheme, one of the EPF81188 devices (EPF81188 #1 in Figure 5) is configured in the active serial (AS) configuration scheme. This device clocks the circuit and controls the configuration process. An EPM7032 support PLD controls the configuration process, generating the addresses for the parallel EPROM. The remaining EPF81188 devices and the FPIC device are configured in the passive serial (PS) configuration scheme, and latch the configuration data from the parallel EPROM on the rising edge of the active EPF81188 device's Clock signal.

Figure 5. EPF8050M Multi-Device Active Serial Bit-Slice (MD-ASB) Configuration Circuit

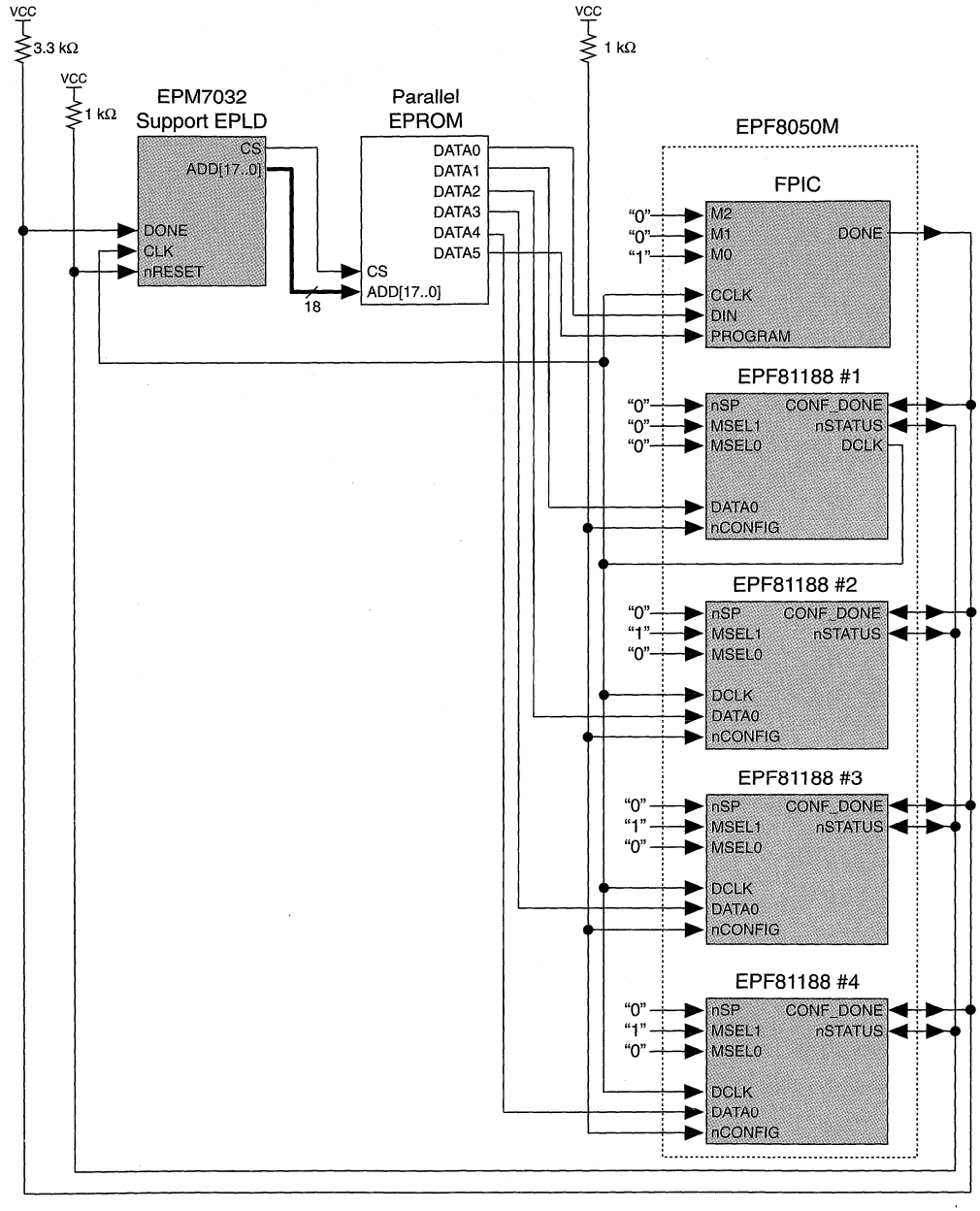


Figure 6 shows an AHDL Text Design File (**.tdf**) that implements the functions required in the EPM7032 support device.

Figure 6. AHDL Text Design File for EPM7032 Support Device (ascontrl.tdf)

```
TITLE "Active Serial 7032 Controller for EPF8050M Designs";
SUBDESIGN ascontrl
(
      clk, done, nreset   : INPUT;
      cs, add[17..0]      : OUTPUT;
)
VARIABLE
      count[17..0] : DFF;
BEGIN
      count[].clk  = global(clk);
      count[].clrn = nreset;
      count[].d    = count[].q + 1;
      add[]        = count[];
      cs           = !done;
END;
```

If one of the EPF81188 devices encounters an error during configuration, it pulls the nSTATUS net low. When the nRESET input to the EPM7032 is pulled low, the address counter in the EPM7032 is reset. When nRESET pulls high again, configuration restarts. Since all nSTATUS pins are tied together, a configuration error on any of the EPF81188 devices causes the EPF8050M to reset. Since the FPIC does not have a "configuration error" output, it is not part of the nSTATUS net. The CONF_DONE and DONE pins are tied together and pulled to V_{CC} via a 3.3-kΩ resistor. If the DONE net is high, configuration is complete and the EPF8050M is in user mode.

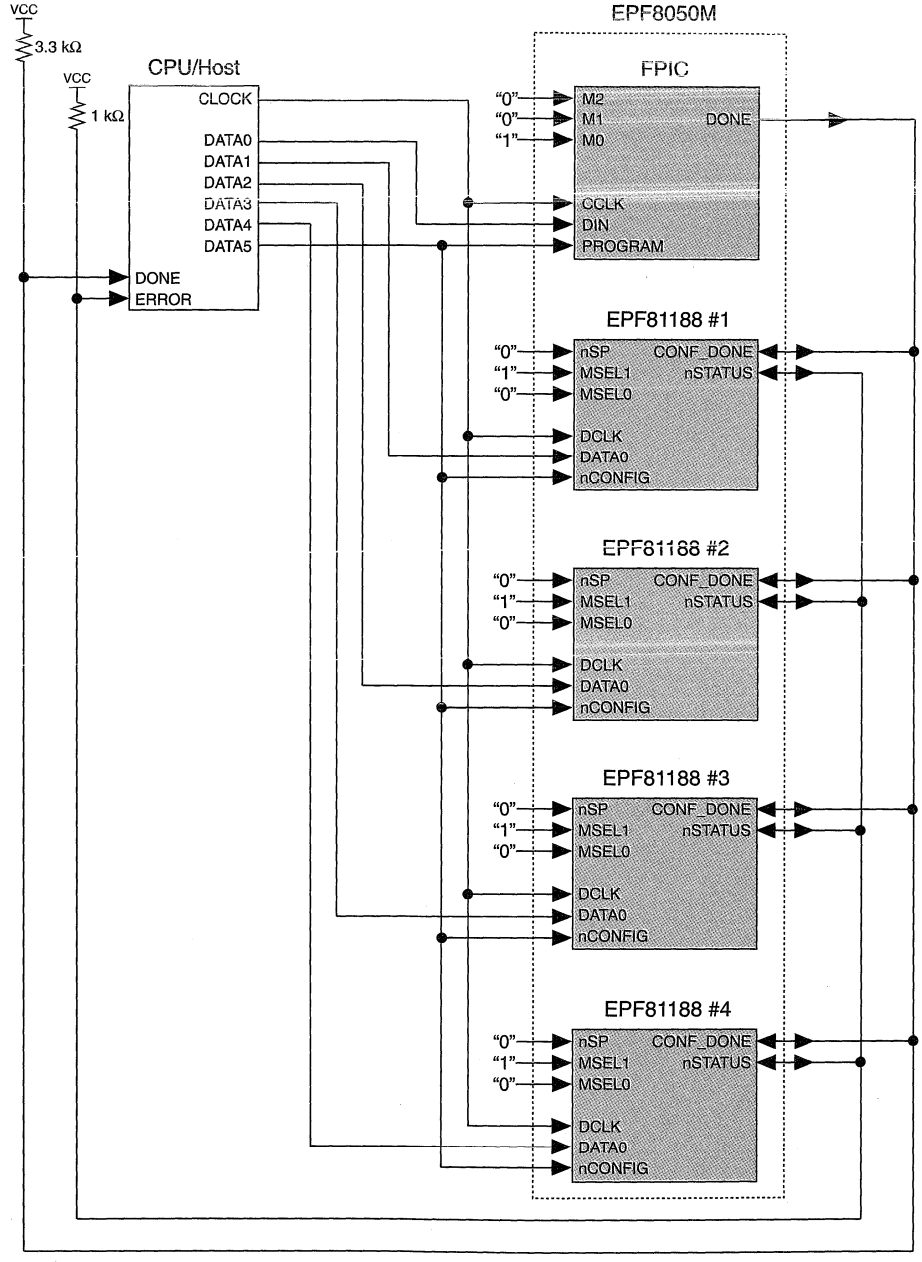
Passive Configuration

In systems with an intelligent host, configuration data is stored in memory or on a hard disk, and is loaded into the devices under control of the host. The individual devices in the EPF8050M can be configured simultaneously or individually, thereby allowing in-circuit reconfiguration. The intelligent host generates the control signals necessary to initiate and complete configuration, typically using a data port on the host and a parallel data path. The serial configuration data for each of the five configurable devices in the EPF8050M are stored in an ASCII-format Tabular Text File (**.ttf**). The first 6 bits in each byte of the TTF contain configuration data, as shown in Table 1.

Figure 7 shows the multi-device passive serial bit-slice (MD-PSB) configuration scheme. All four EPF81188 devices and the FPIC are configured with the PS configuration scheme. The intelligent host provides the configuration Clock.

The nSTATUS pins are pulled low by the EPF81188 devices during the first 64 configuration bits when the EPF8050M is reset. After the 64th bit, the nSTATUS pins are released and pulled to V_{CC} via a pull-up register. If one of the EPF81188 devices encounters an error after the 64th Clock cycle, it pulls the nSTATUS net low again. When the intelligent host detects a low level on the nSTATUS net during configuration, it restarts configuration. Since all nSTATUS pins are tied together, a configuration error on any of the EPF81188 devices causes the EPF8050M to reset. Since the FPIC does not have a "configuration error" output, it is not part of the nSTATUS net. The CONF_DONE and DONE pins are tied together and pulled to V_{CC} via a 3.3-kΩ resistor. A high level on the DONE net indicates that the configuration data has been successfully loaded. The intelligent host must then provide 10 more Clock cycles to initialize the EPF8050M.

Figure 7. EPF8050M Multi-Device Passive Serial Bit-Slice (MD-PSB) Configuration Circuit



Configuration Pins

The configuration scheme for the EPF81188 devices is selected with the nSP, MSEL1, and MSEL0 configuration pins; the configuration scheme for the FPIC is selected with the M2, M1, and M0 configuration pins. Table 2 shows valid selection patterns for the two configuration schemes for the individual EPF81188 and FPIC devices.

Table 2. Valid Selection Patterns for EPF81188 & FPIC Devices

Configuration Scheme	EPF81188 #1 nSP:MSEL1:MSEL0	EPF81188 #2, #3, #4 nSP:MSEL1:MSEL0	FPIC M2:M1:M0
MD-PSB	010	010	001
MD-ASB	000	010	001

nCONFIG & PROGRAM Pins

The nCONFIG (EPF81188) and PROGRAM (FPIC) input pins initiate configuration cycles. A high-to-low transition resets the device; a subsequent low-to-high transition starts the configuration process.

The FLEX 8000 architecture allows the user to tie the nCONFIG pin to V_{CC}, causing the EPF81188 devices to be configured immediately upon power-up. In contrast, a high-low-high pulse is required on the FPIC's PROGRAM pin for every configuration cycle.

nSTATUS Pin

The EPF81188 bidirectional open-drain nSTATUS pins are all connected to the nSTATUS net. The nSTATUS net is pulled to V_{CC} via a 1-kΩ resistor. If an error occurs during configuration, the device that detects the error pulls and holds the nSTATUS net low.

CONF_DONE & DONE Pins

The CONF_DONE (EPF81188) and DONE (FPIC) pins are open-drain "configuration complete" indicators. These pins are tied together and pulled to V_{CC} via a 3.3-kΩ resistor. After the configuration data has been loaded, each device releases its CONF_DONE or DONE pin. Once all five devices are completely configured, the DONE net is pulled to V_{CC}, indicating that the EPF8050M is in user mode. Holding an EPF81188 CONF_DONE pin low prevents the EPF81188 from entering the user mode. In contrast, holding the FPIC's DONE pin low does not prevent the FPIC from entering user mode.

Configuration File Formats

In active configuration schemes, the configuration data for all five devices (four EPF81188 devices and one FPIC device) is combined into a Hexadecimal (Intel-format) File (**.hex**) for device programming. This conversion is automatically performed by the Altera-provided MCMFIT software. The Hex File contains the address information necessary to program a standard 256K × 8 bit parallel EPROM with the configuration data.

In passive configuration schemes, the MCMFIT software automatically converts the configuration data into a Tabular Text File (**.ttf**), an ASCII text file that contains decimal values for each byte. The intelligent host reads an ASCII word from the TTF, converts it to a binary pattern, and provides the six low-order bits to the corresponding devices in the EPF8050M.

Pin-Out Information

Tables 3, 4, and 5 show the device pin-outs for EPF8050M configuration pins, power pins, and I/O pins, respectively.

Table 3. EPF8050M Configuration Pin-Outs

Pin Name	FPIC	EPF81188 #1	EPF81188 #2	EPF81188 #3	EPF81188 #4
nSP	–	D4	D40	AY40	AY4
MSEL0	–	A1	A43	BC43	BC1
MSEL1	–	A3	C43	BC41	BA1
nCONFIG	–	C1	A41	BA43	BC3
DCLK	–	C5	B38	AV42	AW5
nSTATUS	–	B2	B42	BB42	BB2
CONF_DONE	–	A5	E43	BC39	AW1
DATA0	–	B4	D42	BB40	AY2
M0	AW3	–	–	–	–
M1	AV2	–	–	–	–
M2	AU1	–	–	–	–
PROGRAM	BC37	–	–	–	–
DIN	BC35	–	–	–	–
CCLK	BC7	–	–	–	–
DONE	AW41	–	–	–	–

Table 4. EPF8050M VCC and GND Pin-Outs

Pin Name	EPF8050M Pin-Outs
VCCIO	E37, F14, F8, F20, F26, F32, H16, H38, J39, K6, K42, P38, T6, Y38, AB6, AF38, AH6, AM38, AT16, AU7, AU37, AV14, AV20, AV26, AV32, AV40, BA37, BB18, BB38
GNDIO	B18, C39, E41, G9, G15, G17, G21, G27, G33, J37, L7, N37, U7, W37, AC7, AE37, AJ5, AJ7, AL37, AT8, AT18, AT36, AU13, AU19, AU25, AU31, AU41, AW37, BA39
VCCINT	A39, B10, B16, B22, B28, B36, C3, C41, E1, G5, H12, J43, M2, M42, T42, V2, AB42, AD2, AH42, AK2, AP42, AT12, AU5, AW39, AW43, BA3, BA41, BB14, BB20, BB26, BB32, BC5
GNDINT	B40, C11, C17, C23, C29, C37, D2, H6, H14, H42, L43, N3, R41, W3, AA41, AE3, AG41, AL3, AN41, AT14, AV6, AY38, AY42, BA13, BA19, BA25, BA31, BB4
VCCFPIC	B6, B14, B20, B26, B32, G1, G43, P2, P42, Y2, Y42, AF2, AF42, AM2, AM42, AY36, BB6, BB16, BB22, BB28
GNDFPIC	A7, C7, C15, C21, C27, C33, F42, H2, N41, R3, W41, AA3, AE41, AG3, AL41, AN3, AW35, BA5, BA15, BA21, BA27
No Connect (N.C.)	AU43, BC9

Table 5. EPF8050M I/O Pins

A9	D26	F34	K2	T8	AB8	AH8	AP8	AU33	AY18
A11	D28	F36	K4	T36	AB36	AH36	AP36	AU35	AY20
A13	D30	F38	K8	T38	AB38	AH38	AP38	AU39	AY22
A15	D32	F40	K36	T40	AB40	AH40	AP40	AV4	AY24
A17	D34	G3	K38	U1	AC1	AJ1	AR1	AV8	AY26
A19	D36	G7	K40	U3	AC3	AJ3	AR3	AV10	AY28
A21	D38	G11	L1	U5	AC5	AJ37	AR5	AV12	AY30
A23	E3	G13	L3	U37	AC37	AJ39	AR7	AV16	AY32
A25	E5	G19	L5	U39	AC39	AJ41	AR37	AV18	AY34
A27	E7	G23	L37	U41	AC41	AJ43	AR39	AV22	BA7
A29	E9	G25	L39	U43	AC43	AK4	AR41	AV24	BA9
A31	E11	G29	L41	V4	AD4	AK6	AR43	AV28	BA11
A33	E13	G31	M4	V6	AD6	AK8	AT2	AV30	BA17
A35	E15	G35	M6	V8	AD8	AK36	AT4	AV34	BA23
A37	E17	G37	M8	V36	AD36	AK38	AT6	AV36	BA29
B8	E19	G39	M36	V38	AD38	AK40	AT10	AV38	BA33
B12	E21	G41	M38	V40	AD40	AK42	AT20	AW7	BA35
B24	E23	H4	M40	V42	AD42	AL1	AT22	AW9	BB8
B30	E25	H8	N1	W1	AE1	AL5	AT24	AW11	BB10
B34	E27	H10	N5	W5	AE5	AL7	AT26	AW13	BB12
C9	E29	H18	N7	W7	AE7	AL39	AT28	AW15	BB24
C13	E31	H20	N39	W39	AE39	AL43	AT30	AW17	BB30
C19	E33	H22	N43	W43	AE43	AM4	AT32	AW19	BB34
C25	E35	H24	P4	Y4	AF4	AM6	AT34	AW21	BB36
C31	E39	H26	P6	Y6	AF6	AM8	AT38	AW23	BC11
C35	F2	H28	P8	Y8	AF8	AM36	AT40	AW25	BC13
D6	F4	H30	P36	Y36	AF36	AM40	AT42	AW27	BC15
D8	F6	H32	P40	Y40	AF40	AN1	AU3	AW29	BC17
D10	F10	H34	R1	AA1	AG1	AN5	AU9	AW31	BC19
D12	F12	H36	R5	AA5	AG5	AN7	AU11	AW33	BC21
D14	F16	H40	R7	AA7	AG7	AN37	AU15	AY6	BC23
D16	F18	J1	R37	AA37	AG37	AN39	AU17	AY8	BC25
D18	F22	J3	R39	AA39	AG39	AN43	AU21	AY10	BC27
D20	F24	J5	R43	AA43	AG43	AP2	AU23	AY12	BC29
D22	F28	J7	T2	AB2	AH2	AP4	AU27	AY14	BC31
D24	F30	J41	T4	AB4	AH4	AP6	AU29	AY16	BC33

Socket Information

Zero-insertion-force sockets are available from AMP:

25 × 25 Socket Assembly (Proposal Number: 94-3409-025-002)

Notes:

March 1995

MAX 9000 Programmable Logic Device Family


ALTERA
MAX®
EPM9560GC280
ALTERA
MAX®
EPM9560RC208
ALTERA
MAX®
EPM9560RC240

MAX 9000

Programmable Logic Device Family

March 1995, ver. 2 — Data Sheet

Features...

Preliminary Information

- High-performance EEPROM-based programmable logic devices (PLDs) built on third-generation Multiple Array MatriX (MAX) architecture
- Fabricated on 0.65-micron CMOS technology
- High-density EPLD family ranging from 6,000 usable (12,000 available) gates to 12,000 usable (24,000 available) gates (see Table 1)
- 12-ns pin-to-pin logic delays with counter frequencies up to 125-MHz
- PCI-compliant -12 speed grade
- 5.0-V in-system programmability (ISP) through Built-in Joint Test Action Group (JTAG) interface
- Built-in JTAG boundary-scan test (BST) circuitry with internal scan capability
- Dual-output macrocell for independent use of combinatorial and registered logic
- FastTrack continuous routing structure for fast, predictable interconnect delays
- Input/output registers with Clock Enable on all I/O pins
- Programmable output slew-rate control to reduce switching noise
- 3.3-V or 5.0-V I/O operation on all devices
- Configurable expander product-term distribution allowing up to 32 product terms per macrocell

Table 1. MAX 9000 Device Features *Note (1)*

Feature	EPM9320	EPM9400	EPM9480	EPM9560
Available gates	12,000	16,000	20,000	24,000
Usable gates	6,000	8,000	10,000	12,000
Flipflops	484	580	676	772
Macrocells	320	400	480	560
Maximum user I/O	168	184	200	216
t_{PD1} (ns)	12	12	15	15
t_{FSU} (ns)	3	3	5	5
t_{FCO} (ns)	6	6	7	7
f_{CNT} (MHz)	125	125	118	118

Note:
(1) This information is preliminary.

... and More Features

- Programmable power-saver mode for more than 50% power reduction in each macrocell
- Programmable macrocell flipflops with individual Clear, Preset, Clock, and Clock Enable controls
- Programmable Security Bit for total protection of proprietary designs
- Software design support provided by Altera's MAX+PLUS II development system on 486- and Pentium-based PCs, and Sun SPARCstation, HP 9000 Series 700, and IBM RISC System/6000 workstations
- Additional design entry and simulation support provided by EDIF, Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Data I/O, Exemplar, Intergraph, Mentor Graphics, OrCAD, Synopsys, and Viewlogic
- Programming support with Altera's Master Programming Unit (MPU) and BitBlaster, and programming hardware from other manufacturers
- Offered in a variety of package options with 84 to 304 pins (see Table 2)

Table 2. MAX 9000 Package Options & I/O Count *Note (1)*

Device	84-Pin PLCC	160-Pin RQFP	208-Pin RQFP	240-Pin RQFP	280-Pin PGA	304-Pin RQFP
EPM9320	60 *(2)*	120	132	–	168	–
EPM9400	59 *(2)*	–	139	159	184	–
EPM9480	–	117	146	175	200	–
EPM9560	–	–	153 *(3)*	191	216	216

Notes:
(1) Contact Altera for up-to-date information on package availability.
(2) Perform a complete thermal analysis before committing a design to this device package. See *Operating Requirements for Altera Devices* in this data book for more information.
(3) The EPM9560 device is initially available in a 208-pin CQFP package.

General Description

The MAX 9000 family of in-system-programmable, high-density, high-performance EEPROM-based EPLDs is based on Altera's third-generation MAX architecture. Fabricated on advanced 0.65-micron CMOS technology, the MAX 9000 family provides 6,000 to 12,000 usable gates, pin-to-pin delays as fast as 12 ns, and counter speeds of up to 125 MHz. The -12 speed grade of the MAX 9000 family is compliant with the ***PCI Local Bus Specification***. Table 3 shows the speed grades available for MAX 9000 devices.

Table 3. MAX 9000 Speed Grade Availability *Note (1)*			
Device	**Speed Grade**		
	-12	**-15**	**-20**
EPM9320	✓	✓	✓
EPM9400	✓	✓	✓
EPM9480	–	✓	✓
EPM9560	–	✓	✓

Note:
(1) This information is preliminary.

Table 4 shows the performance of MAX 9000 devices for typical functions.

Table 4. MAX 9000 Performance *Notes (1), (2)*					
Application	**Macrocells Used**	**Speed Grade**			**Unit**
		-12	**-15**	**-20**	
16-bit loadable counter	16	125	118	100	MHz
16-bit up/down counter	16	125	118	100	MHz
16-bit prescaled counter	16	125	118	100	MHz
16-bit address decode	1	7 (12)	8.5 (15)	10 (20)	ns
16-to-1 multiplexer	1	9.4 (14.4)	11.5 (18)	16 (26)	ns

Notes:
(1) Internal Logic Array Block (LAB) performance is shown. Numbers in parentheses show external delays from row input to row I/O.
(2) This information is preliminary.

The MAX 9000 architecture supports high-density integration of system-level logic functions. It easily integrates multiple programmable logic devices ranging from PALs, GALs, and 22V10s to field-programmable gate array (FPGA) devices and Erasable Programmable Logic Devices (EPLDs). With speed, density, and I/O resources comparable to commonly used masked gate arrays, MAX 9000 EPLDs are also ideal for gate-array prototyping.

All MAX 9000 device packages provide four dedicated inputs for global control signals with large fan-outs. Each I/O pin has an associated I/O cell register with a Clock Enable control on the periphery of the device. As outputs, these registers provide fast Clock-to-output times; as inputs, they offer quick setup times.

MAX 9000 EPLDs provide 5.0-V in-system programmability (ISP). This feature allows the devices to be programmed and reprogrammed on the printed circuit board for quick and efficient iterations during design development and debug cycles. MAX 9000 devices are guaranteed for 100 program and erase cycles.

MAX 9000 EPLDs contain from 320 to 560 macrocells that are combined into groups of 16 macrocells, called Logic Array Blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register with independently programmable Clock, Clock Enable, Clear, and Preset functions. For increased flexibility, each macrocell offers a dual-output structure that allows the register and the product terms to be used independently. This feature allows register-rich and combinatorial-intensive designs to be implemented efficiently. The dual-output structure of the MAX 9000 macrocell also improves logic utilization, thus increasing the effective capacity of the devices. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and high-speed parallel expander product terms to provide up to 32 product terms per macrocell.

The MAX 9000 family provides programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remainder runs at reduced speed/low power. This speed/power optimization feature enables the user to configure one or more macrocells to operate at 50% or less power while adding only a nominal timing delay. MAX 9000 devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching. MAX 9000 output drivers can be set for either 3.3-V or 5.0-V operation, allowing MAX 9000 devices to be used in mixed-voltage systems.

The MAX 9000 family is supported by Altera's MAX+PLUS II development system, a single, integrated package that offers schematic, text—including the Altera Hardware Description Language (AHDL)—and waveform design entry; compilation and logic synthesis; simulation and timing analysis; and device programming. MAX+PLUS II provides EDIF 2 0 0 and 3 0 0, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and workstation-based EDA tools. MAX+PLUS II runs on 486- and Pentium-based PCs, and Sun SPARCstation, HP 9000 Series 700, and IBM RISC System/6000 workstations.

For more information, go to the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* in this data book.

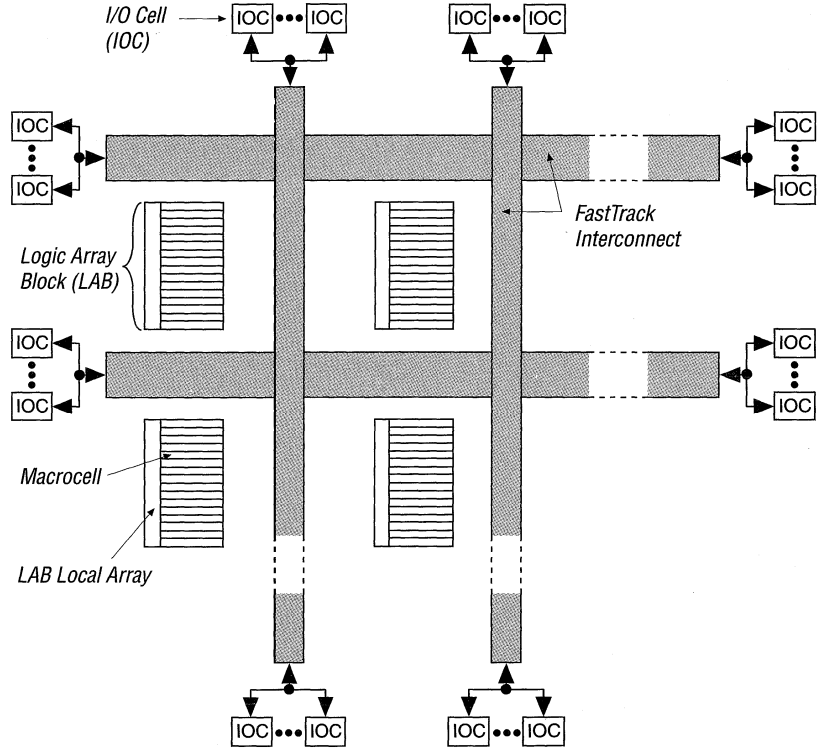
Functional Description

MAX 9000 devices use third-generation MAX architecture that yields both high performance and a high degree of utilization for most applications. The MAX 9000 architecture includes the following elements:

- Logic Array Blocks
- Macrocells
- Expander product terms (shareable and parallel)
- FastTrack Interconnect
- Dedicated inputs
- I/O cells

Figure 1 shows a block diagram of the MAX 9000 architecture.

Figure 1. MAX 9000 Device Block Diagram



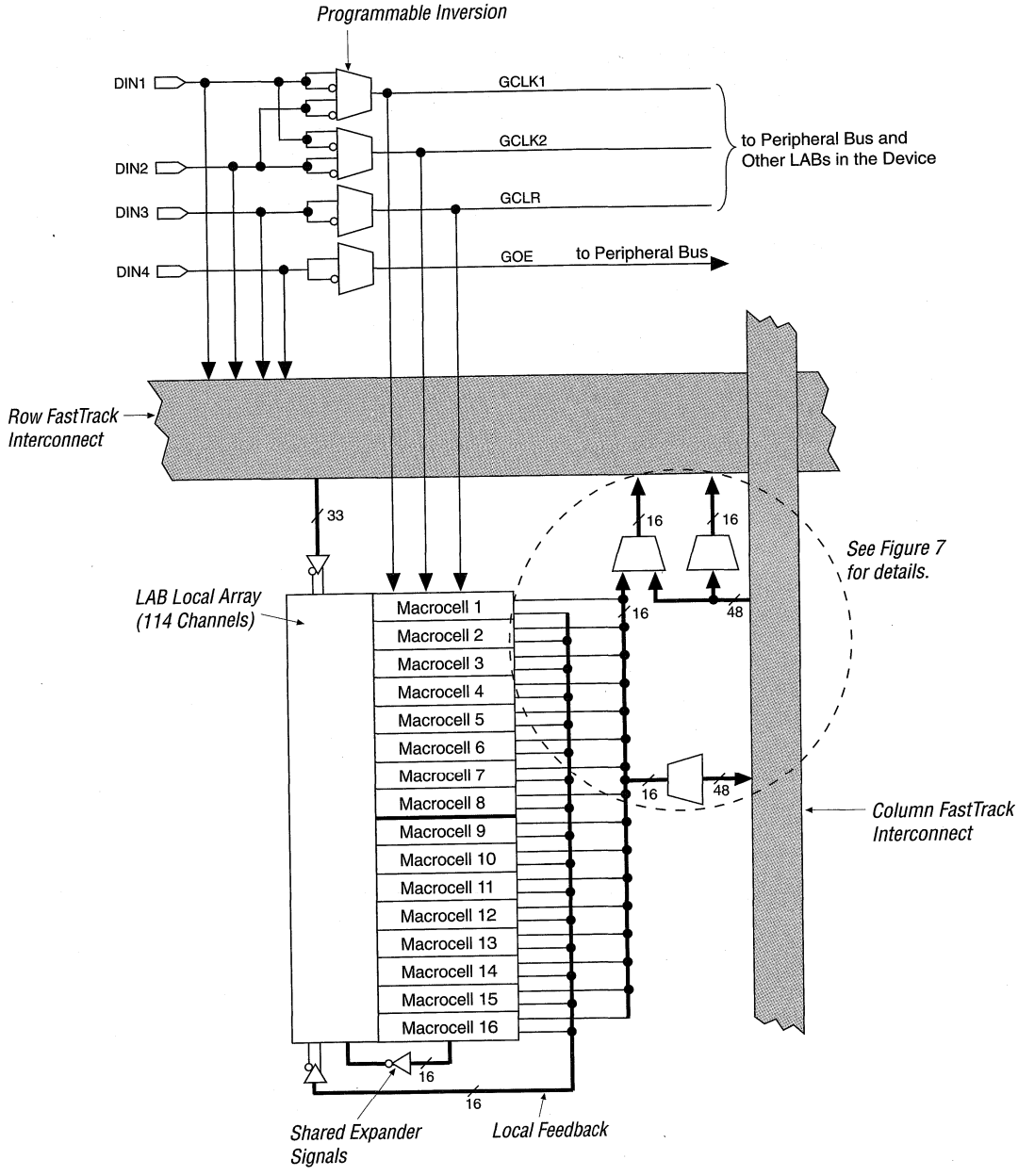
Logic Array Blocks

The MAX 9000 architecture is based on the concept of linking high-performance, flexible logic array modules called Logic Array Blocks (LABs). LABs consist of 16-macrocell arrays that are fed by the LAB local array, as shown in Figure 2. Multiple LABs are linked together via the FastTrack Interconnect, a series of fast, continuous channels that run the entire length and width of the device. The I/O pins are supported by IOCs located at the end of each row (horizontal) and column (vertical) path of the FastTrack Interconnect.

Each LAB is fed by 33 inputs from the row interconnect and 16 feedback signals from the macrocells within the LAB. All of these signals are available within the LAB in their true and inverted form. In addition, 16 shared expander product terms ("expanders") are available in their inverted form, for a total of 114 signals that feed each product term in the LAB. Each LAB is also fed by two low-skew global Clocks and one global Clear that can be used for register control signals in all 16 macrocells.

The LAB drives the row and column interconnect directly. Each macrocell can drive out of the LAB onto one or both of these routing resources. Once signals are on the row or column interconnect, they can quickly traverse to other LABs or to the IOCs.

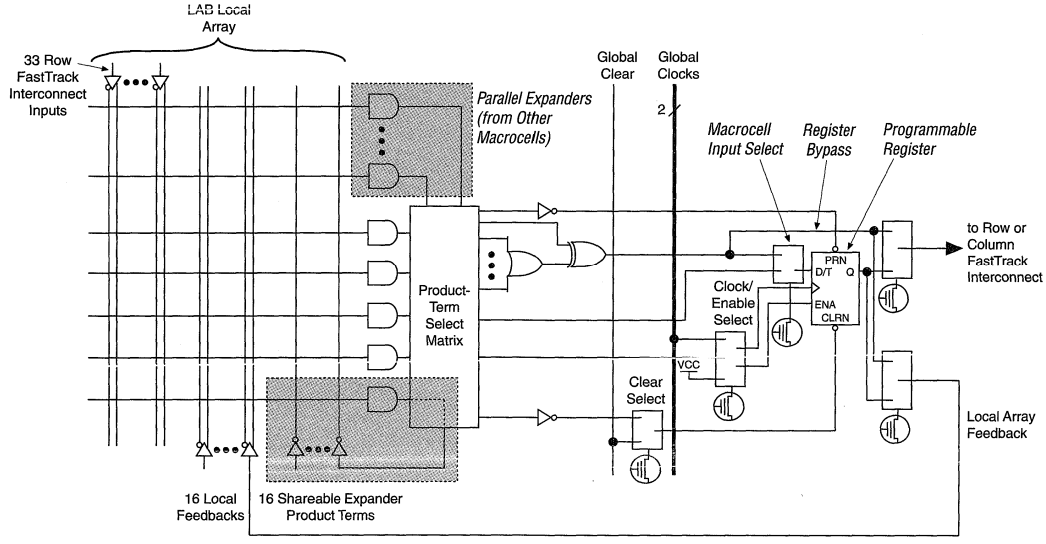
Figure 2. MAX 9000 Logic Array Block



Macrocells

The MAX 9000 macrocell consists of three functional blocks: the product terms, the product-term select matrix, and the programmable register. The macrocell can be individually configured for both sequential and combinatorial logic operation. See Figure 3.

Figure 3. MAX 9000 Macrocell & Local Array



Combinatorial logic is implemented in the local array, which provides five product terms per macrocell. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register Clear, Preset, Clock, and Clock Enable control functions. To supplement the logic resources of a macrocell, two types of expander product terms are available: shareable and parallel. Shareable expanders are inverted product terms that are fed back into the logic array; parallel expanders are product terms borrowed from adjacent macrocells. Based on the logic requirements of the design, MAX+PLUS II automatically optimizes product-term allocation.

For registered functions, each macrocell register can be individually programmed for D, T, JK, or SR operation with programmable Clock control. The flipflop can also be bypassed for combinatorial operation. During design entry, the user specifies the desired register type; MAX+PLUS II then selects the most efficient register operation for each registered function to minimize the resources needed by the design.

Each programmable register can be clocked in three different modes:

- By either global Clock signal. This mode achieves the fastest Clock-to-output performance.
- By a global Clock signal and enabled by an active-high Clock Enable. This mode provides an Enable on each flipflop while still achieving the fast Clock-to-output performance of the global Clock.
- By an array Clock implemented with a product term. In this mode, the flipflop can be clocked by signals from buried macrocells or I/O pins.

Two global Clock signals are available. As shown in Figure 2, these global Clock signals can be the true or the complement of either of the global Clock pins, DIN1 and DIN2.

Each register also supports asynchronous Preset and Clear functions. As shown in Figure 3, the product-term select matrix allocates product terms to control these operations. Although the product-term-driven Preset and Clear inputs to registers are active high, active-low control can be obtained by inverting the signal within the logic array. In addition, each register Clear function can be individually driven by the dedicated global Clear pin (DIN3). The global Clear can be programmed for active-high or active-low operation.

All MAX 9000 macrocells offer a dual-output structure that provides independent register and combinatorial logic output within the same macrocell. This function is implemented by a process called register packing. When register packing is used, the product-term select matrix allocates one product term to the D input to the register, while the remaining product terms can be used to implement unrelated combinatorial logic. Both the registered and the combinatorial output of the macrocell can feed either the FastTrack Interconnect or the LAB local array.

Expander Product Terms

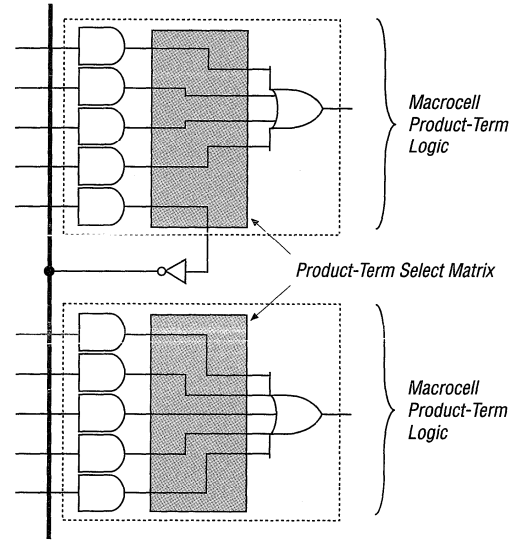
Although most logic functions can be implemented with the five product terms available in each macrocell, some logic functions are more complex and require additional product terms. Although another macrocell can supply the required logic resources, the MAX 9000 architecture also offers both shareable and parallel expander product terms that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

Shareable Expanders

Each LAB has 16 shareable expanders that can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the LAB local array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. A small delay ($t_{LOCAL} + t_{SEXP}$) is incurred when shareable expanders are used. Figure 4 shows how shareable expanders can feed multiple macrocells.

Figure 4. Shareable Expanders

Shareable expanders can be shared by any or all macrocells in the LAB.

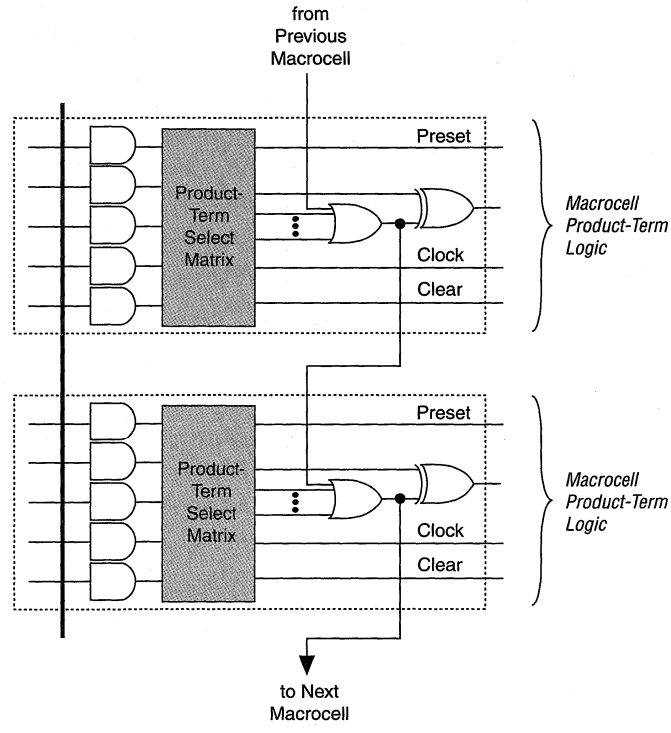


Parallel Expanders

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with 5 product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB. Figure 5 shows how parallel expanders can feed the neighboring macrocell.

Figure 5. Parallel Expanders

Unused product terms in a macrocell can be allocated to a neighboring macrocell.



The MAX+PLUS II Compiler can automatically allocate as many as 3 sets of up to 5 parallel expanders to the macrocells that require additional product terms. Each set of expanders incurs a small, incremental timing delay (t_{PEXP}). For example, if a macrocell requires 14 product terms, the Compiler uses the 5 dedicated product terms within the macrocell and allocates 2 sets of parallel expanders; the first set includes 5 product terms and the second set includes 4 product terms, increasing the total delay by $2 \times t_{PEXP}$.

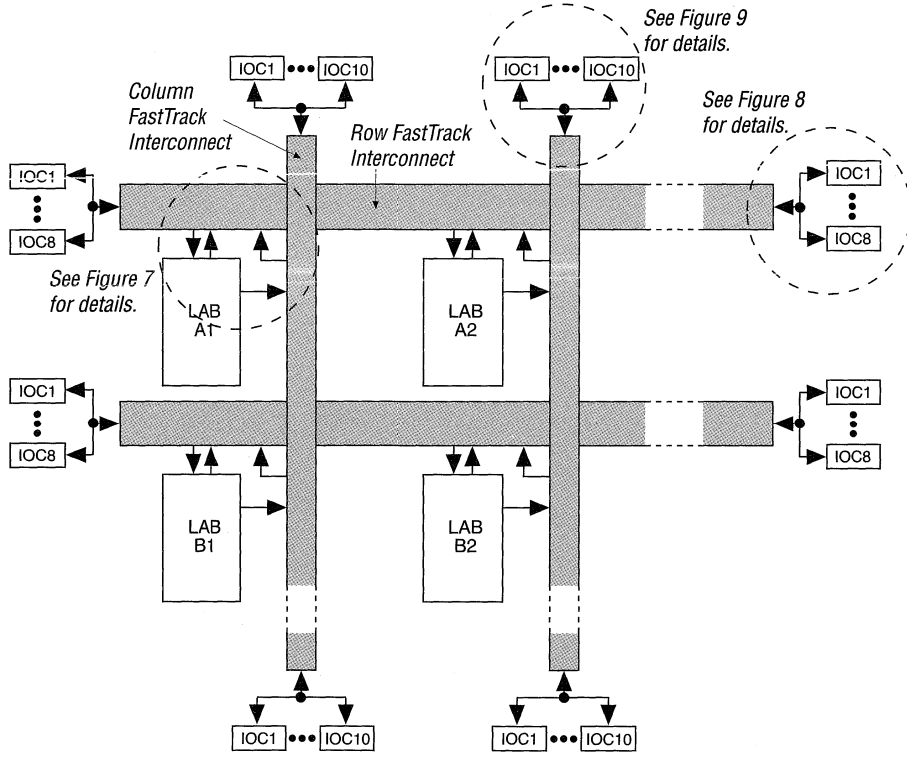
Two groups of 8 macrocells within each LAB (e.g., macrocells 1 to 8 and 9 to 16) form 2 chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of 8, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them.

FastTrack Interconnect

In the MAX 9000 architecture, connections between macrocells and device I/O pins are provided by the FastTrack Interconnect, a series of continuous horizontal and vertical routing channels that traverse the entire MAX 9000 device. This device-wide routing structure provides predictable performance even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance. Figure 6 shows the interconnection of four adjacent LABs with row and column interconnects.

Figure 6. MAX 9000 Device Interconnect Resources

Each LAB is named on the basis of its physical row (A, B, C, etc.) and column (1, 2, 3, etc.) position within the device.



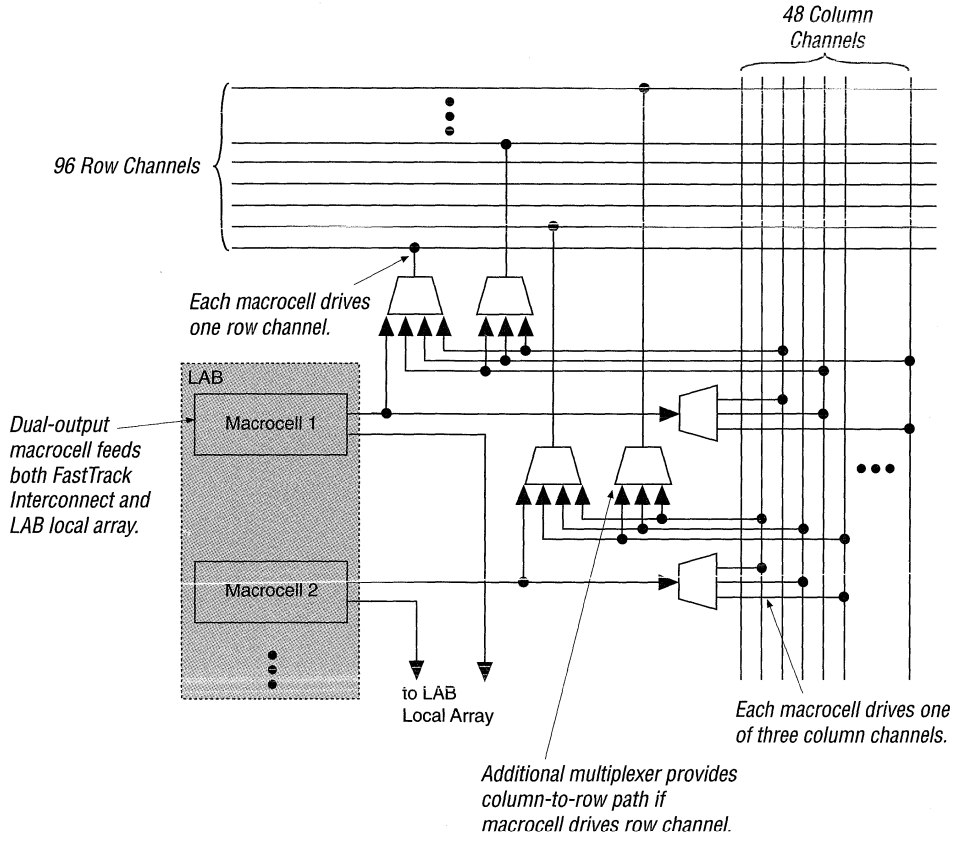
The LABs within MAX 9000 devices are arranged into a matrix of columns and rows. Table 5 shows the number of columns and rows in each MAX 9000 device.

Table 5. MAX 9000 Rows & Columns

Device	Rows	Columns
EPM9320	4	5
EPM9400	5	5
EPM9480	6	5
EPM9560	7	5

Each row of LABs has a dedicated row interconnect that routes signals both into and out of the LABs in the row. The row interconnect can then drive I/O pins or feed other LABs in the device. Each row interconnect has a total of 96 channels. Figure 7 shows how a macrocell drives the row and column interconnect.

Figure 7. LAB Connections to Row & Column Interconnect



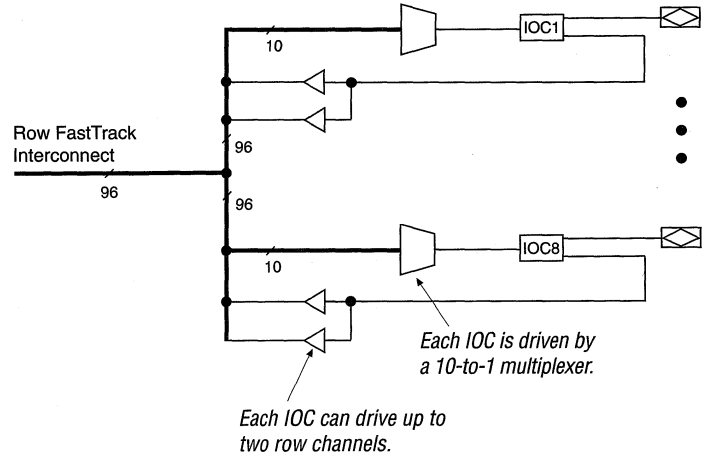
Each macrocell in the LAB can drive one of three separate column interconnect channels. The column channels run vertically across the entire device, and are shared by the macrocells in the same column. The MAX+PLUS II Compiler automatically optimizes connections to a column channel.

A row interconnect channel can be fed by the output of the macrocell through a 4-to-1 multiplexer that the macrocell shares with three column channels. If the multiplexer is used for a macrocell-to-row connection, the three column signals can access another row channel via an additional 3-to-1 multiplexer. Within any LAB, the multiplexers provide all 48 column channels with access to 32 row channels.

Row-to-I/O Cell Connections

Figure 8 illustrates the connections between row interconnect channels and I/O cells (IOCs). An input signal from an IOC can drive two separate row channels. When an IOC is used as an output, the signal is driven by a 10-to-1 multiplexer that selects the row channels. Each end of the row channel feeds up to eight IOCs on the periphery of the device.

Figure 8. MAX 9000 Row-to-IOC Connections



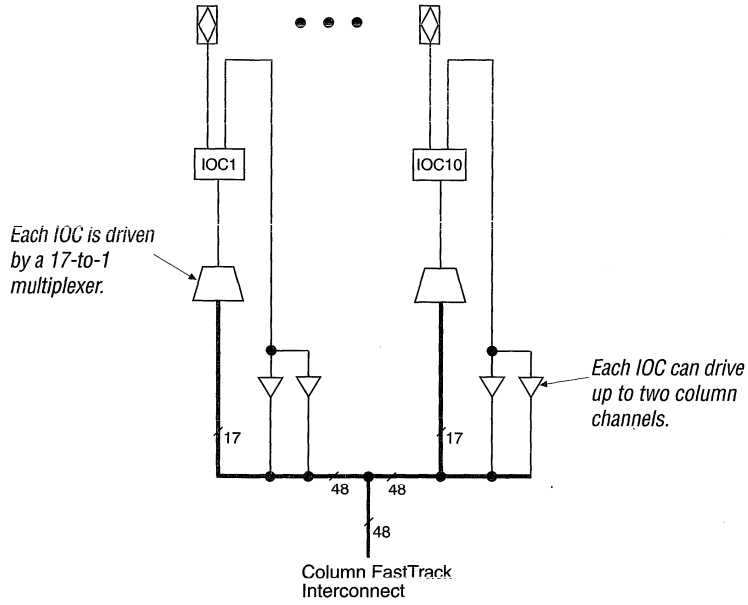
Column-to-I/O Cell Connections

Each end of a column channel has up to 10 IOCs (see Figure 9). An input signal from an IOC can drive two separate column channels. When an IOC is used as an output, the signal is driven by a 17-to-1 multiplexer that selects the column channels.

Dedicated Inputs

In addition to the general-purpose I/O pins, MAX 9000 devices have four dedicated input pins. These dedicated inputs provide low-skew, device-wide signal distribution to the LABs and IOCs in the device, and are typically used for global Clock, Clear, and Output Enable control signals. The global control signals can feed the macrocell or IOC Clock and Clear inputs, as well as the IOC Output Enable. The dedicated inputs can also be used as general-purpose data inputs because they can feed the row FastTrack Interconnect.

Figure 9. MAX 9000 Column-to-IOC Connections

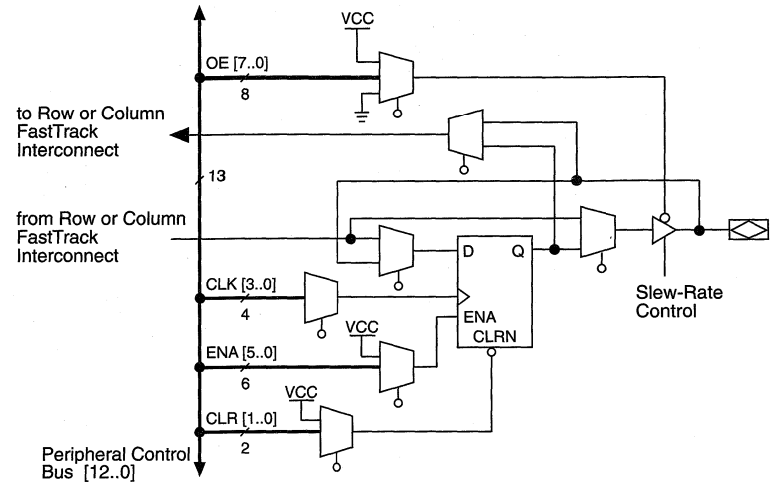


I/O Cells

Figure 10 shows the I/O cell (IOC) block diagram. Signals enter the MAX 9000 device from either the I/O pins that provide general-purpose input capability or from the four dedicated inputs. The IOCs are located at the ends of the row and column interconnect channels.

I/O pins can be used as input, output, or bidirectional pins. Each I/O cell has an I/O cell register with a Clock Enable input. This register can be used either as an input register for external data that requires fast setup times, or as an output register for data that requires fast Clock-to-output performance. The I/O cell register Clock Enable allows the global Clock to be used for fast Clock-to-output performance, while maintaining the flexibility required for selective clocking.

Figure 10. I/O Cell (IOC)



The Clock, Clock Enable, Clear, and Output Enable controls for the IOCs are provided by a network of I/O control signals. These signals can be supplied by either the dedicated input pins or internal logic. The IOC control-signal paths are designed to minimize the skew across the device. All control-signal sources are buffered onto high-speed drivers that drive the signals around the periphery of the device. This "peripheral bus" can be configured to provide up to eight Output Enable signals, up to four Clock signals, up to six Clock Enable signals, and up to two Clear signals. Table 6 shows the sources that drive the peripheral bus and how the IOC control signals share the peripheral bus.

The output buffer in each IOC has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A slower slew rate reduces board-level noise and adds a nominal timing delay to the output buffer delay (t_{OD}) parameter. The fast slew rate should be used for speed-critical outputs in systems that are adequately protected against noise. Designers can specify the slew rate on a pin-by-pin basis during design entry or assign a default slew rate to all pins on a global basis.

Table 6. Peripheral Bus Sources

Peripheral Control Signal	Source			
	EPM9320	EPM9400	EPM9480	EPM9560
OE0/ENA0	Row 3	Row 5	Row 6	Row 7
OE1/ENA1	Row 2	Row 5	Row 6	Row 6
OE2/ENA2	Row 1	Row 5	Row 5	Row 5
OE3/ENA3	Row 2	Row 2	Row 2	Row 2
OE4/ENA4	Row 1	Row 1	Row 1	Row 1
OE5	Row 4	Row 4	Row 4	Row 4
OE6	Row 3	Row 3	Row 3	Row 3
OE7/CLR1	Row 2/GOE	Row 2/GOE	Row 2/GOE	Row 2/GOE
CLR0/ENA5	Row 1/GCLR	Row 1/GCLR	Row 1/GCLR	Row 1/GCLR
CLK0	GCLK1	GCLK0	GCLK0	GCLK0
CLK1	GCLK2	GCLK1	GCLK1	GCLK1
CLK2	Row 4	Row 4	Row 4	Row 4
CLK3	Row 3	Row 3	Row 3	Row 3

3.3-V or 5.0-V I/O Operation

All MAX 9000 devices can be set to interface at 3.3 V or 5.0 V. These devices have one set of V_{CC} pins for internal operation and input buffers (V_{CCINT}), and another set for I/O output drivers (V_{CCIO}).

The V_{CCINT} pins must always be connected to a 5.0-V supply. With a 5.0-V V_{CCINT} level, input voltages are at TTL levels and are therefore compatible with 3.3-V and 5.0-V inputs. The V_{CCIO} pins can be connected to either a 3.3-V or 5.0-V supply, depending on the output requirements. When the V_{CCIO} pins are connected to a 5.0-V supply, the output levels are compatible with 5.0-V systems. When the V_{CCIO} pins are connected to a 3.3-V supply, the output high is at 3.3 V and is therefore compatible with 3.3-V systems. Devices operating with a 3.3-V V_{CCIO} level incur a nominal timing delay adder for the output buffer delay (t_{OD}).

In-System Programmability (ISP)

MAX 9000 devices are in-system-programmable through a 4-pin JTAG interface. In-system programmability (ISP) offers quick and efficient iterations during design development and debug cycles. The MAX 9000 architecture employs internal charge pumps to generate the 12.0-V programming voltage, eliminating the need for an external 12.0-V power supply to program the devices on the board.

ISP simplifies the manufacturing flow by allowing the devices to be mounted on a printed circuit board with standard pick-and-place equipment before they are programmed. Programming can be completed as part of the board testing procedure, eliminating lead damage on high-pin-count packages, such as QFP packages, due to handling during programming. Product upgrades can be performed in the field via software or modem.

For more information on how to use ISP in MAX 9000 devices, refer to *Application Brief 141 (In-System Programmability Using MAX 9000 Devices)*.

MAX 9000 EPLDs can also be programmed on 486- and Pentium-based PCs with MAX+PLUS II, the Altera Master Programming Unit (MPU), and the appropriate device adapter. The MPU performs continuity checking to ensure adequate electrical contact between the adapter and the device.

JTAG Operation

All MAX 9000 devices provide JTAG boundary-scan testing circuitry.

For detailed information on JTAG operation in MAX 9000 devices, refer to *Application Note 39 (JTAG Boundary-Scan Testing in Altera Devices)*.

Programmable Speed/Power Control

MAX 9000 devices offer a power-saving mode that supports low-power operation across user-defined signal paths or the entire device. This feature allows total power dissipation to be reduced by 50% or more, since most logic applications require only a small fraction of all gates to operate at maximum frequency.

The designer can program each individual macrocell in a MAX 9000 EPLD for either high-speed (Turbo Bit on) or low-power (Turbo Bit off) operation. As a result, speed-critical paths in the design can run at high speed, while remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder (t_{LPA}) for the LAB local array delay (t_{LOCAL}).

Design Security

All MAX 9000 EPLDs contain a programmable Security Bit that controls access to the data programmed into the device. When this bit is programmed, a proprietary design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security, since programmed data within EEPROM cells is invisible. The Security Bit that controls this function, as well as all other programmed data, is reset only when the EPLD is erased.

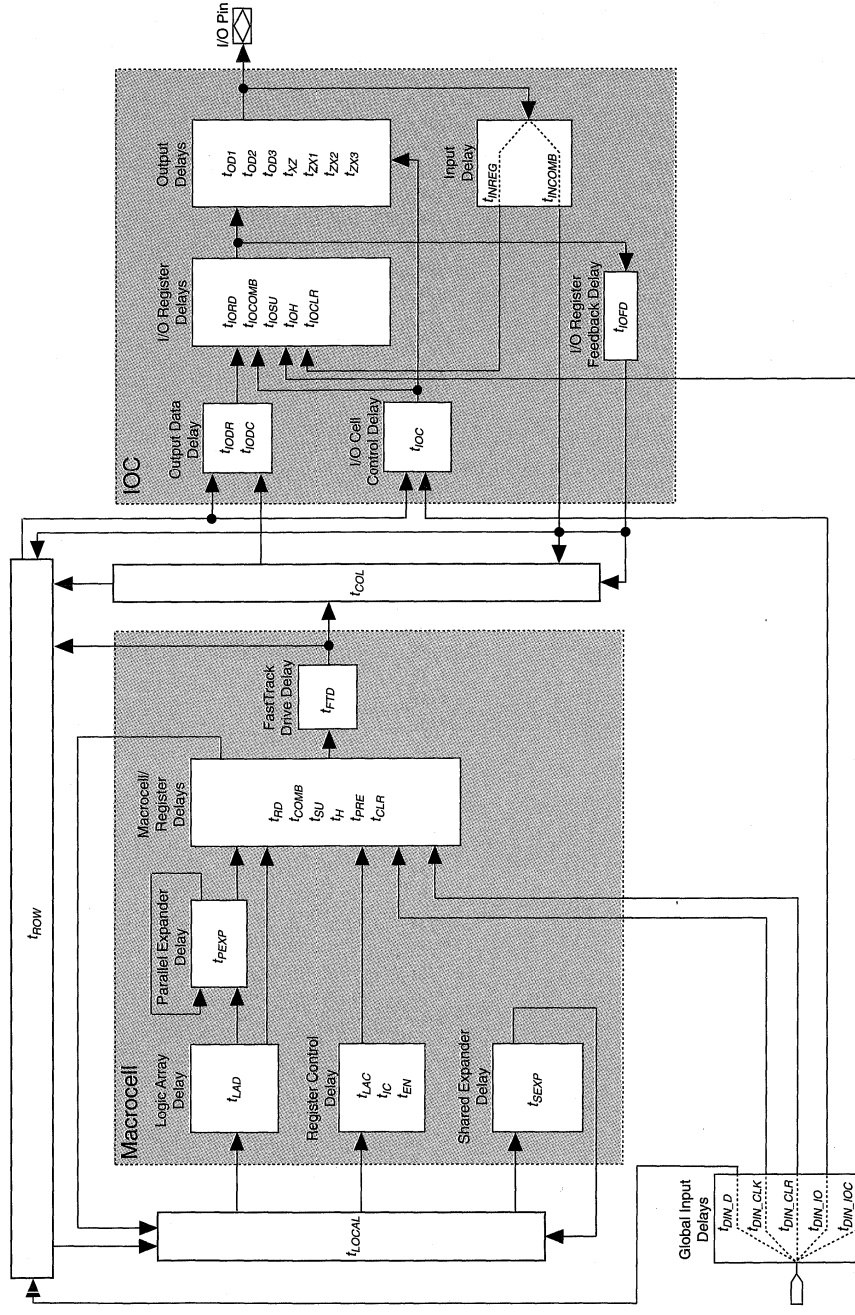
Timing Model

The continuous, high-performance FastTrack Interconnect routing resources ensure predictable performance and accurate simulation analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and hence have unpredictable performance. Timing simulation and delay prediction are available with the MAX+PLUS II Simulator and Timing Analyzer, or with industry-standard EDA tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time prediction, and system-level performance analysis.

The MAX 9000 timing model in Figure 11 shows the delays that correspond to various paths and functions in the circuit. This model contains three distinct parts: the macrocell; the IOC; and the interconnect, including the row and column FastTrack Interconnect and LAB local array paths. Each parameter shown in Figure 11 is expressed as a worst-case value in the "Internal Timing Characteristics" tables in this data sheet. Hand-calculations that use the MAX 9000 timing model and these timing parameters can be used to estimate MAX 9000 device performance.

For more information on calculating MAX 9000 timing delays, go to *Application Brief 144 (Understanding MAX 9000 Timing)* in this data book.

Figure 11. MAX 9000 Timing Model

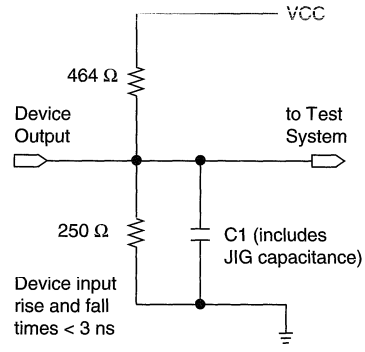


Generic Testing

MAX 9000 EPLDs are fully functionally tested and guaranteed. Complete testing of each programmable EEPROM bit and all logic functionality ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in Figure 12. Test patterns can be used and then erased during the early stages of the production flow.

Figure 12. MAX 9000 AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold test must not be performed under AC conditions. Large-amplitude, fast ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result.



QFP Carrier & Development Socket

MAX 9000 devices in QFP packages with 100 or more pins are shipped in special plastic carriers to protect the fragile QFP leads. The carrier is used with a prototype development socket and special programming hardware available from Altera. This carrier technology makes it possible to program, test, erase, and reprogram a device without exposing the leads to mechanical stress.

For detailed information, go to the *QFP Carrier & Development Socket Data Sheet* in this data book.

Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*Note (2)*	–2.0	7.0	V
V_{PP}	ISP programming voltage	With respect to GND, *Note (2)*	–2.0	7.0	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers		4.75	5.25	V
V_{CCIO}	Supply voltage for output drivers	5.0-V operation	4.75	5.25	V
		3.3-V operation	3.00	3.60	V
V_{PP}	ISP programming voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CCINT}	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C

DC Operating Conditions *Notes (3), (4)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage		2.0	V_{CCINT} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC		0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND, *Note (5)*	–10	10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40	40	µA

Capacitance *Note (6)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{DIN1}	Dedicated input capacitance	V_{IN} = 0 V, f = 1.0 MHz		25	pF
C_{DIN2}	Dedicated input capacitance	V_{IN} = 0 V, f = 1.0 MHz		25	pF
C_{DIN3}	Dedicated input capacitance	V_{IN} = 0 V, f = 1.0 MHz		30	pF
C_{DIN4}	Dedicated input capacitance	V_{IN} = 0 V, f = 1.0 MHz		20	pF
$C_{I/O}$	I/O pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		15	pF

Typical I_{CC} Supply Current Values

Symbol	Parameter	Conditions	EPM9320	EPM9400	EPM9480	EPM9560	Unit
I_{CC1}	V_{CC} supply current (low-power mode, standby, typical)	V_I = GND, No load, *Note (7)*	90	110	130	160	mA

Notes to tables:

(1) See *Operating Requirements for Altera Devices* in this data book.

(2) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.

(3) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.

(4) Operating conditions: V_{CCINT} = 5.0 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CCINT} = 5.0 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CCINT} = 5.0 V ± 10%, T_C = –55° C to 125° C for military use.
V_{CCIO} = 5.0 V ± 5% for 5.0-V operation.
V_{CCIO} = 3.3 V ± 10% for 3.3-V operation.

(5) JTAG input leakage typically –60 µA.

(6) Capacitance measured at 25° C. Sample-tested only.

(7) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB. I_{CC} measured at 0° C.

Figure 13 shows typical output drive characteristics for MAX 9000 devices with 5.0-V V_{CCIO}.

Figure 13. Output Drive Characteristics with 5.0-V V_{CCIO}

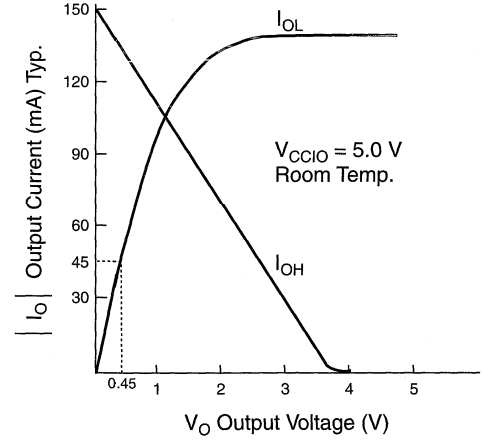
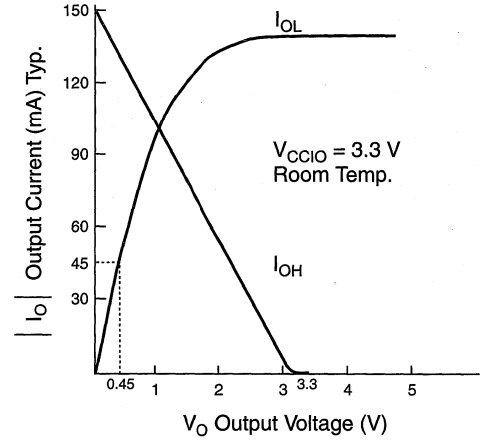


Figure 14 shows typical output drive characteristics for MAX 9000 devices with 3.3-V V_{CCIO}.

Figure 14. Output Drive Characteristics with 3.3-V V_{CCIO}



MAX 9000 External Timing Characteristics *Note (1)*

			-12 Speed Grade		-15 Speed Grade		-20 Speed Grade		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Row I/O pin input to row I/O pin output	C1 = 35 pF, *Note (2)*		12		15		20	ns
t_{PD2}	Column I/O pin input to column I/O pin output	EPM9320, C1 = 35 pF		12.4		16.0		23.0	ns
		EPM9400, C1 = 35 pF		12.6		16.2		23.2	ns
		EPM9480, C1 = 35 pF		12.8		16.9		23.4	ns
		EPM9560, C1 = 35 pF		13.0		16.6		23.6	ns
t_{FSU}	Global clock setup time for I/O cell		3.0		5.0		6.0		ns
t_{FH}	Global clock hold time for I/O cell		0.0		0.0		0.0		ns
t_{FCO}	Global clock to I/O cell output delay	C1 = 35 pF		6.0		7.0		8.5	ns
t_{CNT}	Minimum internal global clock period	*Note (3)*		8.0		8.5		10.0	ns
f_{CNT}	Maximum internal global clock frequency	*Note (3)*	125.0		117.6		100.0		MHz

MAX 9000 Internal Timing Characteristics *Note (1)*

Macrocell Delays			-12 Speed Grade		-15 Speed Grade		-20 Speed Grade		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{LAD}	Logic array delay					4		4.5	ns
t_{LAC}	Logic control array delay					4		4.5	ns
t_{IC}	Array clock delay					4		4.5	ns
t_{EN}	Register enable time					4		4.5	ns
t_{SEXP}	Shared expander delay					5		7.5	ns
t_{PEXP}	Parallel expander delay					1		2	ns
t_{RD}	Register delay					1		1	ns
t_{COMB}	Combinatorial delay					1		1	ns
t_{SU}	Register setup time				3		4		ns
t_{H}	Register hold time				3.5		4.5		ns
t_{PRE}	Register preset time					4		4.5	ns
t_{CLR}	Register clear time					4		4.5	ns
t_{FTD}	FastTrack drive delay					1		2.0	ns
t_{LPA}	Low-power adder	*Note (4)*				15		20	ns

IOC Delays			-12 Speed Grade		-15 Speed Grade		-20 Speed Grade		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IODR}	I/O row output data delay					0.2		1.5	ns
t_{IODC}	I/O column output data delay					0.2		1.5	ns
t_{IOC}	I/O control delay					1		2	ns
t_{IORD}	I/O register Clock-to-output delay					1		1.5	ns
t_{IOCOMB}	I/O combinatorial delay					1		1.5	ns
t_{IOSU}	I/O register setup time before Clock				4		5		ns
t_{IOH}	I/O register hold time after Clock				1		1		ns
t_{IOCLR}	I/O register clear delay					3		3	ns
t_{IOFD}	I/O register feedback delay					0		0.5	ns
t_{INREG}	I/O input pad and buffer to I/O register delay					4.5		5.5	ns
t_{INCOMB}	I/O input pad and buffer to row and column delay					2		2.5	ns
t_{OD1}	Output buffer and pad delay, Slow slew rate = off, V_{CCIO} = 5.0 V	*Note (5)*				2.5		2.5	ns
t_{OD2}	Output buffer and pad delay, Slow slew rate = off, V_{CCIO} = 3.3 V	*Note (6)*				3.5		3.5	ns
t_{OD3}	Output buffer and pad delay, Slow slew rate = on, V_{CCIO} = 5.0 V or 3.3 V	*Notes (5), (6)*				6.5		6.5	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF				2.5		2.5	ns
t_{ZX1}	Output buffer enable delay, Slow slew rate = off, V_{CCIO} = 5.0 V	C1 = 35 pF				2.5		2.5	ns
t_{ZX2}	Output buffer enable delay, Slow slew rate = off, V_{CCIO} = 3.3V	C1 = 35 pF				3.5		3.5	ns
t_{ZX3}	Output buffer enable delay, Slow slew rate = on, V_{CCIO} = 3.3 V or 5.0 V	C1 = 35 pF				6.5		6.5	ns

Interconnect Delays			-12 Speed Grade		-15 Speed Grade		-20 Speed Grade		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Min	Max	Unit
t_{LOCAL}	LAB local array delay					0.5		0.5	ns
t_{ROW}	FastTrack row delay	*Note (7)*				1.4		2	ns
t_{COL}	FastTrack column delay	*Note (7)*				1.7		3	ns
t_{DIN_D}	Dedicated input data delay					4.5		5	ns
t_{DIN_CLK}	Dedicated input Clock delay					3.5		4	ns
t_{DIN_CLR}	Dedicated input Clear delay					5		5.5	ns
t_{DIN_IOC}	Dedicated input I/O register Clock delay					3.5		4.5	ns
t_{DIN_IO}	Dedicated input I/O register Control delay					6		6.5	ns

Notes to tables:

(1) Operating conditions: $V_{CCINT} = 5.0\ V \pm 5\%$, $V_{CCIO} = 5.0\ V \pm 5\%$ (except where noted).
(2) Go to *Application Brief 144 (Understanding MAX 9000 Timing)* in this data book for more information on test conditions for t_{PD1} and t_{PD2} delays.
(3) Measured with a 16-bit loadable, enabled, up/down counter programmed in each LAB.
(4) The t_{LPA} parameter must be added to the t_{LOCAL} parameter for macrocells running in low-power mode.
(5) Operating conditions: $V_{CCIO} = 5.0\ V \pm 5\%$.
(6) Operating conditions: $V_{CCIO} = 3.3\ V \pm 10\%$.
(7) The t_{ROW} and t_{COL} delays are worst-case values for typical applications. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.

Calculating the Supply Current

Supply current (I_{CC} in mA) versus frequency (f_{MAX} in MHz) for MAX 9000 devices is calculated with the following equation:

$$I_{CC} = I_{CCOUTPUT} + I_{CCACTIVE}$$

The $I_{CCOUTPUT}$ value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Operating Requirements for Altera Devices* in this data book. The $I_{CCACTIVE}$ value depends on the switching frequency and the application logic.

The $I_{CCACTIVE}$ value is calculated with the following equation:

$$I_{CC} = (A \times MC_{TON}) + (B \times MC_{TOFF}) + (C \times MC) \times f_{MAX}$$

The parameters for this equation are:

MC_{TON} = Number of macrocells used with Turbo Bit on
MC_{TOFF} = Number of macrocells used with Turbo Bit off
MC = Total number of macrocells used in the design ($MC_{TON} + MC_{TOFF}$)
f_{MAX} = Highest Clock frequency to the device

Table 7 lists the values for the constants A, B, and C.

Table 7. MAX 9000 I_{CC} Equation Constants *Note (1)*

Device	Constant A	Constant B	Constant C
EPM9320	0.59	0.28	0.013
EPM9400	0.59	0.28	0.013
EPM9480	0.59	0.28	0.013
EPM9560	0.59	0.28	0.013

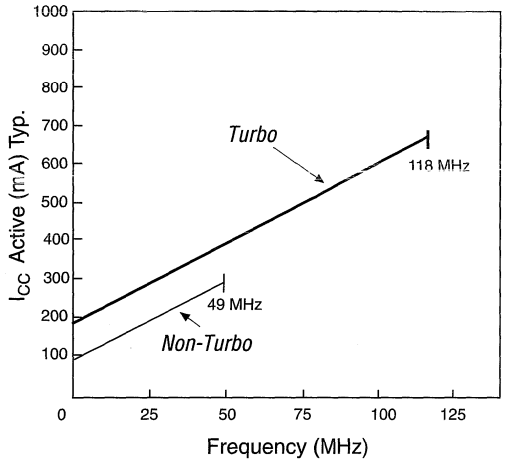
Note:
(1) This information is preliminary.

This calculation provides an I_{CC} estimate based on typical conditions using a typical pattern of a 16-bit, loadable, enabled, up/down counter in each LAB with no output load. Actual I_{CC} should be verified during operation, since the measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

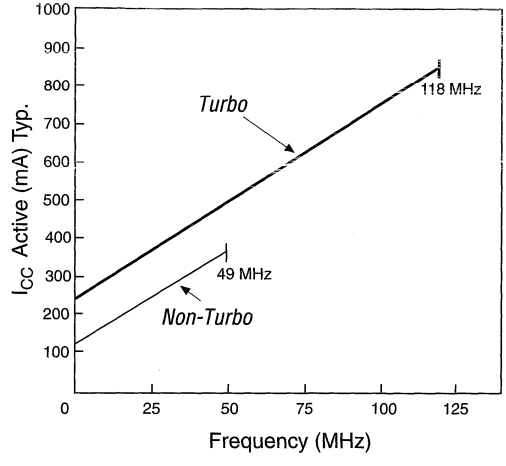
Figure 15 shows typical supply current versus frequency for the MAX 9000 devices listed in Table 7.

Figure 15. I_{CC} vs. Frequency for MAX 9000 Devices

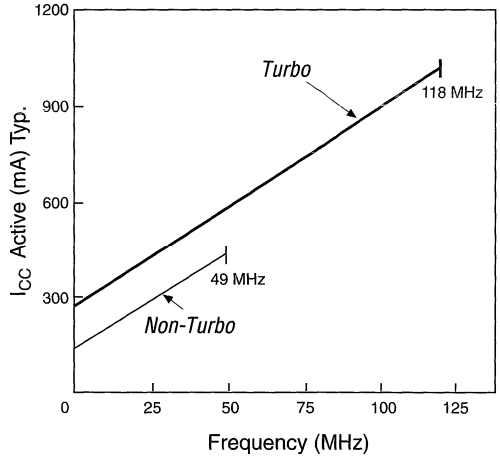
EPM9320



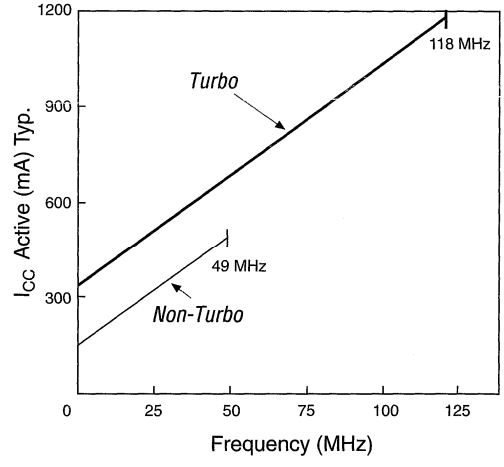
EPM9400



EPM9480



EPM9560



Device Pin-Outs

Tables 8, 9, 10, and 11 show the pin names and numbers for the EPM9320, EPM9400, EPM9480, and EPM9560 packages, respectively.

Table 8. EPM9320 Dedicated Pin-Outs

Dedicated Pin	84-Pin PLCC *(1)*	160-Pin RQFP	208-Pin RQFP	280-Pin PGA
DIN1 (GCLK1)	1	140	182	V10
DIN2 (GCLK2)	84	141	183	U10
DIN3 (GCLR)	13	116	153	V17
DIN4 (GOE)	72	5	4	W2
TCK	43	60	78	A9
TMS	55	36	49	D6
TDI	42	61	79	C11
TDO	30	85	108	A18
GND	6, 18, 24, 25, 48, 61, 67, 70	8, 14, 21, 27, 34, 50, 66, 80, 94, 95, 107, 108, 115, 130, 146, 160	14, 20, 24, 31, 35, 41, 42, 43, 44, 46, 47, 66, 85, 102, 110, 113, 114, 115, 116, 118, 121, 122, 132, 133, 143, 152, 170, 189, 206	D4, D5, D16, E4, E5, E6, E15, E16, F5, F15, G5, G15, H5, H15, J5, J15, K5, K15, L5, L15, M5, M15, N5, N15, P4, P5, P15, P16, R4, R5, R15, R16, T4, T5, T16
VCCINT (5.0 V only)	14, 21, 28, 57, 64, 71	7, 20, 33, 88, 101, 114	10, 19, 30, 45, 112, 128, 139, 148	D15, E8, E10, E12, E14, R7, R9, R11, R13, R14, T14
VCCIO (3.3 or 5.0 V)	15, 37, 60, 79	6, 15, 28, 41, 55, 71, 87, 100, 113, 121, 135, 151	5, 25, 36, 55, 72, 91, 111, 127, 138, 159, 176, 195	D14, E7, E9, E11, E13, R6, R8, R10, R12, T13, T15
No Connect (N.C.)	29	86	6, 7, 8, 9, 11, 12, 13, 15, 16, 17, 18, 109, 140, 141, 142, 144, 145, 146, 147, 149, 150, 151	B6, K19, L2, L4, L18, L19, M1, M2, M3, M4, M16, M17, M18, M19, N1, N2, N3, N4, N16, N17, N18, N19, P1, P2, P3, P17, P18, P19, R1, R2, R3, R17, R18, R19, T1, T2, T3, T17, T18, T19, U1, U2, U3, U17, U18, U19, V1, V2, V19, W1
VPP, *Note (2)*	56	35	48	C4

Notes:

(1) Perform a complete thermal analysis before committing a design to this device package. See *Operating Requirements for Altera Devices* in this data book for more information.

(2) During in-system programming, each device's VPP pin must be connected to the 5.0-V power supply. During normal device operation, the VPP pin is pulled up internally and can be connected to the 5.0-V supply or left unconnected.

Table 9. EPM9400 Dedicated Pin-Outs

Dedicated Pin	84-Pin PLCC *(2)*	208-Pin RQFP	240-Pin RQFP	280-Pin PGA
DIN1 (GCLK1)	2	182	210	V10
DIN2 (GCLK2)	1	183	211	U10
DIN3 (GCLR)	12	153	187	V17
DIN4 (GOE)	74	4	234	W2
TCK	43	78	91	A9
TMS	54	49	68	D6
TDI	42	79	92	C11
TDO	31	108	114	A18
GND	6, 13, 20, 26, 27, 47, 60, 66, 69, 73	14, 20, 24, 31, 35, 41, 42, 43, 44, 46, 47, 66, 85, 102, 110, 113, 114, 115, 116, 118, 121, 122, 132, 133, 143, 152, 170, 189, 206	5, 14, 25, 34, 45, 54, 65, 66, 81, 96, 110, 115, 126, 127, 146, 147, 166, 167, 186, 200, 216, 229	D4, D5, D16, E4, E5, E6, E15, E16, F5, F15, G5, G15, H5, H15, J5, J15, K5, K15, L5, L15, M5, M15, N5, N15, P4, P5, P15, P16, R4, R5, R15, R16, T4, T5, T16
VCCINT (5.0 V only)	16, 23, 30, 56, 63, 70	10, 19, 30, 45, 112, 128, 139, 148	4, 24, 44, 64, 117, 137, 157, 177	D15, E8, E10, E12, E14, R7, R9, R11, R13, R14, T14
VCCIO (3.3 or 5.0 V)	17, 37, 59, 80	5, 25, 36, 55, 72, 91, 111, 127, 138, 159, 176, 195	15, 35, 55, 73, 86, 101, 116, 136, 156, 176, 192, 205, 220, 235	D14, E7, E9, E11, E13, R6, R8, R10, R12, T13, T15
No Connect (N.C.)	–	6, 7, 8, 9, 11, 12, 13, 109, 144, 145, 146, 147, 149, 150, 151	1, 2, 3, 6, 7, 8, 9, 10, 11, 12, 13, 168, 169, 170, 171, 172, 173, 174, 175, 178, 179, 180, 181, 182, 183, 184, 185, 236, 237, 238, 239, 240	B6, M18, N3, N4, N18, N19, P1, P2, P3, P17, P18, P19, R1, R2, R3, R17, R18, R19, T1, T2, T3, T17, T18, T19, U1, U2, U3, U17, U18, U19, V1, V2, V19, W1
VPP, *Note (2)*	55	48	67	C4

Notes:

(1) Perform a complete thermal analysis before committing a design to this device package. See *Operating Requirements for Altera Devices* in this data book for more information.

(2) During in-system programming, each device's VPP pin must be connected to the 5.0-V power supply. During normal device operation, the VPP pin is pulled up internally and can be connected to the 5.0-V supply or left unconnected.

Table 10. EPM9480 Dedicated Pin-Outs

Dedicated Pin	160-Pin RQFP	208-Pin RQFP	240-Pin RQFP	280-Pin PGA
DIN1 (GCLK1)	140	182	210	V10
DIN2 (GCLK2)	141	183	211	U10
DIN3 (GCLR)	120	153	187	V17
DIN4 (GOE)	1	4	234	W2
TCK	60	78	91	A9
TMS	40	49	68	D6
TDI	61	79	92	C11
TDO	82	108	114	A18
GND	4, 9, 20, 26, 31, 38, 52, 66, 77, 83, 89, 90, 101, 111, 112, 119, 131, 145, 157	14, 20, 24, 31, 35, 41, 42, 43, 44, 46, 47, 66, 85, 102, 110, 113, 114, 115, 116, 118, 121, 122, 132, 133, 143, 152, 170, 189, 206	5, 14, 25, 34, 45, 54, 65, 66, 81, 96, 110, 115, 126, 127, 146, 147, 166, 167, 186, 200, 216, 229	D4, D5, D16, E4, E5, E6, E15, E16, F5, F15, G5, G15, H5, H15, J5, J15, K5, K15, L5, L15, M5, M15, N5, N15, P4, P5, P15, P16, R4, R5, R15, R16, T4, T5, T16
VCCINT (5.0 V only)	3, 15, 25, 37, 84, 96, 106, 118	10, 19, 30, 45, 112, 128, 139, 148	4, 24, 44, 64, 117, 137, 157, 177	D15, E8, E10, E12, E14, R7, R9, R11, R13, R14, T14
VCCIO (3.3 or 5.0 V)	2, 10, 32, 44, 56, 70, 95, 117, 124, 136, 149	5, 25, 36, 55, 72, 91, 111, 127, 138, 159, 176, 195	15, 35, 55, 73, 86, 101, 116, 136, 156, 176, 192, 205, 220, 235	D14, E7, E9, E11, E13, R6, R8, R10, R12, T13, T15
No Connect (N.C.)	–	6, 7, 8, 9, 109, 149, 150, 151	1, 2, 3, 178, 179, 180, 181, 182, 183, 184, 185, 236, 237, 238, 239, 240	B6, R2, R3, R19, T3, T17, T18, T19, U1, U2, U3, U17, U18, U19, V1, V2, V19, W1
VPP, *Note (1)*	39	48	67	C4

Note:

(1) During in-system programming, each device's VPP pin must be connected to the 5.0-V power supply. During normal device operation, the VPP pin is pulled up internally and can be connected to the 5.0-V supply or left unconnected.

Table 11. EPM9560 Dedicated Pin-Outs

Dedicated Pin	208-Pin CQFP	240-Pin RQFP	280-Pin PGA	304-Pin RQFP
DIN1 (GCLK1)	182	210	V10	266
DIN2 (GCLK2)	183	211	U10	267
DIN3 (GCLR)	153	187	V17	237
DIN4 (GOE)	4	234	W2	296
TCK	78	91	A9	114
TMS	49	68	D6	85
TDI	79	92	C11	115
TDO	108	114	A18	144
GND	14, 20, 24, 31, 35, 41, 42, 43, 44, 46, 47, 66, 85, 102, 110, 113, 114, 115, 116, 118, 121, 122, 132, 133, 143, 152, 170, 189, 206	5, 14, 25, 34, 45, 54, 65, 66, 81, 96, 110, 115, 126, 127, 146, 147, 166, 167, 186, 200, 216, 229	D4, D5, D16, E4, E5, E6, E15, E16, F5, F15, G5, G15, H5, H15, J5, J15, K5, K15, L5, L15, M5, M15, N5, N15, P4, P5, P15, P16, R4, R5, R15, R16, T4, T5, T16	13, 22, 33, 42, 53, 62, 73, 74, 102, 121, 138, 155, 166, 167, 186, 187, 206, 207, 226, 254, 273, 290
VCCINT (5.0 V only)	10, 19, 30, 45, 112, 128, 139, 148	4, 24, 44, 64, 117, 137, 157, 177	D15, E8, E10, E12, E14, R7, R9, R11, R13, R14, T14	12, 32, 52, 72, 157, 177, 197, 217
VCCIO (3.3 or 5.0 V)	5, 25, 36, 55, 72, 91, 111, 127, 138, 159, 176, 195	15, 35, 55, 73, 86, 101, 116, 136, 156, 176, 192, 205, 220, 235	D14, E7, E9, E11, E13, R6, R8, R10, R12, T13, T15	3, 23, 43, 63, 91, 108, 127, 156, 176, 196, 216, 243, 260, 279
No Connect (N.C.)	109	–	B6, W1	1, 2, 76, 77, 78, 79, 80, 81, 82, 83, 84, 145, 146, 147, 148, 149, 150, 151, 152, 153, 154, 227, 228, 229, 230, 231, 232, 233, 234, 235, 236, 297, 298, 299, 300, 301, 302, 303, 304
VPP, *Note (1)*	48	67	C4	75

Note:

(1) During in-system programming, each device's VPP pin must be connected to the 5.0-V power supply. During normal device operation, the VPP pin is pulled up internally and can be connected to the 5.0-V supply or left unconnected.

March 1995

MAX 7000 Programmable Logic Device Family

MAX 7000S Programmable Logic Device Family


ALTERA
MAX
EPM7192EQC160
ALTERA
MAX
EPM7192EGC160
ALTERA
MAX
EPM7256EGC192
ALTERA
MAX
EPM7256BRC208

Includes MAX 7000E

MAX 7000

Programmable Logic Device Family

March 1995, ver. 3 — Data Sheet

Features...

- High-performance CMOS EEPROM devices based on second-generation Multiple Array MatriX (MAX) architecture
- Complete EPLD family with logic densities ranging from 600 usable (1,200 available) gates to 5,000 usable (10,000 available) gates (see Table 1)
- 5-ns pin-to-pin logic delays with up to 178.6-MHz counter frequencies (including interconnect)
- PCI-compliant -5, -6, -7, -10P, and -12P speed grades
- Programmable flipflops with individual Clear, Preset, Clock, and Clock Enable controls
- Programmable power-saving mode for 50% or greater power reduction in each macrocell
- Configurable expander product-term distribution allowing up to 32 product terms per macrocell
- 44 to 208 pins available in J-lead (PLCC), pin-grid array (PGA), quad flat pack (QFP), and 1-mm thin quad flat pack (TQFP) packages
- Programmable Security Bit for total protection of proprietary designs
- 3.3-V or 5.0-V operation
  - Full 3.3-V EPM7032V
  - 3.3-V or 5.0-V I/O on all devices (except 44-pin devices)

Table 1. MAX 7000 Device Features

Feature	EPM7032	EPM7032V	EPM7064	EPM7096	EPM7128E	EPM7160E	EPM7192E	EPM7256E
Available Gates	1,200	1,200	2,500	3,600	5,000	6,400	7,500	10,000
Usable Gates	600	600	1,250	1,800	2,500	3,200	3,750	5,000
Macrocells	32	32	64	96	128	160	192	256
Maximum User I/O	36	36	68	76	100	104	124	164
t_{PD} (ns)	5	12	6	6	7.5	7.5	10	10
t_{SU} (ns)	4	10	5	5	6	6	7	7
t_{FSU} (ns)	–	–	–	–	3	3	3	3
t_{CO1} (ns)	3.5	7	4	4	4.5	4.5	5	5
f_{CNT} (MHz)	178.6	90.9	151.5	151.5	125	125	100	100

...and More Features

- Enhanced features available in MAX 7000E devices, the higher-density members of the MAX 7000 family
  - Six pin- or logic-driven Output Enable signals
  - Two global Clock signals with optional inversion
  - Enhanced interconnect resources for improved routability
  - Fast input setup times provided by a dedicated path from I/O pin to macrocell registers
  - Programmable output slew-rate control
- Software design support featuring Altera's MAX+PLUS II development system on 486- and Pentium-based PCs and Sun SPARCstation, HP 9000 Series 700, and IBM RISC System/6000 workstations
- Additional design entry and simulation support provided by EDIF, Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Data I/O, Exemplar, Intergraph, Mentor Graphics, OrCAD, Synopsys, and Viewlogic
- Programming support with Altera's Master Programming Unit (MPU) and programming hardware from other manufacturers

General Description

The MAX 7000 family of high-density, high-performance CMOS devices is based on Altera's second-generation MAX architecture. Fabricated with advanced EEPROM-based CMOS technology, the MAX 7000 family provides 600 to 5,000 usable gates, pin-to-pin delays as fast as 5 ns, and counter speeds of up to 178.6 MHz. The –5, –6, –7, –10P, and -12P speed grades comply with the *PCI Local Bus Specification*. See Table 2 for available speed grades.

Table 2. MAX 7000 Speed Grades

Device	Speed Grade									
	–5	–6	–7	–10P	–10	12P	–12	–15	–15T	–20
EPM7032	✓ (1)	✓	✓		✓		✓	✓	✓	
EPM7032V							✓	✓		✓
EPM7064		✓ (1)	✓		✓		✓	✓		
EPM7096		✓ (1)	✓		✓		✓	✓		
EPM7128E			✓ (1)	✓	✓		✓	✓		✓
EPM7160E			✓ (1)	✓	✓		✓	✓		✓
EPM7192E				✓ (1)	✓ (1)	✓ (1)	✓	✓		✓
EPM7256E				✓ (1)	✓ (1)	✓ (1)	✓	✓		✓

Note:
(1) This information is preliminary. Contact Altera Marketing at (408) 894-7104 for product availability.

The higher-density members of the MAX 7000 family—called MAX 7000E devices—include the EPM7128E, EPM7160E, EPM7192E, and EPM7256E devices. (MAX 7000E device names end with the letter E.) These devices have several enhanced features: additional global clocking, additional Output Enable controls, enhanced interconnect resources, fast input registers, and a programmable slew rate.

The MAX 7000 architecture supports 100% TTL emulation and high-density integration of SSI, MSI, and LSI logic functions. It easily integrates multiple programmable logic devices ranging from PALs, GALs, and 22V10s to MACH, pLSI, and FPGA devices. With speed, density, and I/O resources comparable to commonly used masked gate arrays, MAX 7000 devices are also ideal for gate-array prototyping. MAX 7000 devices are available in a wide range of packages, including plastic J-lead chip carrier (PLCC), ceramic pin-grid array (PGA), plastic quad flat pack (PQFP), power quad flat pack (RQFP), and the 1-mm thin quad flat pack (TQFP). See Table 3.

Table 3. MAX 7000 Maximum User I/O Pins *Note (1)*

Device	44-Pin PLCC	44-Pin PQFP	44-Pin TQFP	68-Pin PLCC	84-Pin PLCC	100-Pin PQFP	160-Pin PQFP	160-Pin PGA	192-Pin PGA	208-Pin RQFP
EPM7032	36	36	36							
EPM7032V	36		36							
EPM7064	36		36	52	68	68				
EPM7096				52	64	76				
EPM7128E					68	84	100			
EPM7160E					64	84	104			
EPM7192E							124	124		
EPM7256E							132 *(2)*		164	164

Notes:
(1) Contact Altera for up-to-date information on available device package options.
(2) Perform a complete thermal analysis before committing a design to this device package. See *Operating Requirements for Altera Devices* in this data book for more information.

MAX 7000 devices use CMOS EEPROM cells to implement logic functions. The user-configurable MAX 7000 architecture accommodates a variety of independent combinatorial and sequential logic functions. The devices can be reprogrammed for quick and efficient iterations during design development and debug cycles, and are guaranteed for 100 program and erase cycles.

MAX 7000 devices contain from 32 to 256 macrocells that are combined into groups of 16 macrocells, called Logic Array Blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register with independently programmable Clock, Clock Enable, Clear, and Preset functions. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and high-speed parallel expander product terms to provide up to 32 product terms per macrocell.

The MAX 7000 family provides programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power while the remaining portions run at reduced speed/low power. This speed/power optimization feature enables the designer to configure one or more macrocells to operate at 50% or lower power while adding only a nominal timing delay. MAX 7000E devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching. The output drivers of all MAX 7000 devices (except 44-pin devices) can be set for either 3.3-V or 5.0-V operation, allowing MAX 7000 devices to be used in mixed-voltage systems.

The MAX 7000 family is supported by Altera's MAX+PLUS II development system, a single, integrated package that offers schematic, text—including the Altera Hardware Description Language (AHDL)—and waveform design entry; compilation and logic synthesis; simulation and timing analysis; and device programming. MAX+PLUS II provides EDIF 2 0 0 and 3 0 0, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and workstation-based EDA tools. MAX+PLUS II runs on 486- and Pentium-based PCs, and Sun SPARCstation, HP 9000 Series 700, and IBM RISC System/6000 workstations.

For more information, go to the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* in this data book.

Functional Description

The MAX 7000 architecture includes the following elements:

- Logic Array Blocks
- Macrocells
- Expander product terms (shareable and parallel)
- Programmable Interconnect Array
- I/O control blocks

The MAX 7000 architecture includes four dedicated inputs that can be used as general-purpose inputs or as high-speed, global control signals (Clock, Clear, and two Output Enable signals) for each macrocell and I/O pin. Figure 1 shows the architecture of the EPM7032, EPM7032V, EPM7064, and EPM7096 devices.

Figure 1. Architecture of EPM7032, EPM7032V, EPM7064 & EPM7096 Devices

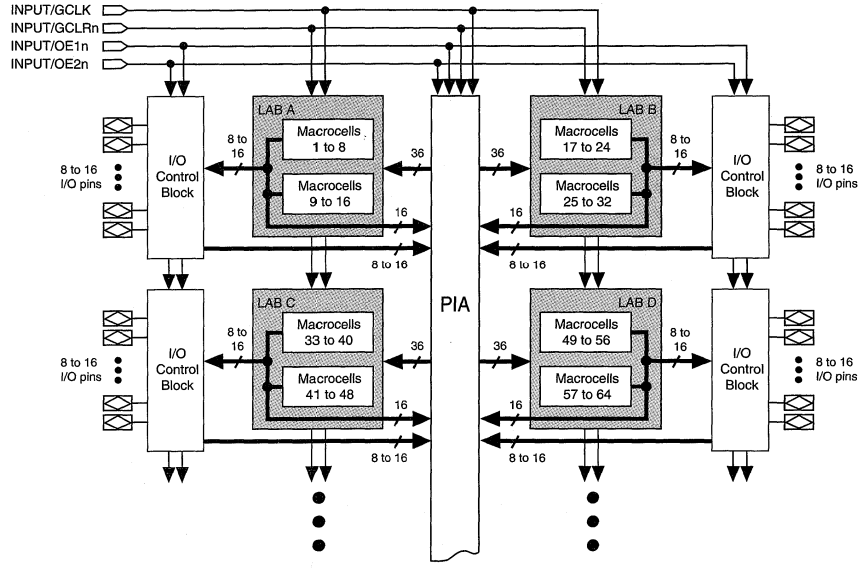
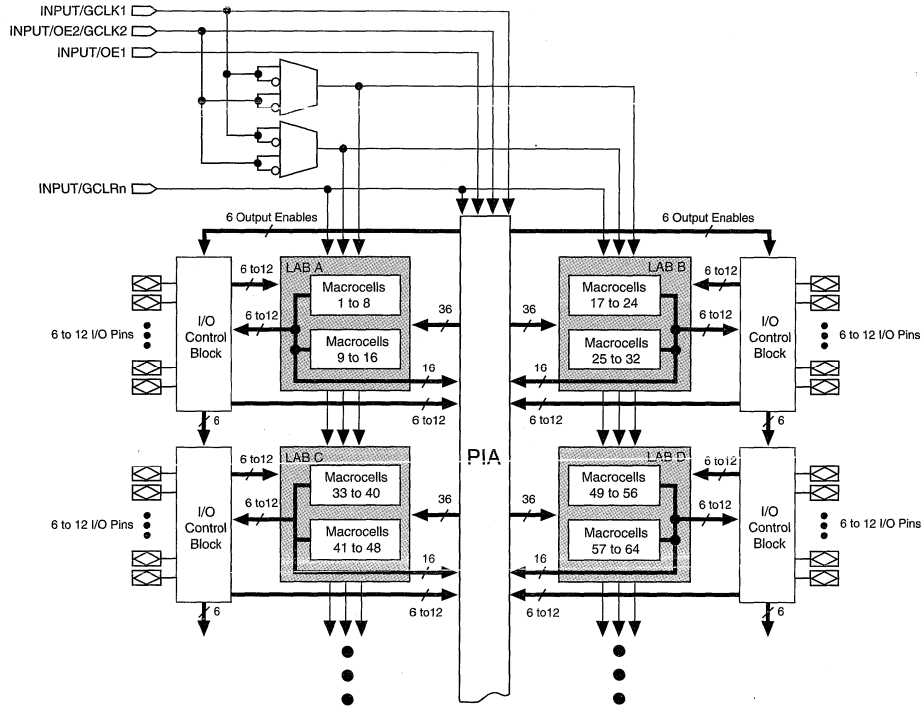


Figure 2 shows the architecture of the EPM7128E, EPM7160E, EPM7192E, and EPM7256E devices.

Figure 2. Architecture of EPM7128E, EPM7160E, EPM7192E & EPM7256E Devices



Logic Array Blocks

The MAX 7000 architecture is based on the linking of high-performance, flexible, logic array modules called Logic Array Blocks (LABs). LABs consist of 16-macrocell arrays, as shown in Figures 1 and 2. Multiple LABs are linked together via the Programmable Interconnect Array (PIA), a global bus that is fed by all dedicated inputs, I/O pins, and macrocells.

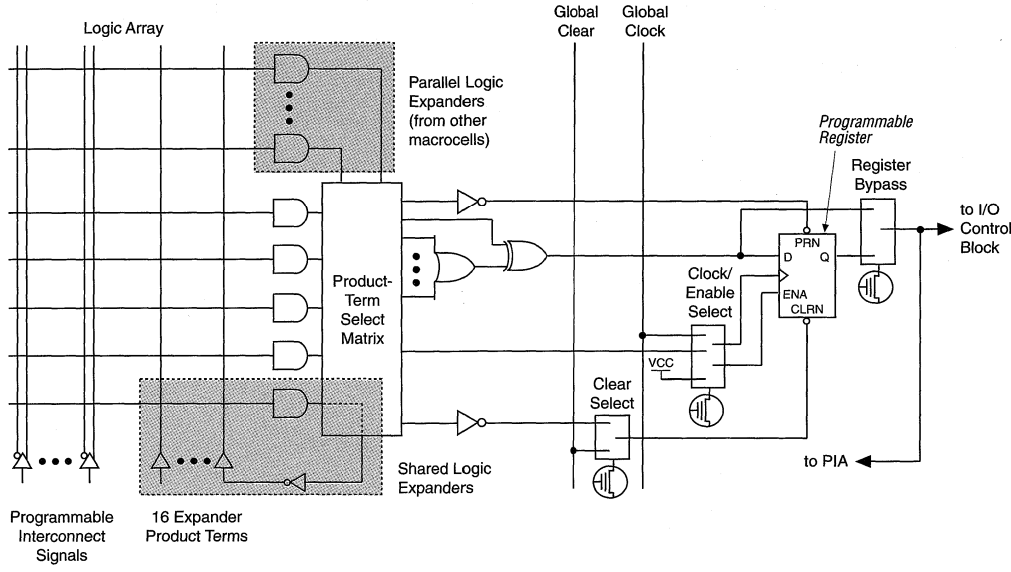
Each LAB is fed by the following signals:

- 36 signals from the PIA that are used for general logic inputs
- Global controls that are used for secondary register functions
- Direct input paths from I/O pins to the registers that are used for fast setup times for the EPM7128E, EPM7160E, EPM7192E, and EPM7256E devices

Macrocells

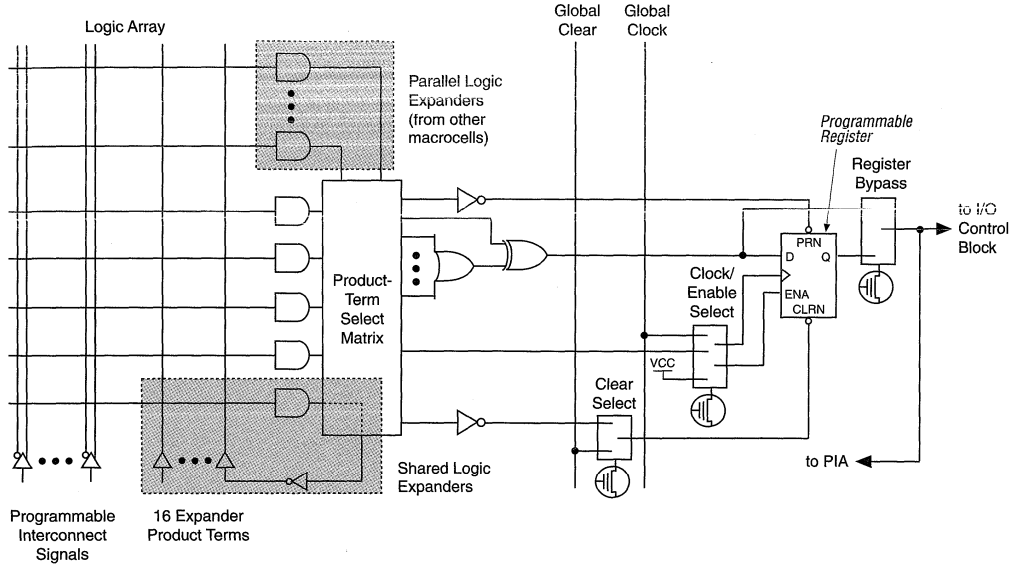
The MAX 7000 macrocell can be individually configured for both sequential and combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register. The macrocell of EPM7032, EPM7032V, EPM7064, and EPM7096 devices is shown in Figure 3.

Figure 3. Macrocell of EPM7032, EPM7032V, EPM7064 & EPM7096 Devices



The macrocell of EPM7128E, EPM7160E, EPM7192E, and EPM7256E devices is shown in Figure 4.

Figure 4. Macrocell of EPM7128E, EPM7160E, EPM7192E & EPM7256E Devices



Combinatorial logic is implemented in the logic array, which provides five product terms per macrocell. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register Clear, Preset, Clock, and Clock Enable control functions. Two kinds of expander product terms ("expanders") are available to supplement macrocell logic resources:

- Shareable expanders, which are inverted product terms that are fed back into the logic array
- Parallel expanders, which are product terms borrowed from adjacent macrocells

MAX+PLUS II automatically optimizes product-term allocation according to the logic requirements of the design.

In registered functions, each macrocell flipflop can be individually programmed to implement D, T, JK, or SR operation with programmable Clock control. If necessary, the flipflop can be bypassed for combinatorial operation. During design entry, the designer specifies the desired flipflop type; MAX+PLUS II then selects the most efficient flipflop operation for each registered function to optimize resource utilization.

Each programmable register can be clocked in three different modes:

- Clocked by a global Clock signal. This mode achieves the fastest Clock-to-output performance.
- Clocked by a global Clock signal and enabled by an active-high Clock Enable. This mode provides an Enable on each flipflop while still achieving the fast Clock-to-output performance of the global Clock.
- Clocked by an array Clock implemented with a product term. In this mode, the flipflop can be clocked by signals from buried macrocells or I/O pins.

In the EPM7032, EPM7032V, EPM7064, and EPM7096 devices, the global Clock signal is available from a dedicated Clock pin, GCLK, as shown in Figure 1. In the EPM7128E, EPM7160E, EPM7192E, and EPM7256E devices, two global Clock signals are available. As shown in Figure 2, these global Clock signals can be the true or the complement of either of the global Clock pins, GCLK1 or GCLK2.

Each register also supports asynchronous Preset and Clear functions. As shown in Figures 3 and 4, the product-term select matrix allocates product terms to control these operations. Although the product-term-driven Preset and Clear of the register are active high, active-low control can be obtained by inverting the signal within the logic array. In addition, each register Clear function can be individually driven by the active-low, dedicated, global Clear pin (GCLRn).

All MAX 7000E I/O pins have a fast input path to a macrocell register. This dedicated path allows a signal to bypass the PIA and combinatorial logic and be clocked to an input D flipflop with an extremely fast (3-ns) input setup time.

Expander Product Terms

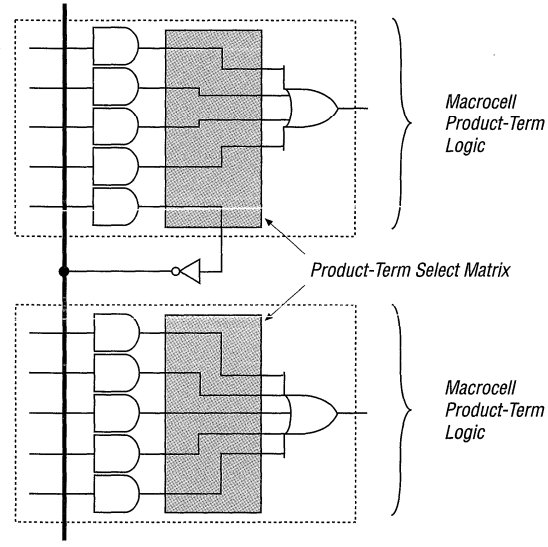
Although most logic functions can be implemented with the five product terms available in each macrocell, some logic functions are more complex and require additional product terms. Another macrocell may be used to supply the required logic resources; however, the MAX 7000 architecture also offers both shareable and parallel expander product terms ("expanders") that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

Shareable Expanders

Each LAB has 16 shareable expanders that can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the logic array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. A small delay (t_{SEXP}) is incurred when shareable expanders are used. Figure 5 shows how shareable expanders can feed multiple macrocells.

Figure 5. Shareable Expanders

Shareable expanders can be shared by any or all macrocells in an LAB.



Parallel Expanders

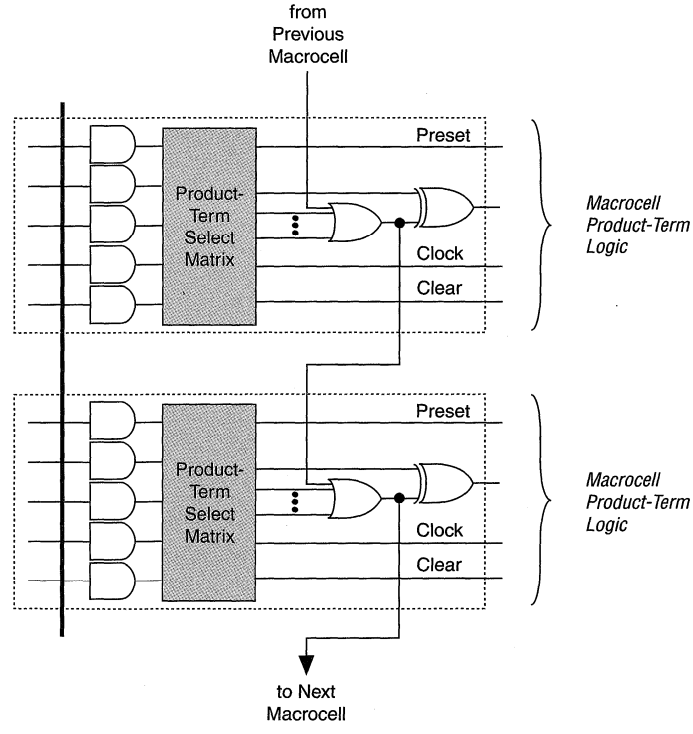
Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with 5 product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The MAX+PLUS II Compiler can automatically allocate up to 3 sets of up to 5 parallel expanders to the macrocells that require additional product terms. Each set of 5 parallel expanders incurs a small, incremental timing delay (t_{PEXP}). For example, if a macrocell requires 14 product terms, the Compiler uses the 5 dedicated product terms within the macrocell and allocates 2 sets of parallel expanders; the first set includes 5 product terms and the second set includes 4 product terms, increasing the total delay by $2 \times t_{PEXP}$.

Two groups of 8 macrocells within each LAB (e.g., macrocells 1 to 8 and 9 to 16) form 2 chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of 8, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them. Figure 6 shows how parallel expanders can be borrowed from a neighboring macrocell.

Figure 6. Parallel Expanders

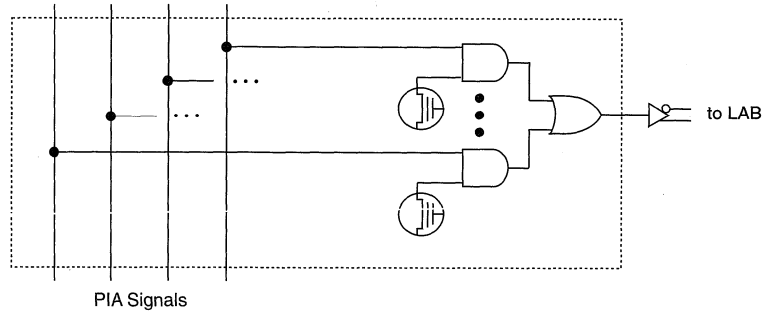
Unused product terms in a macrocell can be allocated to a neighboring macrocell.



Programmable Interconnect Array

Logic is routed between LABs on the Programmable Interconnect Array (PIA). This global bus is a programmable path that connects any signal source to any destination on the device. All MAX 7000 dedicated inputs, I/O pins, and macrocell outputs feed the PIA, which makes them available throughout the entire device. Only the signals required by each LAB are actually routed from the PIA into the LAB. Figure 7 shows how the PIA signals are routed into the LAB. An EEPROM cell controls one input to a 2-input AND gate, which selects a PIA signal to drive into the LAB.

Figure 7. PIA Routing



While the routing delays of channel-based routing schemes in masked or field-programmable gate arrays (FPGAs) are cumulative, variable, and path-dependent, the MAX 7000 PIA has a fixed delay. The PIA thus eliminates skew between signals, and makes timing performance easy to predict.

I/O Control Blocks

The I/O control block allows each I/O pin to be individually configured for input, output, or bidirectional operation. All I/O pins have a tri-state buffer that is individually controlled by one of the global Output Enable signals or directly connected to GND or VCC. Figure 8 shows the I/O control block for the EPM7032, EPM7032V, EPM7064, and EPM7096 devices. The I/O control block has two global Output Enable signals that are driven by two dedicated active-low Output Enable pins (OE1n and OE2n).

Figure 8. I/O Control Block of EPM7032, EPM7032V, EPM7064 & EPM7096 Devices

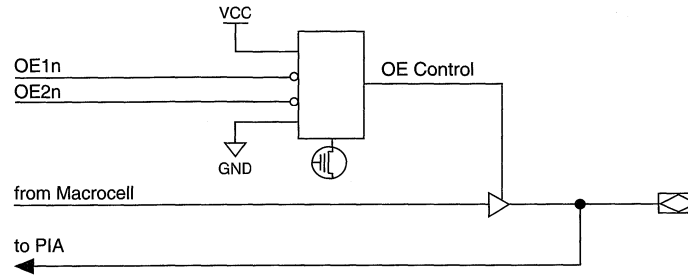
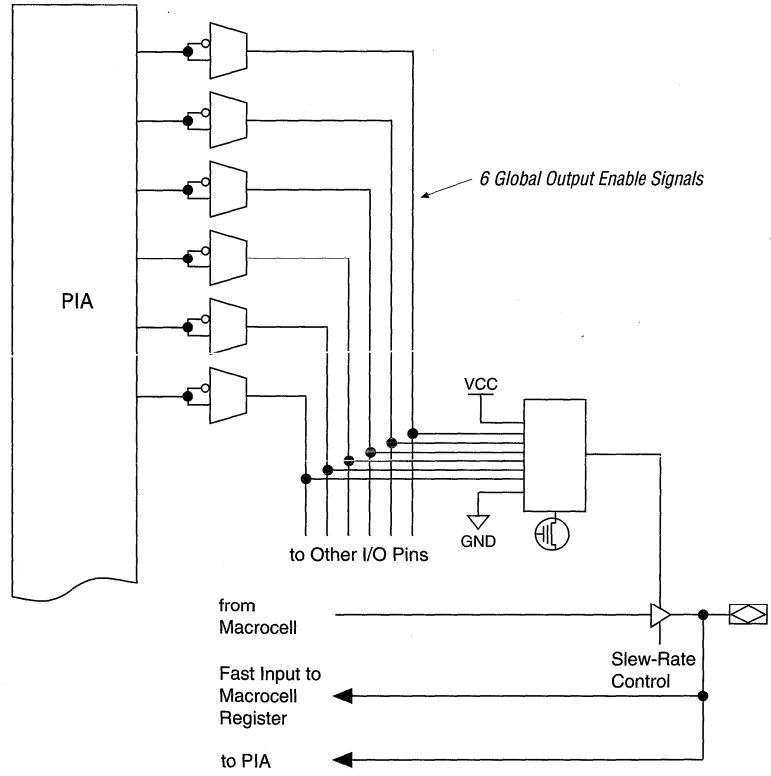


Figure 9 shows the I/O control block of the EPM7128E, EPM7160E, EPM7192E, and EPM7256E devices. The I/O control block has six global Output Enable signals that are driven by the true or complement of two Output Enable signals, a subset of the I/O pins, or a subset of the I/O macrocells.

Figure 9. I/O Control Block of EPM7128E, EPM7160E, EPM7192E & EPM7256E Devices



When the tri-state buffer control is connected to GND, the output is tri-stated (high impedance) and the I/O pin can be used as a dedicated input. When the tri-state buffer control is connected to VCC, the output is enabled.

The MAX 7000 architecture provides dual I/O feedback, in which macrocell and pin feedbacks are independent. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic.

Programmable Speed/Power Control

MAX 7000 devices offer a power-saving mode that supports low-power operation across user-defined signal paths or the entire device. This feature allows total power dissipation to be reduced by 50% or more, since most logic applications require only a small fraction of all gates to operate at maximum frequency.

The designer can program each individual macrocell in a MAX 7000 device for either high-speed (Turbo Bit on) or low-power (Turbo Bit off) operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder (t_{LPA}) for the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{EN}, and t_{SEXP} parameters.

Slew-Rate Control

The output buffer for each MAX 7000E I/O pin has an adjustable output slew rate that can be configured for low-noise or high-speed performance. The slew rate is set to fast when the Turbo Bit is on. A faster slew rate provides very-high-speed transitions, but these fast transitions may introduce more noise transients into the system than a slow slew rate. The fast setting should only be used in speed-critical outputs in systems that are adequately protected against noise. When the Turbo Bit is off, the slew rate is set for low-noise performance, which reduces noise generation and ground bounce.

3.3-V or 5.0-V I/O Operation

All MAX 7000 devices, except 44-pin devices, can be set for 3.3-V or 5.0-V I/O operation. These devices have two sets of V_{CC} pins: one for internal operation and input buffers (V_{CCINT}) and another for I/O output drivers (V_{CCIO}).

V_{CCINT} pins must always be connected to a 5.0-V power supply. With this V_{CCINT} level, input voltages are at TTL levels, and are compatible with both 3.3-V and 5.0-V inputs. V_{CCIO} pins can be connected to either a 3.3-V or a 5.0-V power supply, depending on the output requirements. When V_{CCIO} pins are connected to a 5.0-V supply, the output levels are compatible with 5.0-V systems, and when they are connected to a 3.3-V supply, the output high is 3.3 V and is compatible with 3.3-V systems. Devices operating with V_{CCIO} levels lower than 4.75 V incur a nominal timing delay adder of the output buffer timing parameter (t_{OD}).

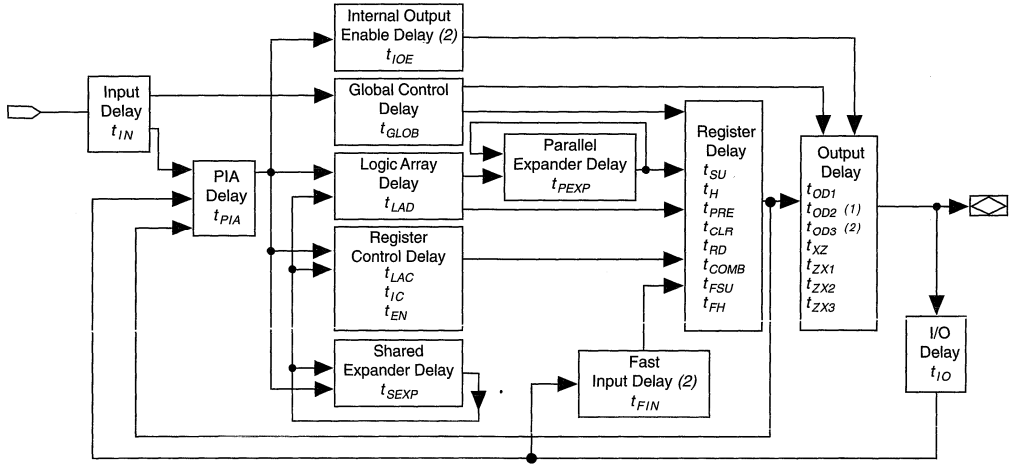
Design Security

All MAX 7000 devices contain a programmable Security Bit that controls access to the data programmed into the device. When this bit is programmed, a proprietary design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security, since programmed data within EEPROM cells is invisible. The Security Bit that controls this function, as well as all other programmed data, is reset only when the device is erased.

Timing Model

MAX 7000 device timing can be analyzed with MAX+PLUS II software, with a variety of popular industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 10. MAX 7000 devices have fixed internal delays that enable the designer to determine the worst-case timing of any design. MAX+PLUS II software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for system-level performance evaluation.

Figure 10. MAX 7000 Timing Model

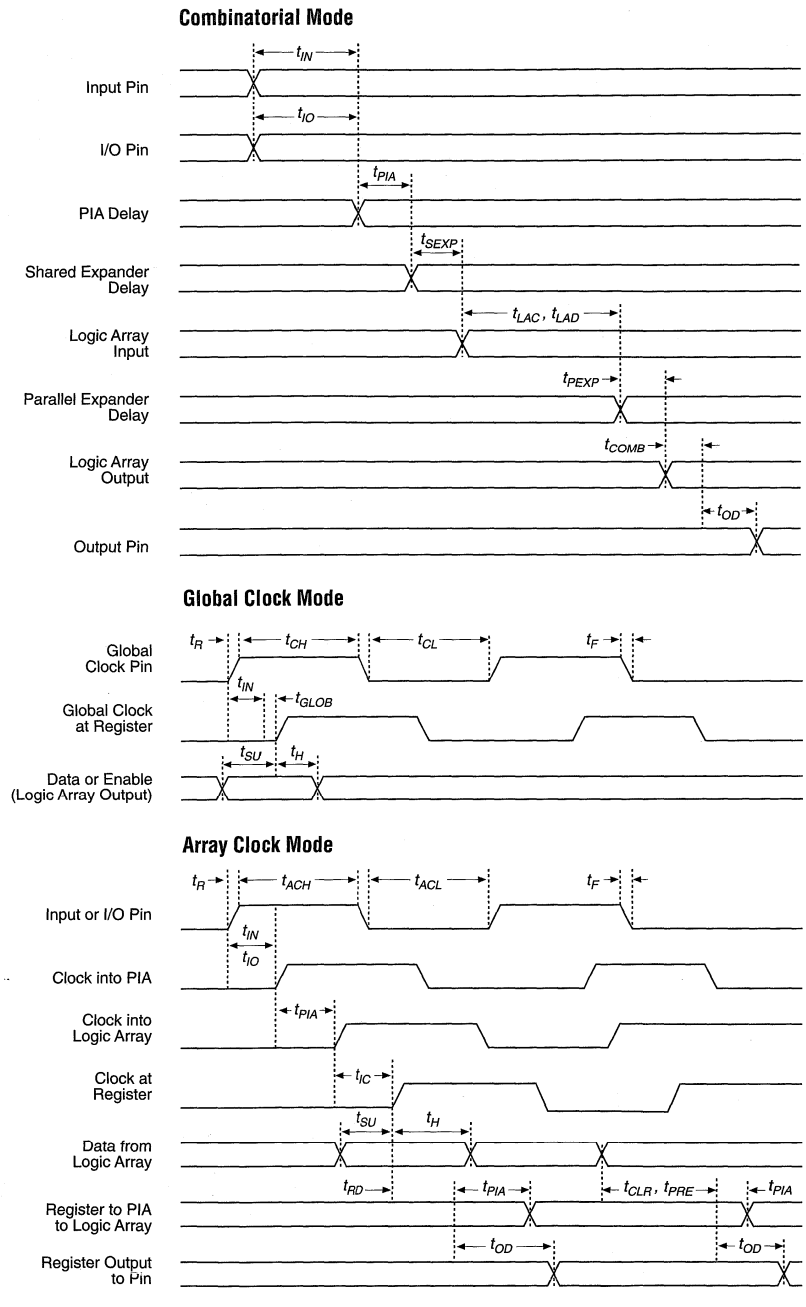


Notes:
(1) Not available in 44-pin devices.
(2) Only available in EPM7128E, EPM7160E, EPM7192E, and EPM7256E devices.

The timing characteristics of any signal path can be derived from the timing model and parameters of a particular device. External timing parameters, which represent pin-to-pin timing delays, can be calculated as the sum of internal parameters. Figure 11 shows the internal timing relationship of internal and external delay parameters. See *Application Brief 100 (Understanding Classic, MAX 5000 & MAX 7000 Timing)* in this data book for more information.

Figure 11. Switching Waveforms

t_R & t_F < 3 ns. Inputs are driven at 3 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.

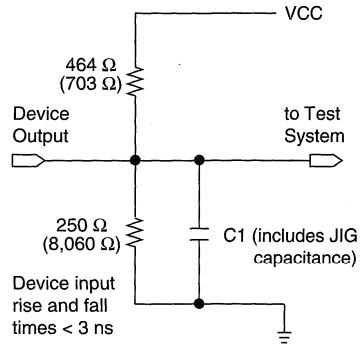


Generic Testing

MAX 7000 devices are fully functionally tested and guaranteed. Complete testing of each programmable EEPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in Figure 12. Test patterns can be used and then erased during early stages of the production flow.

Figure 12. MAX 7000 AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in parentheses are for 3.3-V devices.



Device Programming

All MAX 7000 devices can be programmed on 486- and Pentium-based PCs with an Altera Logic Programmer card, the Master Programming Unit (MPU), and the appropriate device adapter. The MPU performs continuity checking to ensure adequate electrical contact between the adapter and the device.

The MAX+PLUS II software can use text- or waveform-format test vectors created with the MAX+PLUS II Text or Waveform Editor to test the programmed device. For added design verification, designers can perform functional testing to compare the functional behavior of a MAX 7000 device with the results of simulation.

Data I/O and other programming hardware manufacturers also provide programming support for Altera devices. See *Programming Hardware Manufacturers* in this data book for more information.

QFP Carrier & Development Socket

MAX 7000 devices in QFP packages with 100 or more pins are shipped in special plastic carriers to protect the fragile QFP leads. The carrier is used with a prototype development socket and special programming hardware available from Altera. This carrier technology makes it possible to program, test, erase, and reprogram a device without exposing the leads to mechanical stress. For detailed information, refer to the *QFP Carrier & Development Socket Data Sheet* in this data book.

MAX 7000 5.0-V Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*Note (2)*	–2.0	7.0	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias, *Note (3)*	–65 [–55]	135 [125]	° C
T_J	Junction temperature	Under bias, *Note (3)*		150 [175]	° C

MAX 7000 5.0-V Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage of internal logic and input buffers	*Notes (4), (5)*	4.75 (4.5)	5.25 (5.5)	V
V_{CCIO}	Supply voltage of output drivers	5.0-V operation, *Notes (4), (5)*	4.75 (4.5)	5.25 (5.5)	V
		3.3-V operation, *Notes (5), (6)*	3.00	3.60	V
V_I	Input voltage		0	V_{CCINT}	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

MAX 7000 5.0-V Device DC Operating Conditions *Note (7)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage		2.0	V_{CCINT} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
V_{OH}	5.0-V high-level TTL output voltage	I_{OH} = –4 mA DC, V_{CCIO} = 4.75 V	2.4		V
	3.3-V high-level TTL output voltage	I_{OH} = –4 mA DC, V_{CCIO} = 3.0 V	2.4		V
V_{OL}	5.0-V low-level TTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 4.75 V		0.45	V
	3.3-V low-level TTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 3.0 V		0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	–10	10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or GND	–40	40	µA

MAX 7000 5.0-V Device Capacitance: EPM7032, EPM7064 & EPM7096 *Note (8)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		12	pF
$C_{I/O}$	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF

MAX 7000 5.0-V Device Capacitance: EPM7128E, EPM7160E, EPM7192E & EPM7256E *Note (8)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		15	pF
$C_{I/O}$	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		15	pF

Notes to tables:

(1) See *Operating Requirements for Altera Devices* in this data book.

(2) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.

(3) Numbers in brackets are for MIL-STD-883-compliant versions only.

(4) Numbers in parentheses are for military- and industrial-temperature range and MIL-STD-883-compliant versions.

(5) V_{CC} must rise monotonically.

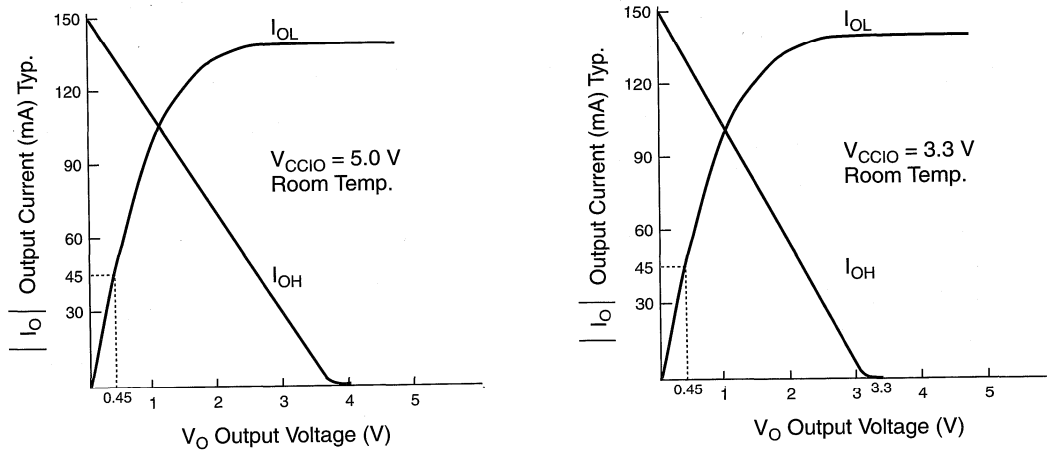
(6) 3.3-V I/O operation is not available for 44-pin packages.

(7) Operating conditions: V_{CCINT} = 5.0 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CCINT} = 5.0 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CCINT} = 5.0 V ± 10%, T_C = –55° C to 125° C for military use.

(8) Capacitance measured at 25° C. Sample-tested only. The `OE1` pin (high-voltage pin during programming) has a maximum capacitance of 20 pF.

Figure 13 shows typical output drive characteristics of MAX 7000 devices.

Figure 13. Output Drive Characteristics of MAX 7000 Devices



MAX 7000 AC Operating Conditions *Notes (1), (2)*

External Timing Parameters			-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		5		6		7.5	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		5		6		7.5	ns
t_{SU}	Global clock setup time		4		5		6		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{FSU}	Global clock setup time of fast input	*Note (3)*	–		–		3		ns
t_{FH}	Global clock hold time of fast input	*Note (3)*	–		–		0.5		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		3.5		4		4.5	ns
t_{CH}	Global clock high time		2		2.5		3		ns
t_{CL}	Global clock low time		2		2.5		3		ns
t_{ASU}	Array clock setup time		2		2.5		3		ns
t_{AH}	Array clock hold time		2		2		2		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		5.5		6.5		7.5	ns
t_{ACH}	Array clock high time		2.5		3		3		ns
t_{ACL}	Array clock low time		2.5		3		3		ns
t_{CNT}	Minimum global clock period			5.6		6.6		8	ns
f_{CNT}	Maximum internal global clock frequency	*Note (4)*	178.6		151.5		125		MHz
t_{ACNT}	Minimum array clock period			5.6		6.6		8	ns
f_{ACNT}	Maximum internal array clock frequency	*Note (4)*	178.6		151.5		125		MHz
f_{MAX}	Maximum clock frequency	*Note (5)*	250		200		166.7		MHz

Internal Timing Parameters			-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			0.4		0.4		0.5	ns
t_{IO}	I/O input pad and buffer delay			0.4		0.4		0.5	ns
t_{FIN}	Fast input delay	*Note (3)*						1	ns
t_{SEXP}	Shared expander delay			3		3.5		4	ns
t_{PEXP}	Parallel expander delay			0.8		0.8		0.8	ns
t_{LAD}	Logic array delay			1.5		2		3	ns
t_{LAC}	Logic control array delay			1.5		2		3	ns
t_{IOE}	Internal output enable delay	*Note (3)*						2	ns
t_{OD1}	Output buffer & pad delay Slow slew rate = off V_{CCIO} = 5.0 V	C1 = 35 pF *Note (1)*		1.5		2		2	ns
t_{OD2}	Output buffer & pad delay Slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF *Note (6)*				2.5		2.5	ns
t_{OD3}	Output buffer & pad delay Slow slew rate = on V_{CCIO} = 5.0 V or 3.3 V	C1 = 35 pF Notes *(1), (3), (6)*						6	ns
t_{ZX1}	Output buffer enable delay Slow slew rate = off V_{CCIO} = 5.0 V	C1 = 35 pF *Note (6)*		4		4		4	ns
t_{ZX2}	Output buffer enable delay Slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF *Note (6)*		–		4.5		4.5	ns
t_{ZX3}	Output buffer enable delay Slow slew rate = on V_{CCIO} = 5.0 V or 3.3 V	C1 = 35 pF *Note (6)*		–		–		8	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4		4		4	ns
t_{SU}	Register setup time		2.5		3		3		ns
t_{H}	Register hold time		1.5		1.5		2		ns
t_{FSU}	Register setup time of fast input	*Note (3)*					3		ns
t_{FH}	Register hold time of fast input	*Note (3)*					0.5		ns
t_{RD}	Register delay			0.8		0.8		1	ns
t_{COMB}	Combinatorial delay			0.8		0.8		1	ns
t_{IC}	Array clock delay			2		2.5		3	ns
t_{EN}	Register enable time			1.5		2		3	ns
t_{GLOB}	Global control delay			0.8		0.8		1	ns
t_{PRE}	Register preset time			2		2		2	ns
t_{CLR}	Register clear time			2		2		2	ns
t_{PIA}	Programmable Interconnect Array delay			0.8		0.8		1	ns
t_{LPA}	Low-power adder	*Note (7)*		8		10		10	ns

External Timing Parameters			-10P Speed Grade		-10 Speed Grade		-12P Speed Grade		-12 Speed Grade		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		10		10		12		12	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		10		10		12		12	ns
t_{SU}	Global clock setup time		7		8		7		10		ns
t_{H}	Global clock hold time		0		0		0		0		ns
t_{FSU}	Global clock setup time of fast input	*Note (3)*	3		3		3		3		ns
t_{FH}	Global clock hold time of fast input	*Note (3)*	0.5		0.5		1		1		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		5		5		6		6	ns
t_{CH}	Global clock high time		4		4		4		4		ns
t_{CL}	Global clock low time		4		4		4		4		ns
t_{ASU}	Array clock setup time		2		3		3		4		ns
t_{AH}	Array clock hold time		3		3		4		4		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		10		10		12		12	ns
t_{ACH}	Array clock high time		4		4		5		5		ns
t_{ACL}	Array clock low time		4		4		5		5		ns
t_{CNT}	Minimum global clock period			10		10		11		11	ns
f_{CNT}	Maximum internal global clock frequency	*Note (4)*	100		100		90.9		90.9		MHz
t_{ACNT}	Minimum array clock period			10		10		11		11	ns
f_{ACNT}	Maximum internal array clock frequency	*Note (4)*	100		100		90.9		90.9		MHz
f_{MAX}	Maximum clock frequency	*Note (5)*	125		125		125		125		MHz

Internal Timing Parameters			-10P Speed Grade		-10 Speed Grade		-12P Speed Grade		-12 Speed Grade		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			0.5		1		1		2	ns
t_{IO}	I/O input pad and buffer delay			0.5		1		1		2	ns
t_{FIN}	Fast input delay	*Note (3)*		1		1		1		1	ns
t_{SEXP}	Shared expander delay			5		5		7		7	ns
t_{PEXP}	Parallel expander delay			0.8		0.8		1		1	ns
t_{LAD}	Logic array delay			5		5		7		5	ns
t_{LAC}	Logic control array delay			5		5		5		5	ns
t_{IOE}	Internal output enable delay	*Note (3)*		2		2		2		2	ns
t_{OD1}	Output buffer & pad delay Slow slew rate = off V_{CCIO} = 5.0 V	C1 = 35 pF *Note (1)*		1.5		2		1		3	ns
t_{OD2}	Output buffer & pad delay Slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF *Note (6)*		2		2.5		2		4	ns
t_{OD3}	Output buffer & pad delay Slow slew rate = on V_{CCIO} = 5.0 V or 3.3 V	C1 = 35 pF *Notes (1), (3), (6)*		5.5		6		5		7	ns
t_{ZX1}	Output buffer enable delay Slow slew rate = off V_{CCIO} = 5.0 V	C1 = 35 pF *Note (6)*		5		5		6		6	ns
t_{ZX2}	Output buffer enable delay Slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF *Note (6)*		5.5		5.5		7		7	ns
t_{ZX3}	Output buffer enable delay Slow slew rate = on V_{CCIO} = 5.0 V or 3.3 V	C1 = 35 pF *Note (6)*		9		9		10		10	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		5		5		6		6	ns
t_{SU}	Register setup time		2		3		1		4		ns
t_{H}	Register hold time		3		3		6		4		ns
t_{FSU}	Register setup time of fast input	*Note (3)*	3		3		4		2		ns
t_{FH}	Register hold time of fast input	*Note (3)*	0.5		0.5		0		2		ns
t_{RD}	Register delay			2		1		2		1	ns
t_{COMB}	Combinatorial delay			2		1		2		1	ns
t_{IC}	Array clock delay			5		5		5		5	ns
t_{EN}	Register enable time			5		5		7		5	ns
t_{GLOB}	Global control delay			1		1		2		0	ns
t_{PRE}	Register preset time			3		3		4		3	ns
t_{CLR}	Register clear time			3		3		4		3	ns
t_{PIA}	Programmable Interconnect Array delay			1		1		1		1	ns
t_{LPA}	Low-power adder	*Note (7)*		11		11		12		12	ns

External Timing Parameters			-15 Speed Grade		-15T Speed Grade		-20 Speed Grade		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		15		15		20	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		15		15		20	ns
t_{SU}	Global clock setup time		11		11		12		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{FSU}	Global clock setup time of fast input	*Note (3)*	3		–		5		ns
t_{FH}	Global clock hold time of fast input	*Note (3)*	1		–		2		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		8		8		12	ns
t_{CH}	Global clock high time		5		6		6		ns
t_{CL}	Global clock low time		5		6		6		ns
t_{ASU}	Array clock setup time		4		4		5		ns
t_{AH}	Array clock hold time		4		4		5		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		15		15		20	ns
t_{ACH}	Array clock high time		6		6.5		8		ns
t_{ACL}	Array clock low time		6		6.5		8		ns
t_{CNT}	Minimum global clock period			13		13		16	ns
f_{CNT}	Maximum internal global clock frequency	*Note (4)*	76.9		76.9		62.5		MHz
t_{ACNT}	Minimum array clock period			13		13		16	ns
f_{ACNT}	Maximum internal array clock frequency	*Note (4)*	76.9		76.9		62.5		MHz
f_{MAX}	Maximum clock frequency	*Note (5)*	100		83.3		83.3		MHz

Internal Timing Parameters			-15 Speed Grade		-15T Speed Grade		-20 Speed Grade		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			2		2		3	ns
t_{IO}	I/O input pad and buffer delay			2		2		3	ns
t_{FIN}	Fast input delay	*Note (3)*		2		–		4	ns
t_{SEXP}	Shared expander delay			8		10		9	ns
t_{PEXP}	Parallel expander delay			1		1		2	ns
t_{LAD}	Logic array delay			6		6		8	ns
t_{LAC}	Logic control array delay			6		6		8	ns
t_{IOE}	Internal output enable delay	*Note (3)*		3		–		4	ns
t_{OD1}	Output buffer & pad delay Slow slew rate = off V_{CCIO} = 5.0 V	C1 = 35 pF *Note (1)*		4		4		5	ns
t_{OD2}	Output buffer & pad delay Slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF *Note (6)*		5		–		6	ns
t_{OD3}	Output buffer & pad delay Slow slew rate = on V_{CCIO} = 5.0 V or 3.3 V	C1 = 35 pF *Notes (3), (6)*		8		–		9	ns
t_{ZX1}	Output buffer enable delay Slow slew rate = off V_{CCIO} = 5.0 V	C1 = 35 pF *Note (6)*		6		6		10	ns
t_{ZX2}	Output buffer enable delay Slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF *Note (6)*		7		–		11	ns
t_{ZX3}	Output buffer enable delay Slow slew rate = on V_{CCIO} = 5.0 V or 3.3 V	C1 = 35 pF *Note (6)*		10		–		14	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		6		6		10	ns
t_{SU}	Register setup time		4		4		4		ns
t_{H}	Register hold time		4		4		5		ns
t_{FSU}	Register setup time of fast input	*Note (3)*	2		–		4		ns
t_{FH}	Register hold time of fast input	*Note (3)*	2		–		3		ns
t_{RD}	Register delay			1		1		1	ns
t_{COMB}	Combinatorial delay			1		1		1	ns
t_{IC}	Array clock delay			6		6		8	ns
t_{EN}	Register enable time			6		6		8	ns
t_{GLOB}	Global control delay			1		1		3	ns
t_{PRE}	Register preset time			4		4		4	ns
t_{CLR}	Register clear time			4		4		4	ns
t_{PIA}	Programmable Interconnect Array delay			2		2		3	ns
t_{LPA}	Low-power adder	*Note (7)*		13		15		15	ns

Notes to tables:

(1) Operating conditions:
V_{CCINT} = 5.0 V ± 5%, V_{CCIO} = 5.0 V ± 5% (except where noted), T_A = 0° C to 70° C for commercial use.
V_{CCINT} = 5.0 V ± 10%, V_{CCIO} = 5.0 V ± 10% (except where noted), T_A = –40° C to 85° C for industrial use.
V_{CCINT} = 5.0 V ± 10%, V_{CCIO} = 5.0 V ± 10% (except where noted), T_C = –55° C to 125° C for military use.

(2) Timing parameters for some devices are preliminary. See Table 2 on page 156 of this data sheet for available speed grades and packages.

(3) This parameter applies only to MAX 7000E devices (EPM7128E, EPM7160E, EPM7192E, and EPM7256E).

(4) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.

(5) The f_{MAX} values represent the highest frequency for pipelined data.

(6) Operating conditions: V_{CCIO} = 3.3 V ± 10% for commercial, industrial, and military use.

(7) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{EN}, and t_{SEXP} parameters for macrocells running in the low-power mode.

3.3-V EPM7032V

The EPM7032V device is a high-performance MAX 7000 device that meets the low power and voltage requirements of 3.3-V applications ranging from notebook computers to battery-operated, hand-held equipment. The EPM7032V provides in-system speeds of up to 90.9 MHz and propagation delays of 12 ns. It is available in 44-pin reprogrammable PLCC or TQFP packages and can accommodate designs with up to 36 inputs and 32 outputs.

Power Management

The 3.3-V operation of the EPM7032V offers power savings of 30% to 50% over the 5.0-V operation of the EPM7032. Power-saving features of the EPM7032V include a programmable power-saving mode and a power-down mode.

Power-Down Mode

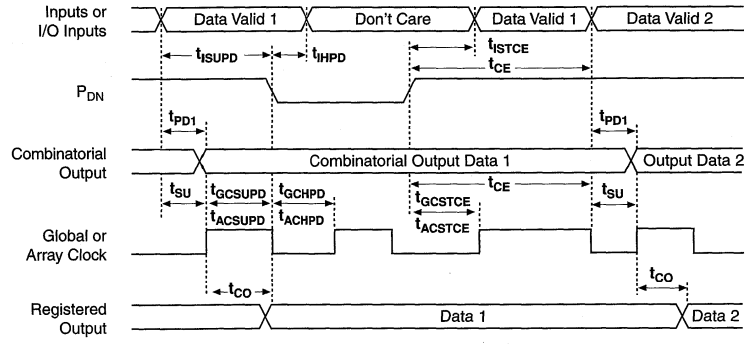
The EPM7032V device provides a unique power-down mode that allows the device to consume near-zero power (typically 50 µA). The power-down mode is controlled externally by the dedicated power-down pin (PDn). When PDn is asserted (active low), the power-down sequence latches all input pins, internal logic, and output pins of the EPM7032V device, preserving their present state. Output pins maintain their present low, high, or tri-state value while in power-down mode.

Once in power-down mode, any or all of the inputs, including Clocks, can be toggled without affecting the state of the device. Since internal latches are used to ensure that the proper state exists during power-down mode, the external inputs and Clocks must meet certain setup and hold time requirements. See Figure 14 and the "Power-Down Timing Parameters" and "Chip Enable Timing Parameters" tables on page 189 of this data sheet.

Figure 14. Power-Down Mode Switching Waveforms

The switching waveforms for the EPM7032V are identical to those of the 5.0-V EPM7032 in all modes, except for the additional power-down mode shown here.

t_R & t_F < 3 ns. Inputs are driven at 3 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.



When the PDn signal is brought high, the device is enabled and the combinatorial outputs respond to the present input conditions within the specified chip-enable delay (t_{CE}). Registered outputs respond to Clock transitions within t_{CE}. Clocking the device during the chip-enable sequence can cause the data to change inside the chip if a Clock transition occurs during certain intervals of the chip-enable or chip-disable sequences. All Clocks should be gated to prevent Clock transitions during the Clock setup time (t_{GCSUPD} or t_{ACSUPD}) and during the chip-enable setup time (t_{GCSTCE} or t_{ACSTCE}), as shown in Figure 14.

All registers in the EPM7032V provide Clock Enable control, which makes it easy to disable Clocks. If output signals must be frozen in a high-impedance state during power-down, the associated Output Enable signal must be asserted, the system Clock must be removed, and the PDn pin must be asserted. To reactivate the device, the sequence is reversed. For some systems, it may be more appropriate to switch the order of the Clock and Output Enable controls.

All power-down/chip-enable timing parameters are computed from external input or I/O pins, with the macrocell Turbo Bit turned on, and without the use of parallel expanders. For macrocells in low-power mode (Turbo Bit off), the low-power adder, t_{LPA}, must be added to the power-down/chip-enable timing parameters, which include the data paths t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{ACH}, and t_{SEXP}. For macrocells that use shared or parallel expanders, t_{SEXP} or t_{PEXP} must be added. For data or Clock paths that use more than one logic array delay, the worst-case data or Clock delay must be added to the respective power-down/chip-enable parameters. Actual worst-case timing of data and Clock paths can be calculated with the MAX+PLUS II Simulator or Timing Analyzer, or with other industry-standard EDA verification tools.

MAX 7000 3.3-V Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND, *Note (2)*	–2.0	5.6	V
V_I	DC input voltage	With respect to GND, *Note (2)*	–2.0	5.6	V
I_{OUT}	DC output current per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C
P_D	Power dissipation			1,000	mW
I_{MAX}	DC V_{CC} or GND current			300	mA

MAX 7000 3.3-V Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	*Note (3)*	3.0	3.6	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

MAX 7000 3.3-V Device DC Operating Conditions *Notes (4), (5)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –0.1 mA DC	V_{CC} – 0.2			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC			0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or GND	–10		10	µA
I_{CC0}	V_{CC} supply current (standby, power-down mode)	*Note (6)*		2	150	µA
I_{CC1}	V_{CC} supply current (standby, low-power mode)	V_I = GND, no load, *Note (6)*		10	20	mA
I_{CC2}	V_{CC} supply current (active, low-power mode)	V_I = GND, no load, f = 1.0 MHz, *Note (6)*		15	25	mA

MAX 7000 3.3-V Device Capacitance *Note (7)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		12	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF

Notes to tables:

(1) See *Operating Requirements for Altera Devices* in this data book.

(2) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to V_{CC} + 2.0 V for periods shorter than 20 ns under no-load conditions.

(3) V_{CC} must rise monotonically.

(4) Typical values are for T_A = 25° C and V_{CC} = 3.3 V.

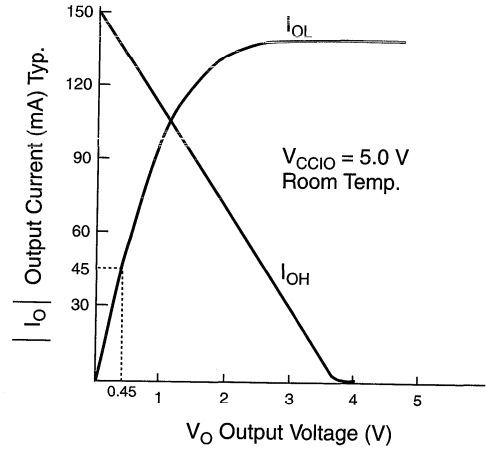
(5) Operating conditions: V_{CC} = 3.3 V ± 10%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 3.3 V ± 10%, T_A = –40° C to 85° C for industrial use.

(6) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB. I_{CC} is measured at 0° C.

(7) Capacitance is measured at 25° C. Sample-tested only. The `OE1n` pin (high-voltage pin during programming) has a maximum capacitance of 20 pF.

Figure 15 shows typical output drive characteristics of the EPM7032V.

Figure 15. EPM7032V Output Drive Characteristics



EPM7032V AC Operating Conditions *Note (1)*

External Timing Parameters			EPM7032V-12		EPM7032V-15		EPM7032V-20		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		12		15		20	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		12		15		20	ns
t_{SU}	Global clock setup time		10		11		12		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		7		8		12	ns
t_{CH}	Global clock high time		4		5		6		ns
t_{CL}	Global clock low time		4		5		6		ns
t_{ASU}	Array clock setup time		4		4		5		ns
t_{AH}	Array clock hold time		4		4		5		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		12		15		20	ns
t_{ACH}	Array clock high time		5		6		8		ns
t_{ACL}	Array clock low time		5		6		8		ns
t_{CNT}	Minimum global clock period			11		13		16	ns
f_{CNT}	Maximum internal global clock frequency	*Note (2)*	90.9		76.9		62.5		MHz
t_{ACNT}	Minimum array clock period			11		13		16	ns
f_{ACNT}	Maximum internal array clock frequency	*Note (2)*	90.9		76.9		62.5		MHz
f_{MAX}	Maximum clock frequency	*Note (3)*	125		100		83.3		MHz

EPM7032V AC Operating Conditions *Note (1)*

Internal Timing Parameters			EPM7032V-12		EPM7032V-15		EPM7032V-20		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			3		2		3	ns
t_{IO}	I/O input pad and buffer delay			3		2		3	ns
t_{SEXP}	Shared expander delay			7		8		9	ns
t_{PEXP}	Parallel expander delay			1		1		2	ns
t_{LAD}	Logic array delay			4		6		8	ns
t_{LAC}	Logic control array delay			4		6		8	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		3		4		5	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		6		6		9	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		6		6		9	ns
t_{SU}	Register setup time		5		4		4		ns
t_{H}	Register hold time		4		4		5		ns
t_{RD}	Register delay			1		1		1	ns
t_{COMB}	Combinatorial delay			1		1		1	ns
t_{IC}	Array clock delay			4		6		8	ns
t_{EN}	Register enable time			4		6		8	ns
t_{GLOB}	Global control delay			0		1		3	ns
t_{PRE}	Register preset time			3		4		4	ns
t_{CLR}	Register clear time			3		4		4	ns
t_{PIA}	Programmable Interconnect Array delay			1		2		3	ns
t_{LPA}	Low-power adder	*Note (4)*		15		17		20	ns

Notes to tables:

(1) Operating conditions: V_{CC} = 3.3 V ± 10%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 3.3 V ± 10%, T_A = –40° C to 85° C for industrial use.

(2) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB. I_{CC} is measured at 0° C.

(3) The f_{MAX} values represent the highest frequency for pipelined data.

(4) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{EN}, and t_{SEXP} parameters for macrocells running in low-power mode.

MAX 7000 3.3-V Device Power-Down/Chip-Enable Timing Parameters

Power-Down Timing Parameters		EPM7032V-12		EPM7032V-15		EPM7032V-20		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{ISUPD}	Input or I/O input setup time before power down	30		30		35		ns
t_{IHPD}	Input or I/O input hold time after power down	0		0		0		ns
t_{GCSUPD}	Global clock setup time before power down	20		20		25		ns
t_{GCHPD}	Global clock hold time after power down	0		0		0		ns
t_{ACSUPD}	Array clock setup time before power down	30		30		35		ns
t_{ACHPD}	Array clock hold time after power down	0		0		0		ns
t_{HPD}	Minimum high pulse width of power-down pin	800		800		900		ns
t_{LPD}	Minimum low pulse width of power-down pin	800		800		900		ns
t_{PDOWN}	Power down delay		800		800		900	ns

Chip-Enable Timing Parameters		EPM7032V-12		EPM7032V-15		EPM7032V-20		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{ISTCE}	Input or I/O input stable after chip enable		60		60		70	ns
t_{GCSTCE}	Global clock stable after chip enable		60		60		70	ns
t_{ACSTCE}	Array clock stable after chip enable		60		60		70	ns
t_{CE}	Data stable after chip enable		700		700		800	ns

Calculating the Supply Current

Supply current (I_{CC}) versus frequency (f_{MAX}) for MAX 7000 devices is calculated with the following equation:

$$I_{CC} = I_{CCOUTPUT} + I_{CCACTIVE}$$

The $I_{CCOUTPUT}$ value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Operating Requirements for Altera Devices* in this data book. The $I_{CCACTIVE}$ value depends on the switching frequency and the application logic.

The $I_{CCACTIVE}$ value is calculated with the following equation:

$$I_{CCACTIVE} = (A \times MC_{TON}) + (B \times MC_{TOFF}) + (C \times MC) \times f_{MAX}$$

The parameters for this equation are:

MC_{TON} = number of macrocells used with Turbo Bit on
MC_{TOFF} = number of macrocells used with Turbo Bit off
MC = total number of macrocells used in the design ($MC_{TON} + MC_{TOFF}$)
f_{MAX} = highest Clock frequency to the device

Table 4 lists the values of constants A, B, and C.

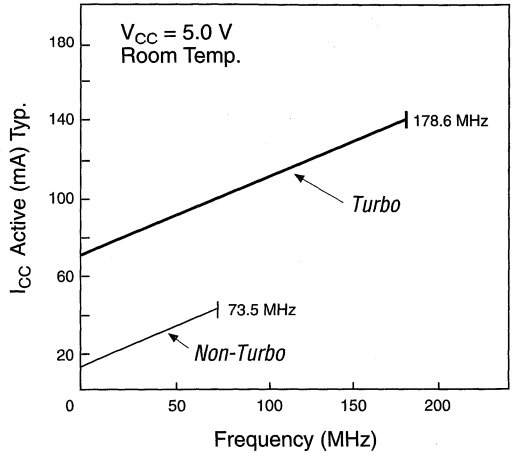
Table 4. MAX 7000 I_{CC} Equation Constants

Device	Constant A	Constant B	Constant C
EPM7032	2.20	0.55	0.0180
EPM7032V	0.98	0.42	0.0060
EPM7064	1.92	0.78	0.0180
EPM7096	1.92	0.78	0.0180
EPM7128E	1.38	0.57	0.0120
EPM7160E	1.38	0.57	0.0120
EPM7192E	1.38	0.57	0.0120
EPM7256E	1.38	0.57	0.0120

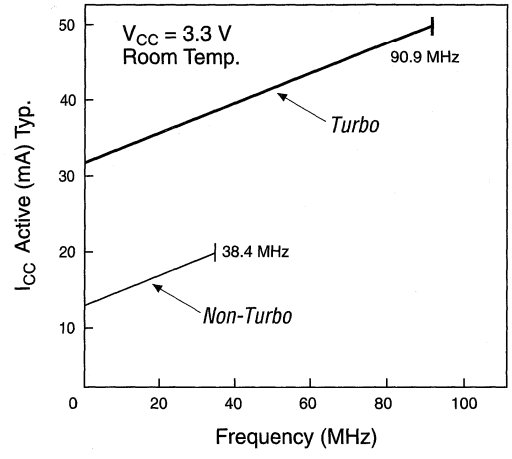
This calculation provides an I_{CC} estimate based on typical conditions using a typical pattern of a 16-bit, loadable, enabled, up/down counter in each LAB with no output load. Actual I_{CC} should be verified during operation since this measurement is sensitive to the actual pattern in the device and the environmental operating conditions. Figure 16 shows typical supply current versus frequency of the MAX 7000 devices listed in Table 4.

Figure 16. I_{CC} vs. Frequency of MAX 7000 Devices (Part 1 of 2)

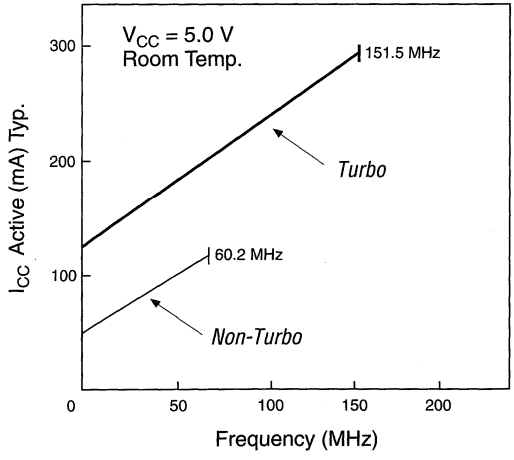
EPM7032



EPM7032V



EPM7064



EPM7096

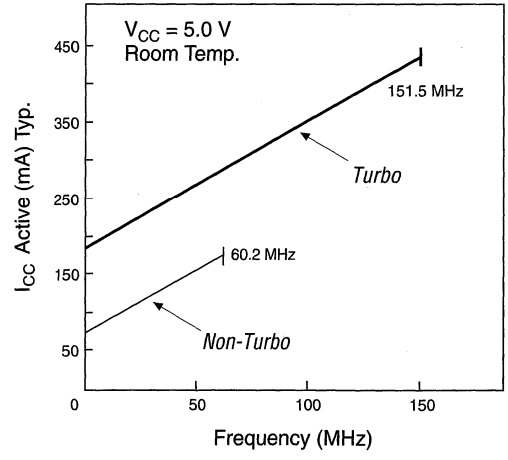
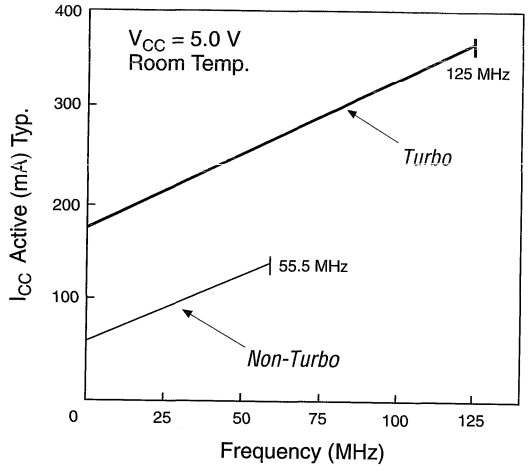
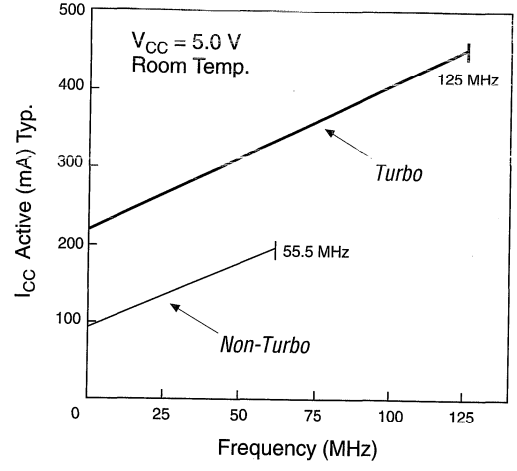


Figure 16. I_{CC} vs. Frequency of MAX 7000 Devices (Part 2 of 2)

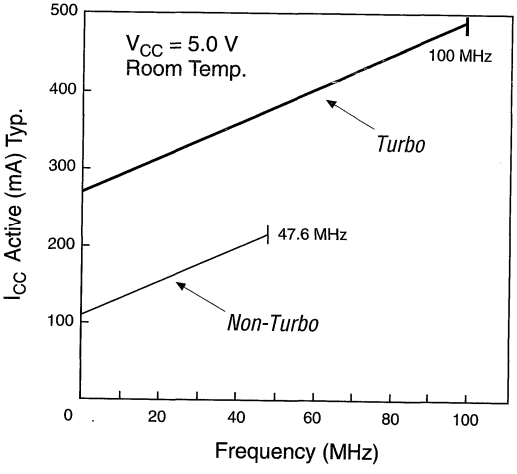
EPM7128E



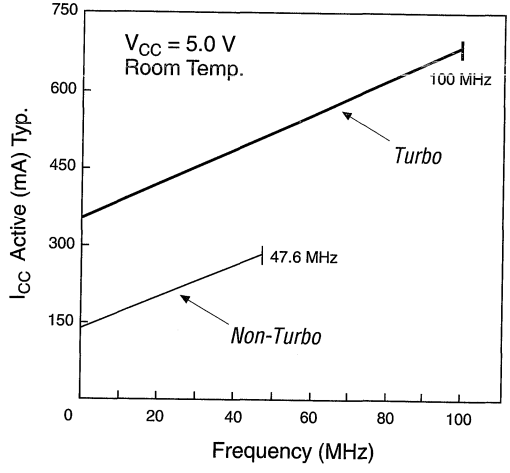
EPM7160E



EPM7192E



EPM7256E



Device Pin-Outs

Tables 5 through 18 show the pin names and numbers of MAX 7000 device packages.

Table 5. EPM7032 & EPM7032V Dedicated Pin-Outs

Dedicated Pin	44-Pin J-Lead	44-Pin QFP
INPUT/GCLK	43	37
INPUT/GCLR*n*	1	39
INPUT/OE1*n*	44	38
INPUT/OE2*n*	2	40
GND	10, 22, 30, 42	4, 16, 24, 36
VCC	3, 15, 23, 35	9, 17, 29, 41
No Connect (N.C.)	–	–
Total User I/O Pins	32	32

Table 6. EPM7032 & EPM7032V I/O Pin-Outs

MC	LAB	44-Pin J-Lead	44-Pin QFP	MC	LAB	44-Pin J-Lead	44-Pin QFP
1	A	4	42	17	B	41	35
2	A	5	43	18	B	40	34
3	A	6	44	19	B	39	33
4	A	7	1	20	B	38	32
5	A	8	2	21	B	37	31
6	A	9	3	22	B	36	30
7	A	11	5	23	B	34	28
8	A	12	6	24	B	33	27
9	A	13	7	25	B	32	26
10	A	14	8	26	B	31	25
11	A	16	10	27	B	29	23
12	A	17	11	28	B	28	22
13	A	18	12	29	B	27	21
14	A	19	13	30	B	26	20
15	A	20	14	31	B	25	19
16	A	21	15	32	B	24	18

Table 7. EPM7064 Dedicated Pin-Outs

Dedicated Pin	44-Pin J-Lead	44-Pin QFP	68-Pin J-Lead	84-Pin J-Lead	100-Pin QFP
INPUT/GCLK	43	37	67	83	89
INPUT/GCLRn	1	39	1	1	91
INPUT/OE1n	44	38	68	84	90
INPUT/OE2n	2	40	2	2	92
GND	10, 22, 30, 42	4, 16, 24, 36	6, 16, 26, 34, 38, 48, 58, 66	7, 19, 32, 42, 47, 59, 72, 82	13, 28, 40, 45, 61, 76, 88, 97
VCCINT (5.0 V only)	3, 15, 23, 35	9, 17, 29, 41	3, 35	3, 43	41, 93
VCCIO (3.3 V or 5.0 V)	–	–	11, 21, 31, 43, 53, 63	13, 26, 38, 53, 66, 78	5, 20, 36, 53, 68, 84
No Connect (N.C.)	–	–	–	–	1, 2, 7, 9, 24, 26, 29, 30, 51, 52, 55, 57, 72, 74, 79, 80
Total User I/O Pins	32	32	48	64	64

Table 8. EPM7064 I/O Pin-Outs

MC	LAB	44-Pin J-Lead	44-Pin QFP	68-Pin J-Lead	84-Pin J-Lead	100-Pin QFP	MC	LAB	44-Pin J-Lead	44-Pin QFP	68-Pin J-Lead	84-Pin J-Lead	100-Pin QFP
1	A	12	6	18	22	16	17	B	21	15	33	41	39
2	A	–	–	–	21	15	18	B	–	–	–	40	38
3	A	11	5	17	20	14	19	B	20	14	32	39	37
4	A	9	3	15	18	12	20	B	19	13	30	37	35
5	A	8	2	14	17	11	21	B	18	12	29	36	34
6	A	–	–	13	16	10	22	B	–	–	28	35	33
7	A	–	–	–	15	8	23	B	–	–	–	34	32
8	A	7	1	12	14	6	24	B	17	11	27	33	31
9	A	–	–	10	12	4	25	B	16	10	25	31	27
10	A	–	–	–	11	3	26	B	–	–	–	30	25
11	A	6	44	9	10	100	27	B	–	–	24	29	23
12	A	–	–	8	9	99	28	B	–	–	23	28	22
13	A	–	–	7	8	98	29	B	–	–	22	27	21
14	A	5	43	5	6	96	30	B	14	8	20	25	19
15	A	–	–	–	5	95	31	B	–	–	–	24	18
16	A	4	42	4	4	94	32	B	13	7	19	23	17
33	C	24	18	36	44	42	49	D	33	27	51	63	65
34	C	–	–	–	45	43	50	D	–	–	–	64	66
35	C	25	19	37	46	44	51	D	34	28	52	65	67
36	C	26	20	39	48	46	52	D	36	30	54	67	69
37	C	27	21	40	49	47	53	D	37	31	55	68	70
38	C	–	–	41	50	48	54	D	–	–	56	69	71
39	C	–	–	–	51	49	55	D	–	–	–	70	73
40	C	28	22	42	52	50	56	D	38	32	57	71	75
41	C	29	23	44	54	54	57	D	39	33	59	73	77
42	C	–	–	–	55	56	58	D	–	–	–	74	78
43	C	–	–	45	56	58	59	D	–	–	60	75	81
44	C	–	–	46	57	59	60	D	–	–	61	76	82
45	C	–	–	47	58	60	61	D	–	–	62	77	83
46	C	31	25	49	60	62	62	D	40	34	64	79	85
47	C	–	–	–	61	63	63	D	–	–	–	80	86
48	C	32	26	50	62	64	64	D	41	35	65	81	87

Table 9. EPM7096 Dedicated Pin-Outs

Dedicated Pin	68-Pin J-Lead	84-Pin J-Lead	100-Pin QFP
INPUT/GCLK	67	83	89
INPUT/GCLR*n*	1	1	91
INPUT/OE1*n*	68	84	90
INPUT/OE2*n*	2	2	92
GND	6, 16, 26, 34, 38, 48, 58, 66	7, 19, 32, 42, 47, 59, 72, 82	13, 28, 40, 45, 61, 76, 88, 97
VCCINT (5.0 V only)	3, 35	3, 43	41, 93
VCCIO (3.3 V or 5.0 V)	11, 21, 31, 43, 53, 63	13, 26, 38, 53, 66, 78	5, 20, 36, 53, 68, 84
No Connect (N.C.)	–	6, 39, 46, 79	9, 24, 37, 44, 57, 72, 85, 96
Total User I/O Pins	48	60	72

Table 10. EPM7096 I/O Pin-Outs (Part 1 of 2)

MC	LAB	68-Pin J-Lead	84-Pin J-Lead	100-Pin QFP	MC	LAB	68-Pin J-Lead	84-Pin J-Lead	100-Pin QFP
1	A	13	16	8	17	B	23	28	23
2	A	–	–	–	18	B	–	–	–
3	A	–	15	7	19	B	22	27	22
4	A	12	14	6	20	B	–	–	21
5	A	–	–	4	21	B	20	25	19
6	A	10	12	3	22	B	–	24	18
7	A	–	–	–	23	B	–	–	–
8	A	9	11	2	24	B	19	23	17
9	A	8	10	1	25	B	18	22	16
10	A	–	–	–	26	B	–	–	–
11	A	–	9	100	27	B	17	21	15
12	A	7	8	99	28	B	–	20	14
13	A	–	–	98	29	B	15	18	12
14	A	5	5	95	30	B	–	–	11
15	A	–	–	–	31	B	–	–	–
16	A	4	4	94	32	B	14	17	10

Table 10. EPM7096 I/O Pin-Outs (Part 2 of 2)

MC	LAB	68-Pin J-Lead	84-Pin J-Lead	100-Pin QFP	MC	LAB	68-Pin J-Lead	84-Pin J-Lead	100-Pin QFP
33	C	33	41	39	49	D	36	44	42
34	C	–	–	–	50	D	–	–	–
35	C	32	40	38	51	D	37	45	43
36	C	–	–	35	52	D	–	–	46
37	C	30	37	34	53	D	39	48	47
38	C	–	36	33	54	D	–	49	48
39	C	–	–	–	55	D	–	–	–
40	C	29	35	32	56	D	40	50	49
41	C	28	34	31	57	D	41	51	50
42	C	–	–	–	58	D	–	–	–
43	C	27	33	30	59	D	42	52	51
44	C	–	–	29	60	D	–	–	52
45	C	25	31	27	61	D	44	54	54
46	C	–	30	26	62	D	–	55	55
47	C	–	–	–	63	D	–	–	–
48	C	24	29	25	64	D	45	56	56
65	E	46	57	58	81	F	56	69	73
66	E	–	–	–	82	F	–	–	–
67	E	47	58	59	83	F	–	70	74
68	E	–	–	60	84	F	57	71	75
69	E	49	60	62	85	F	–	–	77
70	E	–	61	63	86	F	59	73	78
71	E	–	–	–	87	F	–	–	–
72	E	50	62	64	88	F	60	74	79
73	E	51	63	65	89	F	61	75	80
74	E	–	–	–	90	F	–	–	–
75	E	52	64	66	91	F	–	76	81
76	E	–	65	67	92	F	62	77	82
77	E	54	67	69	93	F	–	–	83
78	E	–	–	70	94	F	64	80	86
79	E	–	–	–	95	F	–	–	–
80	E	55	68	71	96	F	65	81	87

Table 11. EPM7128E Dedicated Pin-Outs

Dedicated Pin	84-Pin J-Lead	100-Pin QFP	160-Pin QFP
INPUT/GCLK1	83	89	139
INPUT/GCLRn	1	91	141
INPUT/OE1	84	90	140
INPUT/OE2/GCLK2	2	92	142
GND	7, 19, 32, 42, 47, 59, 72, 82	13, 28, 40, 45, 61, 76, 88, 97	17, 42, 60, 66, 95, 113, 138, 148
VCCINT (5.0 V only)	3, 43	41, 93	61, 143
VCCIO (3.3 V or 5.0 V)	13, 26, 38, 53, 66, 78	5, 20, 36, 53, 68, 84	8, 26, 55, 79, 104, 133
No Connect (N.C.)	–	–	1, 2, 3, 4, 5, 6, 7, 34, 35, 36, 37, 38, 39, 40, 44, 45, 46, 47, 74, 75, 76, 77, 81, 82, 83, 84, 85, 86, 87, 114, 115, 116, 117, 118, 119, 120, 124, 125, 126, 127, 154, 155, 156, 157
Total User I/O Pins	64	80	96

Table 12. EPM7128E I/O Pin-Outs (Part 1 of 2)

MC	LAB	84-Pin J-Lead	100-Pin QFP	160-Pin QFP	MC	LAB	84-Pin J-Lead	100-Pin QFP	160-Pin QFP
1	A	–	4	160	17	B	22	16	21
2	A	–	–	–	18	B	–	–	–
3	A	12	3	159	19	B	21	15	20
4	A	–	–	158	20	B	–	–	19
5	A	11	2	153	21	B	20	14	18
6	A	10	1	152	22	B	–	12	16
7	A	–	–	–	23	B	–	–	–
8	A	9	100	151	24	B	18	11	15
9	A	–	99	150	25	B	17	10	14
10	A	–	–	–	26	B	–	–	–
11	A	8	98	149	27	B	16	9	13
12	A	–	–	147	28	B	–	–	12
13	A	6	96	146	29	B	15	8	11
14	A	5	95	145	30	B	–	7	10
15	A	–	–	–	31	B	–	–	–
16	A	4	94	144	32	B	14	6	9
33	C	–	27	41	49	D	41	39	59
34	C	–	–	–	50	D	–	–	–
35	C	31	26	33	51	D	40	38	58
36	C	–	–	32	52	D	–	–	57
37	C	30	25	31	53	D	39	37	56
38	C	29	24	30	54	D	–	35	54
39	C	–	–	–	55	D	–	–	–
40	C	28	23	29	56	D	37	34	53
41	C	–	22	28	57	D	36	33	52
42	C	–	–	–	58	D	–	–	–
43	C	27	21	27	59	D	35	32	51
44	C	–	–	25	60	D	–	–	50
45	C	25	19	24	61	D	34	31	49
46	C	24	18	23	62	D	–	30	48
47	C	–	–	–	63	D	–	–	–
48	C	23	17	22	64	D	33	29	43

Table 12. EPM7128E I/O Pin-Outs (Part 2 of 2)

MC	LAB	84-Pin J-Lead	100-Pin QFP	160-Pin QFP	MC	LAB	84-Pin J-Lead	100-Pin QFP	160-Pin QFP
65	E	44	42	62	81	F	–	54	80
66	E	–	–	–	82	F	–	–	–
67	E	45	43	63	83	F	54	55	88
68	E	–	–	64	84	F	–	–	89
69	E	46	44	65	85	F	55	56	90
70	E	–	46	67	86	F	56	57	91
71	E	–	–	–	87	F	–	–	–
72	E	48	47	68	88	F	57	58	92
73	E	49	48	69	89	F	–	59	93
74	E	–	–	–	90	F	–	–	–
75	E	50	49	70	91	F	58	60	94
76	E	–	–	71	92	F	–	–	96
77	E	51	50	72	93	F	60	62	97
78	E	–	51	73	94	F	61	63	98
79	E	–	–	–	95	F	–	–	–
80	E	52	52	78	96	F	62	64	99
97	G	63	65	100	113	H	–	77	121
98	G	–	–	–	114	H	–	–	–
99	G	64	66	101	115	H	73	78	122
100	G	–	–	102	116	H	–	–	123
101	G	65	67	103	117	H	74	79	128
102	G	–	69	105	118	H	75	80	129
103	G	–	–	–	119	H	–	–	–
104	G	67	70	106	120	H	76	81	130
105	G	68	71	107	121	H	–	82	131
106	G	–	–	–	122	H	–	–	–
107	G	69	72	108	123	H	77	83	132
108	G	–	–	109	124	H	–	–	134
109	G	70	73	110	125	H	79	85	135
110	G	–	74	111	126	H	80	86	136
111	G	–	–	–	127	H	–	–	–
112	G	71	75	112	128	H	81	87	137

Table 13. EPM7160E Dedicated Pin-Outs

Dedicated Pin	84-Pin J-Lead	100-Pin QFP	160-Pin QFP
INPUT/GCLK1	83	89	139
INPUT/GCLR*n*	1	91	141
INPUT/OE1	84	90	140
INPUT/OE2/GCLK2	2	92	142
GND	7, 19, 32, 42, 47, 59, 72, 82	13, 28, 40, 45, 61, 76, 88, 97	17, 42, 60, 66, 95, 113, 138, 148
VCCINT (5.0 V only)	3, 43	41, 93	61, 143
VCCIO (3.3 V or 5.0 V)	13, 26, 38, 53, 66, 78	5, 20, 36, 53, 68, 84	8, 26, 55, 79, 104, 133
No Connect (N.C.)	6, 39, 46, 79	–	1, 2, 3, 4, 5, 6, 34, 35, 36, 37, 38, 39, 40, 45, 46, 47, 74, 75, 76, 81, 82, 83, 84, 85, 86, 87, 115, 116, 117, 118, 119, 120, 124, 125, 126, 127, 154, 155, 156, 157
Total User I/O Pins	60	80	100

Table 14. EPM7160E I/O Pin-Outs (Part 1 of 3)

MC	LAB	84-Pin J-Lead	100-Pin QFP	160-Pin QFP	MC	LAB	84-Pin J-Lead	100-Pin QFP	160-Pin QFP
1	A	11	2	158	17	B	18	11	15
2	A	–	–	–	18	B	–	–	–
3	A	10	1	153	19	B	17	10	14
4	A	–	–	–	20	B	–	–	–
5	A	–	–	152	21	B	–	–	13
6	A	–	100	151	22	B	–	9	12
7	A	–	–	–	23	B	–	–	–
8	A	9	99	150	24	B	16	8	11
9	A	8	98	149	25	B	15	7	10
10	A	–	–	–	26	B	–	–	–
11	A	5	96	147	27	B	14	6	9
12	A	–	–	–	28	B	–	–	–
13	A	–	–	146	29	B	–	–	7
14	A	–	95	145	30	B	–	4	160
15	A	–	–	–	31	B	–	–	–
16	A	4	94	144	32	B	12	3	159
33	C	–	21	27	49	D	–	–	48
34	C	–	–	–	50	D	–	–	–
35	C	25	19	25	51	D	33	30	44
36	C	–	–	–	52	D	–	–	–
37	C	–	–	24	53	D	–	29	43
38	C	24	18	23	54	D	31	27	41
39	C	–	–	–	55	D	–	–	–
40	C	23	17	22	56	D	30	26	33
41	C	–	12	16	57	D	–	–	32
42	C	–	–	–	58	D	–	–	–
43	C	20	14	18	59	D	29	25	31
44	C	–	–	–	60	D	–	–	–
45	C	–	–	19	61	D	–	24	30
46	C	21	15	20	62	D	28	23	29
47	C	–	–	–	63	D	–	–	–
48	C	22	16	21	64	D	27	22	28

Table 14. EPM7160E I/O Pin-Outs (Part 2 of 3)

MC	LAB	84-Pin J-Lead	100-Pin QFP	160-Pin QFP	MC	LAB	84-Pin J-Lead	100-Pin QFP	160-Pin QFP
65	E	–	–	59	81	F	–	–	62
66	E	–	–	–	82	F	–	–	–
67	E	41	39	58	83	F	44	42	63
68	E	–	–	–	84	F	–	–	–
69	E	–	38	57	85	F	–	43	64
70	E	40	37	56	86	F	45	44	65
71	E	–	–	–	87	F	–	–	–
72	E	37	35	54	88	F	48	46	67
73	E	–	–	53	89	F	–	–	68
74	E	–	–	–	90	F	–	–	–
75	E	36	34	52	91	F	49	47	69
76	E	–	–	–	92	F	–	–	–
77	E	–	33	51	93	F	–	48	70
78	E	35	32	50	94	F	50	49	71
79	E	–	–	–	95	F	–	–	–
80	E	34	31	49	96	F	51	50	72
97	G	–	–	73	113	H	–	60	94
98	G	–	–	–	114	H	–	–	–
99	G	52	51	77	115	H	60	62	96
100	G	–	–	–	116	H	–	–	–
101	G	–	52	78	117	H	–	–	97
102	G	54	54	80	118	H	61	63	98
103	G	–	–	–	119	H	–	–	–
104	G	55	55	88	120	H	62	64	99
105	G	–	–	89	121	H	–	69	105
106	G	–	–	–	122	H	–	–	–
107	G	56	56	90	123	H	65	67	103
108	G	–	–	–	124	H	–	–	–
109	G	–	57	91	125	H	–	–	102
110	G	57	58	92	126	H	64	66	101
111	G	–	–	–	127	H	–	–	–
112	G	58	59	93	128	H	63	65	100

Table 14. EPM7160E I/O Pin-Outs (Part 3 of 3)

MC	LAB	84-Pin J-Lead	100-Pin QFP	160-Pin QFP	MC	LAB	84-Pin J-Lead	100-Pin QFP	160-Pin QFP
129	I	67	70	106	145	J	74	79	123
130	I	–	–	–	146	J	–	–	–
131	I	68	71	107	147	J	75	80	128
132	I	–	–	–	148	J	–	–	–
133	I	–	–	108	149	J	–	–	129
134	I	–	72	109	150	J	–	81	130
135	I	–	–	–	151	J	–	–	–
136	I	69	73	110	152	J	76	82	131
137	I	70	74	111	153	J	77	83	132
138	I	–	–	–	154	J	–	–	–
139	I	71	75	112	155	J	80	85	134
140	I	–	–	–	156	J	–	–	–
141	I	–	–	114	157	J	–	–	135
142	I	–	77	121	158	J	–	86	136
143	I	–	–	–	159	J	–	–	–
144	I	73	78	122	160	J	81	87	137

Table 15. EPM7192E Dedicated Pin-Outs

Dedicated Pin	160-Pin PGA	160-Pin QFP
INPUT/GCLK1	M8	139
INPUT/GCLR*n*	N8	141
INPUT/OE1	P8	140
INPUT/OE2/GCLK2	R8	142
GND	C4, C6, C11, D7, D9, D13, G4, H12, J4, M7, M9, M13, N4, N11	3, 18, 32, 47, 57, 64, 66, 81, 96, 111, 126, 138, 143, 148
VCCINT (5.0 V only)	C7, C9, N7, N9	56, 65, 137, 144
VCCIO (3.3 V or 5.0 V)	C5, C10, C12, D3, G12, H4, J12, M3, N5, N12	10, 25, 40, 55, 74, 89, 103, 118, 133, 155
No Connect (N.C.)	A1, A2, A14, A15, R1, R2, R14, R15	1, 11, 39,54, 67, 82, 110, 120
Total User I/O Pins	120	120

Table 16. EPM7192E I/O Pin-Outs (Part 1 of 2)

MC	LAB	160-Pin PGA	160-Pin QFP	MC	LAB	160-Pin PGA	160-Pin QFP	MC	LAB	160-Pin PGA	160-Pin QFP
1	A	M12	156	17	B	L14	8	33	C	H14	21
2	A	–	–	18	B	–	–	34	C	–	–
3	A	P11	154	19	B	M14	7	35	C	J13	20
4	A	–	–	20	B	–	–	36	C	–	–
5	A	P12	153	21	B	M15	6	37	C	H15	19
6	A	P10	152	22	B	N14	5	38	C	J15	17
7	A	–	–	23	B	–	–	39	C	–	–
8	A	R12	151	24	B	N15	4	40	C	J14	16
9	A	N10	150	25	B	P15	2	41	C	K15	15
10	A	–	–	26	B	–	–	42	C	–	–
11	A	R11	149	27	B	N13	160	43	C	K13	14
12	A	–	–	28	B	–	–	44	C	–	–
13	A	R10	147	29	B	P14	159	45	C	L15	13
14	A	P9	146	30	B	P13	158	46	C	K14	12
15	A	–	–	31	B	–	–	47	C	–	–
16	A	R9	145	32	B	R13	157	48	C	L13	9
49	D	D15	33	65	E	B12	45	81	F	D8	60
50	D	–	–	66	E	–	–	82	F	–	–
51	D	E15	31	67	E	B13	44	83	F	A9	59
52	D	–	–	68	E	–	–	84	F	–	–
53	D	E14	30	69	E	C13	43	85	F	C8	58
54	D	F15	29	70	E	B14	42	86	F	B9	53
55	D	–	–	71	E	–	–	87	F	–	–
56	D	F13	28	72	E	C14	41	88	F	A10	52
57	D	G14	27	73	E	D12	38	89	F	B10	51
58	D	–	–	74	E	–	–	90	F	–	–
59	D	F14	26	75	E	B15	37	91	F	A11	50
60	D	–	–	76	E	–	–	92	F	–	–
61	D	G13	24	77	E	D14	36	93	F	B11	49
62	D	G15	23	78	E	C15	35	94	F	A12	48
63	D	–	–	79	E	–	–	95	F	–	–
64	D	H13	22	80	E	E13	34	96	F	A13	46

Table 16. EPM7192E I/O Pin-Outs (Part 2 of 2)

MC	LAB	160-Pin PGA	160-Pin QFP	MC	LAB	160-Pin PGA	160-Pin QFP	MC	LAB	160-Pin PGA	160-Pin QFP
97	G	A8	61	113	H	A3	76	129	I	E3	88
98	G	–	–	114	H	–	–	130	I	–	–
99	G	B8	62	115	H	B4	77	131	I	F3	90
100	G	–	–	116	H	–	–	132	I	–	–
101	G	A7	63	117	H	B3	78	133	I	E2	91
102	G	A6	68	118	H	C3	79	134	I	F2	92
103	G	–	–	119	H	–	–	135	I	–	–
104	G	B7	69	120	H	B2	80	136	I	E1	93
105	G	A5	70	121	H	B1	83	137	I	G3	94
106	G	–	–	122	H	–	–	138	I	–	–
107	G	B6	71	123	H	C2	84	139	I	F1	95
108	G	–	–	124	H	–	–	140	I	–	–
109	G	A4	72	125	H	C1	85	141	I	G1	97
110	G	B5	73	126	H	D2	86	142	I	G2	98
111	G	–	–	127	H	–	–	143	I	–	–
112	G	D4	75	128	H	D1	87	144	I	H1	99
145	J	H2	100	161	K	L2	113	177	L	R3	125
146	J	–	–	162	K	–	–	178	L	–	–
147	J	J1	101	163	K	N1	114	179	L	R4	127
148	J	–	–	164	K	–	–	180	L	–	–
149	J	H3	102	165	K	L3	115	181	L	M4	128
150	J	J3	104	166	K	P1	116	182	L	R5	129
151	J	–	–	167	K	–	–	183	L	–	–
152	J	K1	105	168	K	M2	117	184	L	P5	130
153	J	J2	106	169	K	N2	119	185	L	R6	131
154	J	–	–	170	K	–	–	186	L	–	–
155	J	K2	107	171	K	P2	121	187	L	P6	132
156	J	–	–	172	K	–	–	188	L	–	–
157	J	K3	108	173	K	N3	122	189	L	N6	134
158	J	L1	109	174	K	P3	123	190	L	R7	135
159	J	–	–	175	K	–	–	191	L	–	–
160	J	M1	112	176	K	P4	124	192	L	P7	136

Table 17. EPM7256E Dedicated Pin-Outs

Dedicated Pin	160-Pin QFP *(1)*	192-Pin PGA	208-Pin QFP
INPUT/GCLK1	139	P9	184
INPUT/GCLR*n*	141	R9	182
INPUT/OE1	140	T9	183
INPUT/OE2/GCLK2	142	U9	181
GND	3, 18, 32, 47, 57, 64, 66, 81, 96, 111, 126, 138, 143, 148	C7, C13, D4, D8, D10, G14, H4, K14, L4, P8, P10, P15, R4, R11	14, 32, 50, 72, 75, 82, 94, 116, 134, 152, 174, 180, 185, 200
VCCINT (5.0 V only)	56, 65, 137, 144	D7, D11, P7, P11	74, 83, 179, 186
VCCIO (3.3 V or 5.0 V)	10, 25, 40, 55, 74, 89, 103, 118, 133, 155	C5, C11, D14, G4, H14, K4, L14, P3, R5, R14	5, 23, 41, 63, 85, 107, 125, 143, 165, 191
No Connect (N.C.)	–	–	1, 2, 51, 52, 53, 54, 103, 104, 105, 106, 155, 156, 157, 158, 207, 208.
Total User I/O Pins	128	160	160

Note:

(1) Be sure to perform a complete thermal analysis before committing a design to this device package. See *Operating Requirements for Altera Devices* in this data book for more information.

Table 18. EPM7256E I/O Pin-Outs (Part 1 of 4)

MC	LAB	160-Pin QFP	192-Pin PGA	208-Pin QFP	MC	LAB	160-Pin QFP	192-Pin PGA	208-Pin QFP
1	A	2	U17	153	17	B	12	N17	141
2	A	–	–	–	18	B	–	–	–
3	A	1	R16	154	19	B	11	M16	142
4	A	–	–	–	20	B	–	–	–
5	A	160	P14	159	21	B	9	M15	144
6	A	–	U16	160	22	B	–	P17	145
7	A	–	–	–	23	B	–	–	–
8	A	159	R15	161	24	B	8	N16	146
9	A	158	U15	162	25	B	7	R17	147
10	A	–	–	–	26	B	–	–	–
11	A	157	T15	163	27	B	6	P16	148
12	A	–	–	–	28	B	–	–	–
13	A	156	U14	164	29	B	5	T17	149
14	A	–	U13	166	30	B	–	N15	150
15	A	–	–	–	31	B	–	–	–
16	A	154	T14	167	32	B	4	T16	151
33	C	39	B17	108	49	D	49	A14	92
34	C	–	–	–	50	D	–	–	–
35	C	38	C15	109	51	D	48	B12	93
36	C	–	–	–	52	D	–	–	–
37	C	37	C17	110	53	D	46	B13	95
38	C	–	C16	111	54	D	–	A15	96
39	C	–	–	–	55	D	–	–	–
40	C	36	D17	112	56	D	45	B14	97
41	C	35	D15	113	57	D	44	A16	98
42	C	–	–	–	58	D	–	–	–
43	C	34	E17	114	59	D	43	C14	99
44	C	–	–	–	60	D	–	–	–
45	C	33	D16	115	61	D	42	B16	100
46	C	–	E15	117	62	D	–	B15	101
47	C	–	–	–	63	D	–	–	–
48	C	31	F16	118	64	D	41	A17	102

Table 18. EPM7256E I/O Pin-Outs (Part 2 of 4)

MC	LAB	160-Pin QFP	192-Pin PGA	208-Pin QFP	MC	LAB	160-Pin QFP	192-Pin PGA	208-Pin QFP
65	E	153	U12	168	81	F	21	J16	130
66	E	–	–	–	82	F	–	–	–
67	E	152	R13	169	83	F	20	J15	131
68	E	–	–	–	84	F	–	–	–
69	E	151	U11	170	85	F	19	K17	132
70	E	–	T13	171	86	F	–	J14	133
71	E	–	–	–	87	F	–	–	–
72	E	150	T11	172	88	F	17	K16	135
73	E	149	T12	173	89	F	16	K15	136
74	E	–	–	–	90	F	–	–	–
75	E	147	R12	175	91	F	15	L17	137
76	E	–	–	–	92	F	–	–	–
77	E	146	U10	176	93	F	14	L16	138
78	E	–	R10	177	94	F	–	M17	139
79	E	–	–	–	95	F	–	–	–
80	E	145	T10	178	96	F	13	L15	140
97	G	30	E16	119	113	H	60	C9	79
98	G	–	–	–	114	H	–	–	–
99	G	29	F17	120	115	H	59	D9	80
100	G	–	–	–	116	H	–	–	–
101	G	28	F15	121	117	H	58	C10	81
102	G	–	G16	122	118	H	–	A10	84
103	G	–	–	–	119	H	–	–	–
104	G	27	G15	123	120	H	54	A11	86
105	G	26	G17	124	121	H	53	B10	87
106	G	–	–	–	122	H	–	–	–
107	G	24	H17	126	123	H	52	A12	88
108	G	–	–	–	124	H	–	–	–
109	G	23	H15	127	125	H	51	B11	89
110	G	–	J17	128	126	H	–	A13	90
111	G	–	–	–	127	H	–	–	–
112	G	22	H16	129	128	H	50	C12	91

Table 18. EPM7256E I/O Pin-Outs (Part 3 of 4)

MC	LAB	160-Pin QFP	192-Pin PGA	208-Pin QFP	MC	LAB	160-Pin QFP	192-Pin PGA	208-Pin QFP
129	I	128	U6	197	145	J	100	J2	27
130	I	–	–	–	146	J	–	–	–
131	I	129	T5	196	147	J	101	J3	26
132	I	–	–	–	148	J	–	–	–
133	I	130	U7	195	149	J	102	K1	25
134	I	–	T6	194	150	J	–	J4	24
135	I	–	–	–	151	J	–	–	–
136	I	131	T7	193	152	J	104	K2	22
137	I	132	R6	192	153	J	105	K3	21
138	I	–	–	–	154	J	–	–	–
139	I	134	R7	190	155	J	106	L1	20
140	I	–	–	–	156	J	–	–	–
141	I	135	U8	189	157	J	107	L2	19
142	I	–	R8	188	158	J	–	M1	18
143	I	–	–	–	159	J	–	–	–
144	I	136	T8	187	160	J	108	L3	17
161	K	91	F3	38	177	L	61	B9	78
162	K	–	–	–	178	L	–	–	–
163	K	92	F1	37	179	L	62	C8	77
164	K	–	–	–	180	L	–	–	–
165	K	93	E2	36	181	L	63	A9	76
166	K	–	G2	35	182	L	–	A8	73
167	K	–	–	–	183	L	–	–	–
168	K	94	G3	34	184	L	67	A7	71
169	K	95	G1	33	185	L	68	B8	70
170	K	–	–	–	186	L	–	–	–
171	K	97	H1	31	187	L	69	A6	69
172	K	–	–	–	188	L	–	–	–
173	K	98	H3	30	189	L	70	B7	68
174	K	–	J1	29	190	L	–	A5	67
175	K	–	–	–	191	L	–	–	–
176	K	99	H2	28	192	L	71	C6	66

Table 18. EPM7256E I/O Pin-Outs (Part 4 of 4)

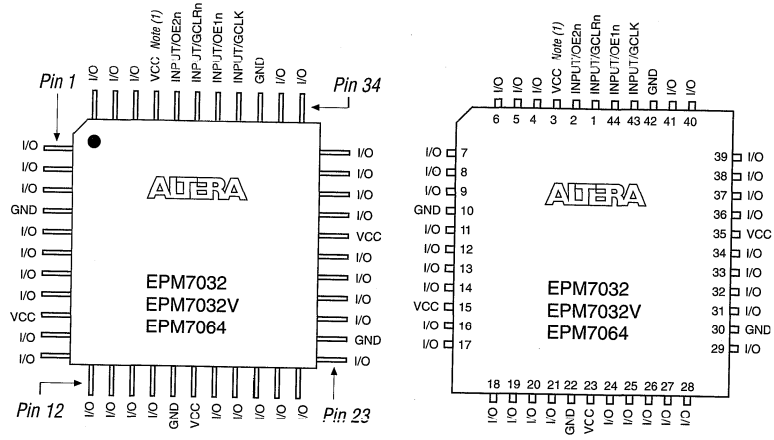
MC	LAB	160-Pin QFP	192-Pin PGA	208-Pin QFP	MC	LAB	160-Pin QFP	192-Pin PGA	208-Pin QFP
193	M	119	U1	4	209	N	109	N1	16
194	M	–	–	–	210	N	–	–	–
195	M	120	R2	3	211	N	110	M2	15
196	M	–	–	–	212	N	–	–	–
197	M	121	R3	206	213	N	112	M3	13
198	M	–	U2	205	214	N	–	P1	12
199	M	–	–	–	215	N	–	–	–
200	M	122	P4	204	216	N	113	N2	11
201	M	123	U3	203	217	N	114	R1	10
202	M	–	–	–	218	N	–	–	–
203	M	124	T3	202	219	N	115	P2	9
204	M	–	–	–	220	N	–	–	–
205	M	125	U4	201	221	N	116	T1	8
206	M	–	U5	199	222	N	–	N3	7
207	M	–	–	–	223	N	–	–	–
208	M	127	T4	198	224	N	117	T2	6
225	O	82	B1	49	241	P	72	A4	65
226	O	–	–	–	242	P	–	–	–
227	O	83	C3	48	243	P	73	B6	64
228	O	–	–	–	244	P	–	–	–
229	O	84	C1	47	245	P	75	B5	62
230	O	–	D3	46	246	P	–	A3	61
231	O	–	–	–	247	P	–	–	–
232	O	85	D1	45	248	P	76	B4	60
233	O	86	C2	44	249	P	77	A2	59
234	O	–	–	–	250	P	–	–	–
235	O	87	E1	43	251	P	78	C4	58
236	O	–	–	–	252	P	–	–	–
237	O	88	E3	42	253	P	79	B2	57
238	O	–	D2	40	254	P	–	B3	56
239	O	–	–	–	255	P	–	–	–
240	O	90	F2	39	256	P	80	A1	55

Pin-Out Diagrams

Figures 17 through 22 show the package pin-out diagrams of MAX 7000 devices.

Figure 17. 44-Pin Package Pin-Out Diagram

Package outlines not drawn to scale.



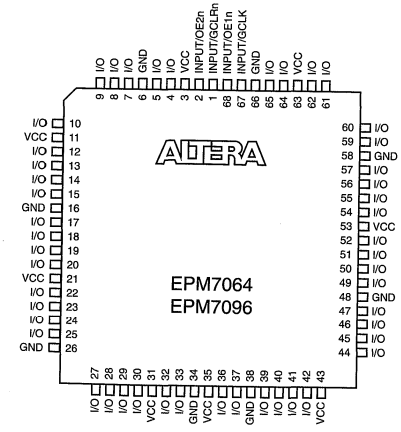
44-Pin QFP

44-Pin J-Lead

Note:
(1) Pin 41 ia a power-down pin (PDn) for the EMP7032V device.

Figure 18. 68-Pin Package Pin-Out Diagram

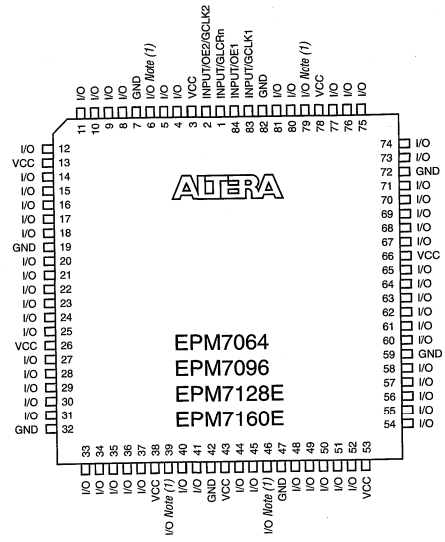
Package outline not drawn to scale.



68-Pin J-Lead

Figure 19. 84-Pin Package Pin-Out Diagram

Package outline not drawn to scale.

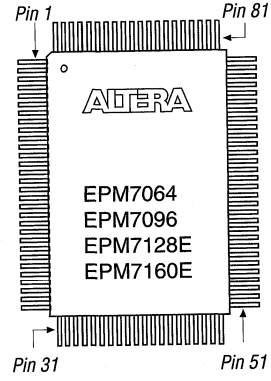


84-Pin J-Lead

Note:
(1) Pins 6, 39, 46, and 79 are no-connect (N.C.) pins on EPM7096 and EPM7160E devices.

Figure 20. 100-Pin Package Pin-Out Diagram

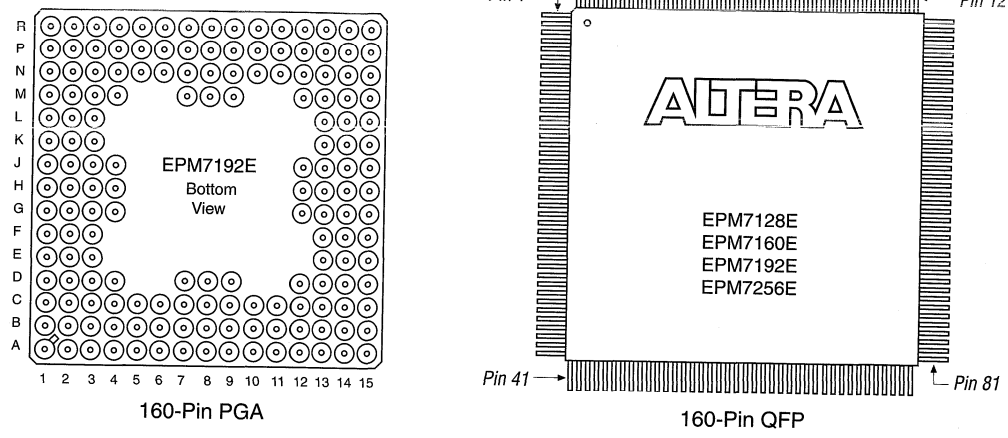
Package outline not drawn to scale.



100-Pin QFP

Figure 21. 160-Pin Package Pin-Out Diagram.

Package outline not drawn to scale.

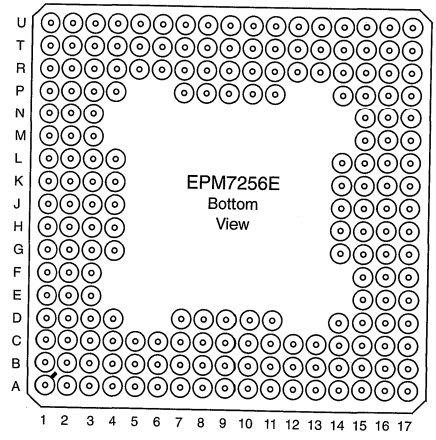


160-Pin PGA

160-Pin QFP

Figure 22. 192-Pin Package Pin-Out Diagram

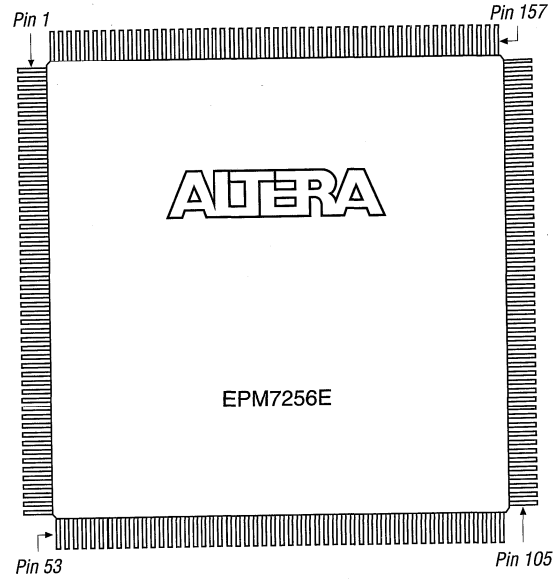
Package outline not drawn to scale.



192-Pin PGA

Figure 23. 208-Pin Package Pin-Out Diagram

Package outline not drawn to scale.



208-Pin QFP

Notes:

MAX 7000S

Programmable Logic Device Family

March 1995, ver. 2 — Advance Information Brief

Features...

- High-performance, EEPROM-based programmable logic devices (PLDs) based on second-generation Multiple Array MatriX (MAX) architecture
- Fabricated on a 0.5-micron, triple-layer-metal CMOS technology
- Support for in-system programmability (ISP)
- Superset version of the popular MAX 7000 family
- Pin-, function-, and programming file-compatible with all MAX 7000 devices (including MAX 7000E)
- Enhanced features (including 6 Output Enable controls, 2 global Clocks, fast input registers, and programmable slew rate) for all family members
- Open-collector output option
- Built-in Joint Test Action Group (JTAG) boundary-scan test (BST) circuitry in devices with 128 or more macrocells
- 5-ns delays with up to 178.6-MHz counter frequencies (including interconnect)
- PCI-compliant devices available in -5, -6, and -7 speed grades
- Programmable power-saving mode for 50% or greater power reduction in each macrocell
- Programmable macrocell flipflops with individual Clear, Preset, Clock, and Clock Enable controls

Preliminary Information

Table 1. MAX 7000S Devices

Feature	EPM7032S	EPM7064S	EPM7096S	EPM7128S	EPM7160S	EPM7192S	EPM7256S
6 Output Enables	✓	✓	✓	✓	✓	✓	✓
2 global Clocks	✓	✓	✓	✓	✓	✓	✓
Fast input registers	✓	✓	✓	✓	✓	✓	✓
Slew rate control	✓	✓	✓	✓	✓	✓	✓
ISP	✓	✓	✓	✓	✓	✓	✓
Open-collector output option	✓	✓	✓	✓	✓	✓	✓
JTAG BST circuitry				✓	✓	✓	✓

...and More Features

- Configurable expander product-term distribution, allowing up to 32 product terms per macrocell
- Programmable Security Bit for total protection of proprietary designs
- 3.3-V or 5.0-V I/O on all devices (except 44-pin packages)
- 44 to 208 pins available in J-lead (PLCC), pin-grid array (PGA), quad flat pack (QFP), and 1-mm thin quad flat pack (TQFP) packages

For more information on MAX 7000S devices contact Altera Marketing at (408) 894-7104.

March 1995

FLASHlogic Programmable Logic Device Family


ALTERA
FLASHlogic
EPX740LC68-10
ALTERA
FLASHlogic
EPX880QC160-10
PCI
ALTERA
FLASHlogic
EPX8160QC208-10
PCI

FLASHlogic

Programmable Logic Device Family

March 1995, ver. 1 Data Sheet

Features...

Preliminary Information

- Formerly Intel's FLEXlogic (iFX) family
- High-performance programmable logic device (PLD) family
  - SRAM-based logic with shadow EPROM or FLASH memory elements fabricated on 0.6- and 0.8-micron CMOS technology
  - Logic densities from 800 usable gates (1,600 available gates) to 3,200 usable (6,400 available) gates (see Table 1)
  - Combinatorial speeds with t_{PD} as low as 10 ns
  - Counter frequencies of up to 83.3 MHz
- 4 to 16 Logic Array Blocks (LABs) linked by a 100%-connectable Programmable Interconnect Array (PIA) for improved fitting of complex designs
- 24V10 macrocell features available
  - Dual feedback on all I/O pins
  - Product-term allocation matrix supporting up to 16 product terms per macrocell
  - Programmable registers providing D, T, SR, and JK flipflop functionality with Clear, Preset, and Clock controls
  - Fast 12-bit identity compare option
- EPX880 and EPX8160 devices are fully compliant with *PCI Local Bus Specification.*

Table 1. FLASHlogic Device Features

Feature	EPX740	EPX780	EPX880 *(1)*	EPX8160
Available gates	1600	3,200	3,200	6,400
Usable gates	800	1,600	1,600	3,200
Maximum SRAM bits	5,120	10,240	10,240	20,480
Macrocells	40	80	80	160
Package options (maximum user I/O pins)	44-pin PLCC (32) 68-pin PLCC (52)	84-pin PLCC (62) 132-pin QFP (104)	84-pin PLCC (62) 160-pin QFP (104)	208-pin QFP (172)
t_{PD} (ns)	10	10	10	10
t_{CO} (ns)	6	6	6	6
f_{CNT} (MHz)	83.3	83.3	80	80

Note:
(1) All data for EPX880 devices are preliminary.

... and More Features

- LABs can be configured as either of the following:
  - 24V10 logic block with 10 macrocells
  - 128 X 10 SRAM block
- 3.3-V or 5.0-V I/O on all devices (selectable in each LAB)
- Low Power Consumption:
  - Low-power EPX740Z and EPX780Z versions available (1 mA/MHz in standby mode; 1.0 to 1.5 mA/MHz in active mode)
  - Low-power EPX880 and EPX8160 (1 mA/MHz in standby mode; 1.5 to 2.5 mA/MHz in active mode)
- 44 to 208 pins available in plastic J-lead (PLCC) and quad flat pack (QFP) packages (see Table 1)
- Open-drain output option
- JTAG IEEE 1149.1-compatible test port supporting:
  - Boundary-scan testing (BST)
  - In-circuit reconfigurability (ICR)
  - In-system programmability (ISP)
- Programmable Security Bit for total protection of proprietary designs
- Supported by industry-standard design and programming tools from Altera and other vendors

General Description

Formerly Intel's FLEXlogic (iFX) device family, FLASHlogic devices are SRAM-based devices with shadow EPROM (EPX740, EPX780) or shadow FLASH (EPX880, EPX8160) memory elements. Fabricated on advanced 0.6- and 0.8-micron CMOS technology, FLASHlogic devices provide from 800 to 3,200 usable gates, pin-to-pin delays as fast as 10 ns, and counter speeds of up to 83.3 MHz. Table 2 shows the available speed grades for FLASHlogic devices.

Table 2. FLASHlogic Speed Grades

Device	Available Speed Grades *Notes (1), (2)*				
	-10Z	-10	-12	-15Z	-15
EPX740	✓	✓	✓	✓	✓
EPX780	✓	✓	✓	✓	✓
EPX880		✓ *(3)*	✓ *(3)*		
EPX8160		✓	✓		

Notes:
(1) The speed grade number after the dash refers to t_{PD} in ns.
(2) The Z after the speed grade indicates a low-power device.
(3) Information for this speed grade is preliminary.

FLASHlogic devices have a unique combination of features that is ideal for a variety of applications, including communications and bus interface controllers. They provide low power consumption and user-selectable 5.0-V and 3.3-V outputs. Therefore, they are good candidates for mixed-voltage applications such as portable and embedded systems.

FLASHlogic device architecture supports 100% TTL emulation and high-density integration of SSI, MSI, and LSI logic functions. It easily integrates multiple programmable logic devices ranging from PALs, GALs, and 22V10s to MACH, pLSI, and FPGA devices. With speed, density, and I/O resources comparable to commonly used masked gate arrays, FLASHlogic devices are ideal for gate array prototyping and PC applications. In addition, the -10 speed grade of the EPX880 and EPX8160 devices are PCI-compliant.

FLASHlogic devices are available in a range of packages, including plastic J-lead chip carrier (PLCC) and plastic quad flat pack (PQFP) packages.

FLASHlogic devices contain 4 to 16 Logic Array Blocks (LABs) linked by a Programmable Interconnect Array (PIA). Each LAB can be defined either as a 24V10 logic block of 10 macrocells or as a 128 × 10 SRAM block. When defined as a 24V10 logic block, all 10 macrocells have a programmable-AND/allocatable-OR array and a configurable register with independently programmable Clock, Clear, and Preset functions. To build complex logic functions, product-term allocation allows up to 16 product terms for a single macrocell.

FLASHlogic devices provide dedicated pins compliant with the JTAG IEEE 1149.1 specification. The JTAG pins support boundary-scan testing, in-circuit reconfigurability (ICR), and in-system programmability (ISP). ICR and ISP offer the designer greater flexibility in prototyping new designs. These features make FLASHlogic devices ideal for applications in which the final configuration is not fixed.

FLASHlogic devices are supported by industry-standard PC- and workstation-based EDA tools, including the Altera PLDshell Plus development system. In addition, MAX+PLUS II currently provides programming-only support for FLASHlogic devices; full-compilation support will be available in the second half of 1995.

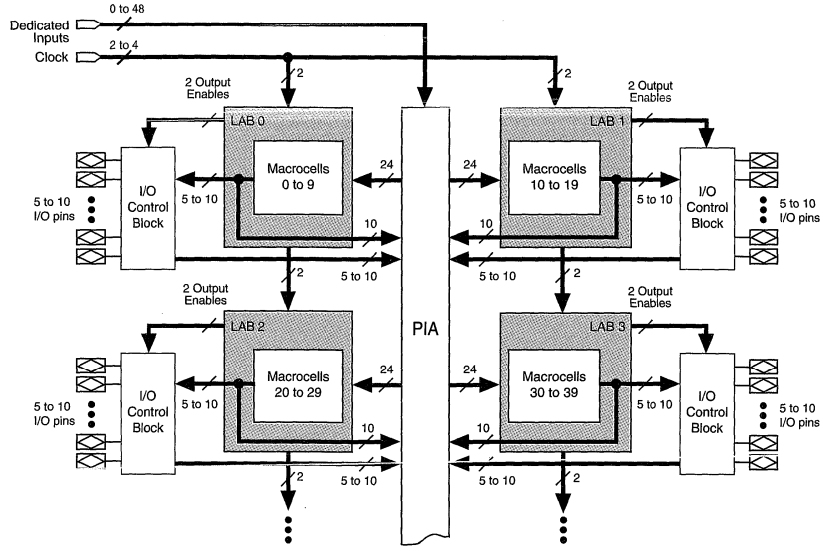
Functional Description

FLASHlogic device architecture includes the following elements:

- Logic Array Blocks
  - 24V10 configuration
  - SRAM configuration
- Programmable Interconnect Array
- I/O control blocks

Figure 1 shows the block diagram of the device architecture, which consists of LABs linked by a 100%-connectable PIA.

Figure 1. FLASHlogic Architecture



Logic Array Block

FLASHlogic device architecture is based on high-performance, flexible Logic Array Blocks (LABs). Each LAB can be configured as a 24V10 logic block or as a 128 × 10 SRAM block. The LABs are linked via the PIA, which is fed by all dedicated inputs, I/O pins, and either macrocells (in 24V10 configuration) or SRAM outputs (in SRAM configuration). Each LAB is fed by 24 signals from the PIA and 2 global Clocks.

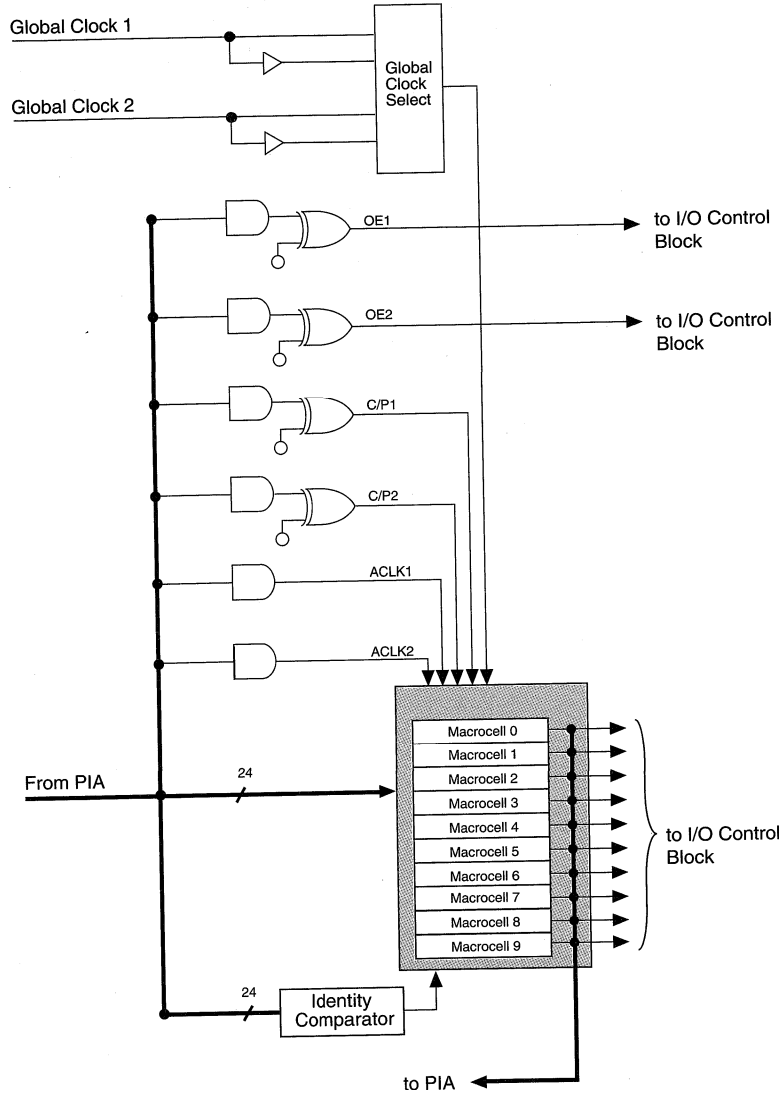
24V10 Configuration

When the LAB is configured as a 24V10 block, each block contains the following elements:

- 10 macrocells
- 12-bit identity comparator
- 2 global Clocks
- I/O logic
- Control logic for array Clocks and for Clear, Preset, and Output Enable signals

Figure 2 shows a diagram of the LAB configured as a 24V10 logic block.

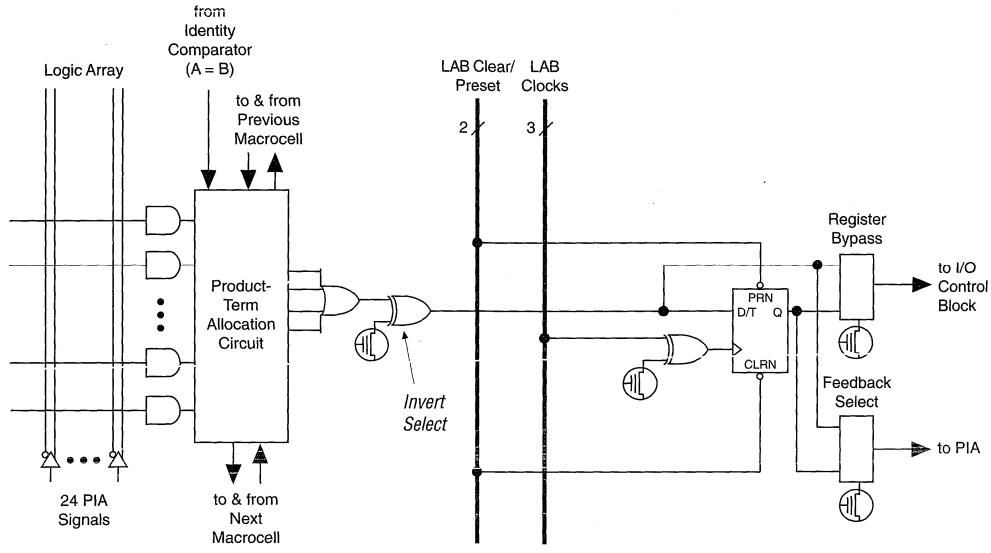
Figure 2. LAB in 24V10 Configuration



Macrocells

Each FLASHlogic macrocell can be individually configured for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term allocation circuit, and the programmable register. See Figure 3.

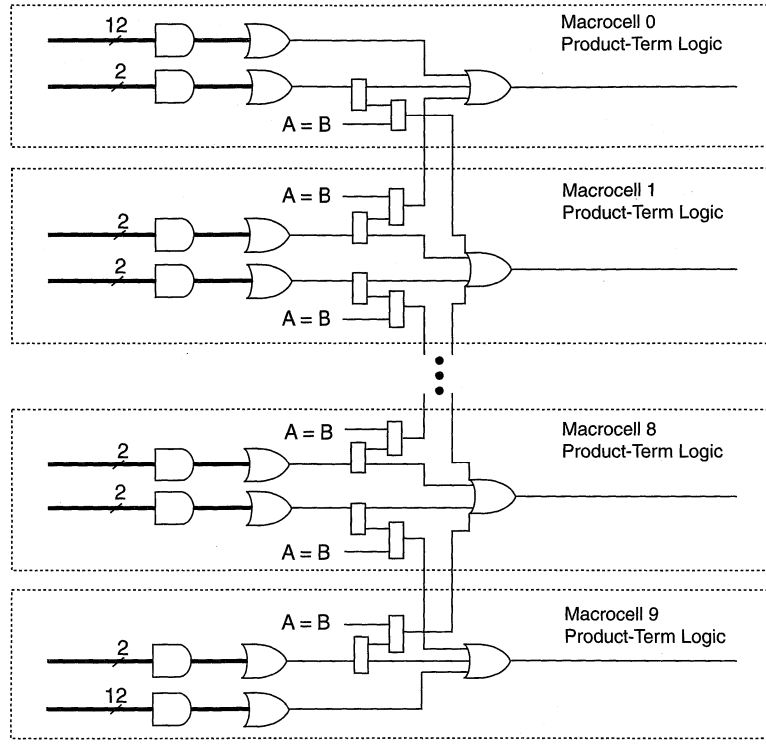
Figure 3. FLASHlogic Macrocell



Combinatorial logic is implemented in the logic array. Within the logic array, product terms are grouped into 2 sets of 2 product terms per macrocell. Each macrocell can borrow from its adjacent macrocells to increase the total number of product terms per macrocell to a maximum of 8. In addition, the macrocells located at the ends of each LAB have access to additional product terms and can support up to 16 product-term equations. The performance of each macrocell is uniform regardless of whether 2 or 16 product terms are used. Figure 4 shows the flexible product-term-allocation circuit.

In registered functions, each macrocell flipflop can be individually programmed to implement D, T, JK, or SR operation with programmable Clock, Preset, and Clear controls. If necessary, the register can be bypassed for combinatorial operation.

Figure 4. LAB Product-Term Allocation



Each LAB supports a global Clock and two array Clock signals. Global clocking is provided by either of two global clock signals or two delayed versions of these signals. Array clocking is provided by two LAB product terms. Each register in the LAB can then be clocked by the true or the complement of any two of these three Clock signals.

Each programmable register can be clocked in three different modes:

- Synchronous mode, by either of two global Clock signals. This mode achieves the fastest Clock-to-output performance.
- Delayed synchronous mode, by either of two global Clock signals with an added local delay (within the LAB).
- Array mode, by either of two array Clocks implemented with a product term. In this mode, the register can be clocked by signals from buried macrocells.

These clocking modes give FLASHlogic devices more timing flexibility enabling the designer to vary the setup time, hold time, and Clock-to-output time of each register. See Table 3. These modes are particularly useful for integrating devices with short-setup-time microprocessors, such as a Pentium microprocessor.

Table 3. EPX780-10 Sample Clocking Modes

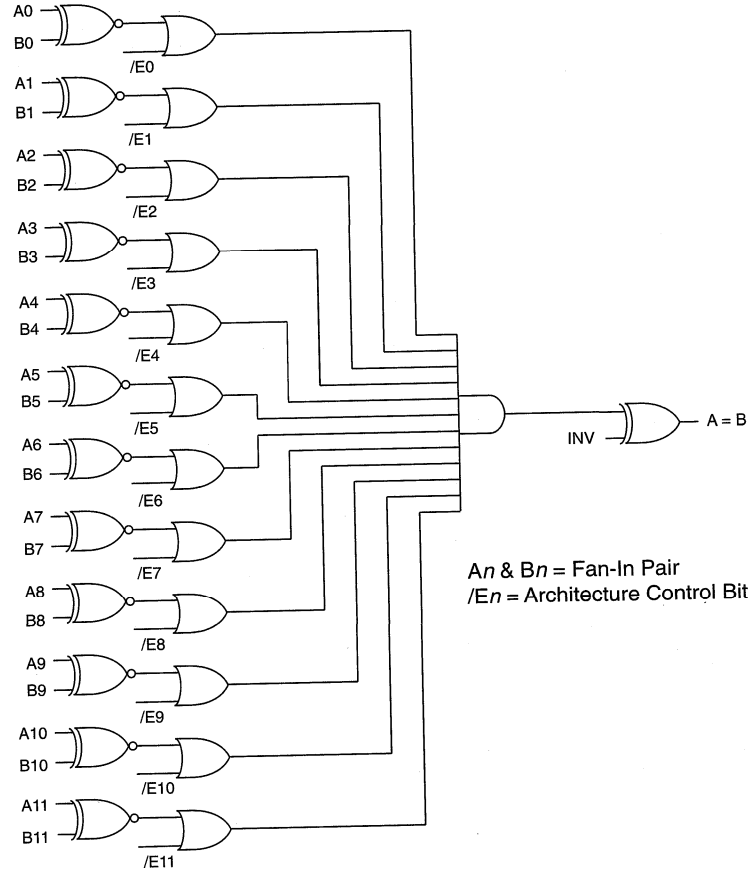
Clock Mode	Setup Time	Hold Time	Clock-to-Output Time	Unit
Synchronous	6	0	6	ns
Delayed Synchronous	4.5	2	8	ns
Array	2	5	12.5	ns

Each register also supports array Preset and Clear functions. These functions are driven by product terms and can be inverted. See Figure 2 on page 225 for a diagram of this logic.

Comparator Circuit

Each LAB also provides a comparator circuit that compares up to 12 pairs of inputs within the t_{PD} of the device. The product-term allocation matrix allows any one of the ten macrocells in the LAB to use the output of the comparator circuit. See Figure 5.

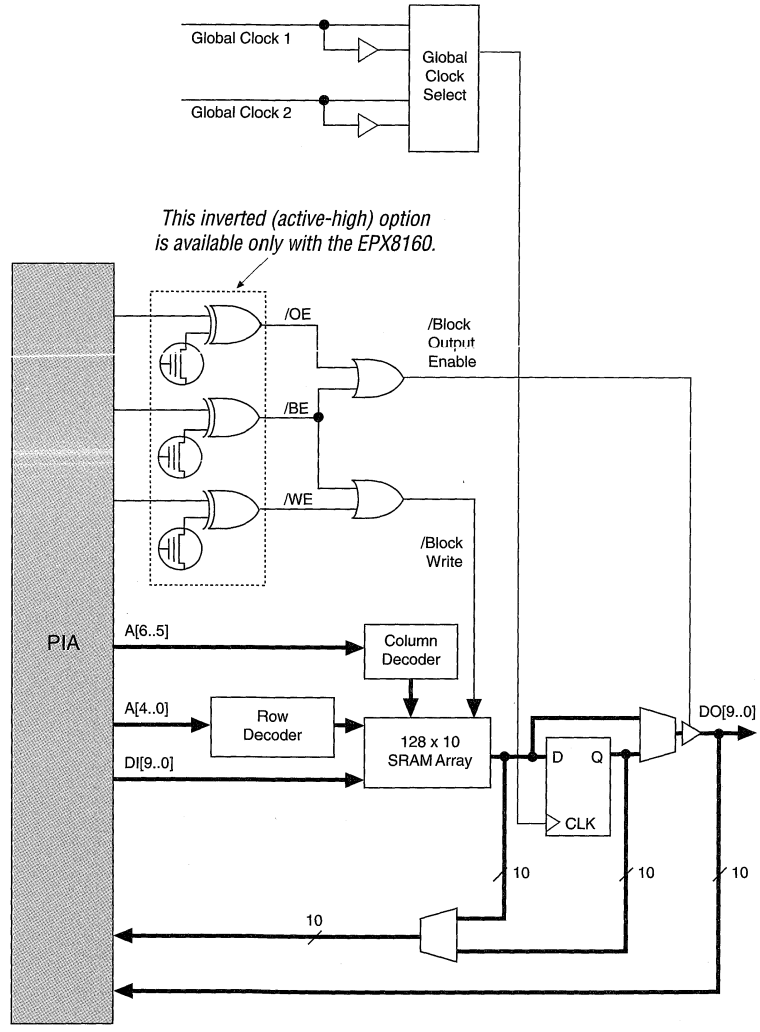
Figure 5. 12-Bit Identity Compare Logic



SRAM Configuration

Each FLASHlogic LAB can be configured as a 128 × 10 (128 words by 10 bits) SRAM block, as shown in Figure 6. The SRAM block can be defined with either a bidirectional I/O data bus or with separate input and output data buses.

Figure 6. LAB in SRAM Configuration



The SRAM is accessed using 24-signal fan-in: 7 bits are for address information; 10 bits are for data-in; 3 bits are for /BE (Block Enable), /WE, and /OE controls, as shown in Table 4.

Table 4. SRAM Functions

Inputs			Cycle	I/O Pins
/BE	/WE	/OE		
1	X	X	None	Disabled
0	1	1	Read	Disabled
0	1	0	Read	Enabled
0	0	1	Write	Disabled
0	0	0	Write	Enabled

During power-up, the SRAM memory elements are initialized by on-chip, nonvolatile configuration cells. During operation, the SRAM contains a copy of the information contained in the nonvolatile configuration cells, unless other data is written to these blocks. Therefore, the SRAM block can be used as read-only memory (ROM).

When a LAB is configured as SRAM, all product terms are used as SRAM blocks and cannot be used for regular macrocell logic. Multiple LABs can be cascaded to create larger SRAM blocks, thereby increasing the width or depth of the memory.

Programmable Interconnect Array

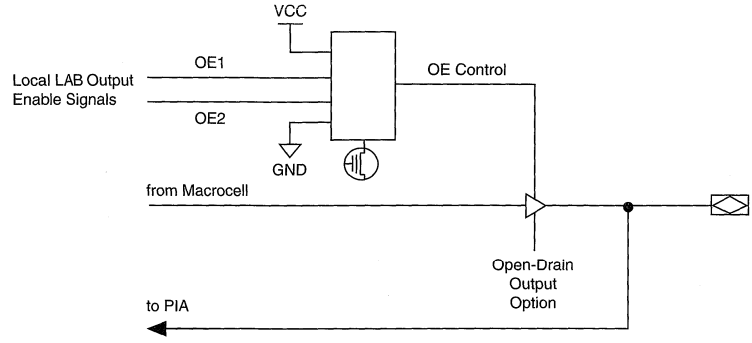
Signals are routed between LABs by the 100%-connectable Programmable Interconnect Array (PIA). This global bus connects any signal source to any destination on the device. All dedicated pins, I/O pins, and macrocell outputs feed into the PIA, and are accessible to all LABs. The high degree of connectivity and efficient resource management between LABs minimizes routing problems during design debugging.

The routing delays of channel-based routing schemes in masked or field-programmable gate arrays (FPGAs) are cumulative, variable, and path-dependent. In contrast, the FLASHlogic PIA has a fixed delay. Therefore, the PIA eliminates skew between signals, making timing and performance easy to predict.

I/O Control Blocks

The I/O control block allows each I/O pin to be individually configured for input, output, or bidirectional operation. All I/O pins have a tri-state buffer that is either individually controlled by one of the two local LAB Output Enable signals generated within each LAB, or directly connected to GND or V_{CC}. Figure 7 shows the I/O control block for FLASHlogic devices.

Figure 7. I/O Control Block for FLASHlogic Devices



When the tri-state buffer control is connected to GND, the output is tri-stated (high-impedance) and the I/O pin can be used as a dedicated input. When the tri-state buffer control is connected to V_{CC}, the output is enabled.

The FLASHlogic architecture provides dual I/O feedback in which macrocell and pin feedbacks are independent. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic.

Input Configuration

Device inputs, as well as I/O pins that are used as inputs, can be optimized for minimum standby current during either CMOS or TTL operation by using the `CMOS_LEVEL` keyword (for 5.0-V CMOS inputs) and the `TTL_LEVEL` keyword (for TTL or 3.3-V CMOS inputs) available in the PLDasm design language supported by PLDshell Plus. `TTL_LEVEL` is the default condition for PLDasm.

Output Configuration

FLASHlogic device outputs can be configured to meet a variety of system-level requirements.

3.3 V or 5.0 V Operation

The pins in an I/O control block can operate at 3.3 V or 5.0 V. This functionality enables the designer to mix 3.3-V outputs and 5.0-V inputs if the appropriate V_{CCO} pins are tied to a 3.3-V power supply. FLASHlogic devices require a V_{CC} of 5.0 V for normal operation. However, the V_{CCO} pin associated with each LAB pair can be connected to either 5.0 V or 3.3 V to control the output voltages of the I/O pins of that LAB pair. This feature allows FLASHlogic devices to be used in mixed-voltage systems. For example, the devices can be used as an interface between a 3.3-V CPU and 5.0-V peripheral logic.

Power sequencing is required when any or all LABs operate at 3.3-V levels. In other words, the voltage levels of the 5.0-V source must be greater than or equal to the 3.3-V source during power-up and power-down.

Open-Drain Output Option

FLASHlogic devices can be configured to provide an optional open-drain output for each I/O pin. If desired, complex equations can be implemented using multiple open-drain outputs with an externally supplied pull-up resistor to emulate an additional OR plane.

CMOS-Compatible Outputs

A weak pull-up resistor is provided for CMOS-compatible outputs. This resistor is always active in both 3.3-V and 5.0-V modes.

I/O Pull-Up Resistor

EPX8160 devices contain active-weak pull-up resistors on the I/O pins that hold the I/O at a logic high during power-up, reconfiguration, and erase/program cycles. This resistor is disabled during normal device operation to reduce power consumption. Dedicated inputs do not have active pull-up resistors.

High Drive I/O

EPX880 and EPX8160 output buffers are designed specifically for applications requiring high drive current. These buffers enable the devices to drive a bus (including PCI) and at the same time provide 10-ns pin-to-pin performance, eliminating the need for external buffers and their associated delays.

PCI Compliance

EPX880 and EPX8160 5.0-V output buffers are designed to meet the current-vs.-voltage specifications for PCI. EPX880-10 and EPX8160-10 devices also offer a predictable, 10-ns pin-to-pin propagation delay, a 6-ns Clock-to-signal valid delay, and a 6.5-ns synchronous setup time to meet the timing demands of PCI applications. To support bidirectional PCI signals, two Output Enable product terms are provided in each LAB, for a total of 32 in the device.

Go to *Application Note 41, (PCI Bus Applications in Altera Devices)* for more information on using EPX8160 devices in PCI applications.

JTAG Operation

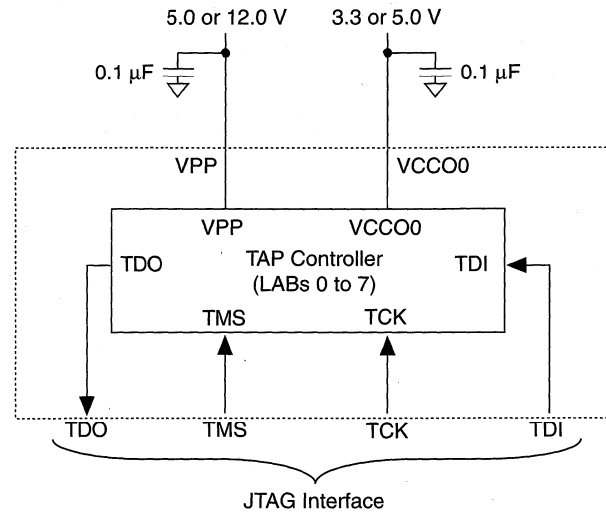
FLASHlogic devices support the JTAG IEEE 1149.1 standard boundary-scan testing (BST). The JTAG BST architecture enables fault-isolation testing of board designs at the device level, enhances production testing and field repair, and is ideal for fault-tolerant applications.

FLASHlogic BST support consists of an instruction register, a data register, scan cells, and associated logic, all of which are accessed through the Test Access Port (TAP). The TAP interface consists of three inputs—Test Mode Select (TMS), Test Data Input (TDI), and Test Clock Input (TCK)—and one output, Test Data Output (TDO).

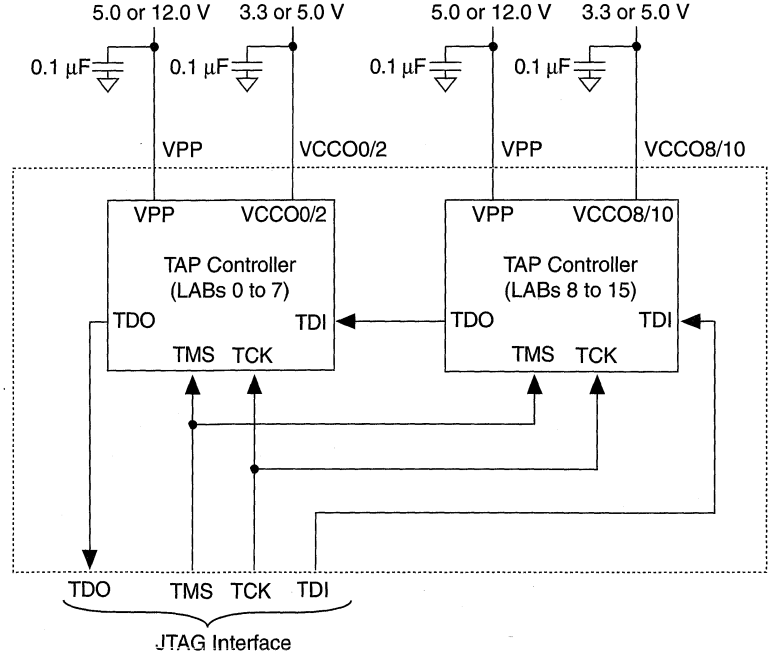
EPX740, EPX780, and EPX880 devices each contain one JTAG TAP controller; EPX8160 devices contain two JTAG TAP controllers. The JTAG TAP controllers support group (partial) reconfiguration, group reprogramming, and boundary-scan testing. Figure 8 shows the internal connection of the JTAG TAP controllers.

Figure 8. JTAG Connections of TAP Controllers

EPX740, EPX780 & EPX880



EPX8160



In FLASHlogic devices, the boundary-scan I/O pins are linked to form a shift register chain for all active pins. This chain provides a path that can be used to shift boundary-scan data into and out of the device.

For example, a continuity test can be performed between two JTAG devices on a circuit board by placing a known value on the output buffers of one device and observing the input buffers of the other device. The same technique can also be used to perform in-circuit functional testing of FLASHlogic devices for prototyping new system designs.

The 4-pin JTAG test interface is also used for standard programming, in-circuit reconfiguration, and in-system programming.

Boundary-Scan Instructions

The FLASHlogic boundary-scan instruction register (IR) supports the instruction opcodes and extended instruction opcodes used for the Program/Verify modes. (See Table 5).

Table 5. Instruction Opcodes

Name	IR Opcode (Binary) MSB..LSB	Description
EXTEST	00000	The EXTEST instruction drives the output pins to the values contained in the boundary-scan cells. The instruction tests the external circuitry used for printed circuit board interconnects.
BYPASS	11111	The BYPASS instruction selects the one-bit bypass register (BPR) to be connected to TDI and TDO.
SAMPLE/PRELOAD	00001	The SAMPLE/PRELOAD instruction is used for two functions: 1) to allow a snapshot of the values of the device pins in an unobtrusive manner, and 2) to preload data onto the device pins that are driven to the system circuit board when executing the EXTEST instruction.
IDCODE	00010	The IDCODE instruction selects the ID code register to be connected to TDI and TDO, allowing the ID code to be serially shifted out of TDO.
UESCODE	10110	The UESCODE instruction selects the User Electronic Signature (UES) register to be connected to TDI and TDO, allowing the UES code to be serially shifted out of TDO.
HIZ	01000	The HIZ instruction sets all I/O pins to a high-impedance state.

ICR & ISP

FLASHlogic devices support in-circuit reconfigurability (ICR). Using the 4-pin JTAG test port, a new configuration can be downloaded to the SRAM by simply shifting the new data into the device. Device reconfiguration can be repeated as many times as desired during prototyping.

Once the design is finalized, it can be programmed into the shadow EPROM or FLASH cells so that the configuration is not lost, even when the power is turned off. This capability is known as in-system programmability (ISP). Devices are programmed in-system using the JTAG test port and the programming voltage pins (V_{PP}). EPROM-based devices can be programmed once; FLASH-based devices can be programmed up to 100 times.

Go to *Application Note 45 (Configuring FLASHlogic Devices)* for more information on ICR.

Design Security

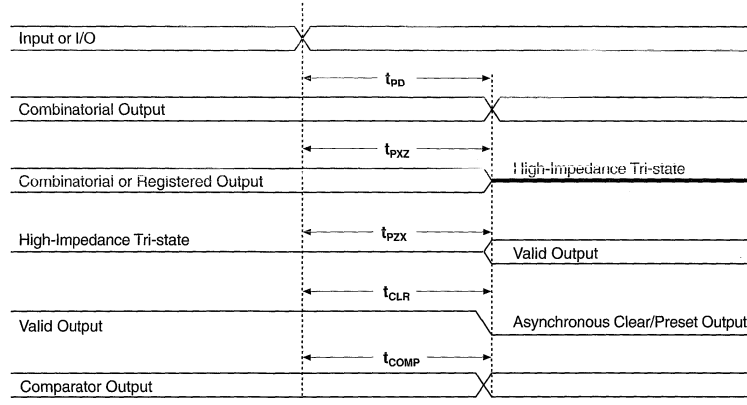
FLASHlogic devices contain a programmable Security Bit that controls access to the data programmed into the device. Once this Security Bit is set, the design cannot be read from the nonvolatile cells or the SRAM. The state of the nonvolatile Security Bit at power-up determines whether data programmed into the device can be accessed and changed by in-circuit reconfiguration.

Timing Model

FLASHlogic devices have fixed internal delays that allow the user to determine the worst-case timing for any design. Device timing can be analyzed with a variety of industry-standard EDA simulators and timing analyzers. Industry-standard EDA tools provide timing simulation, point-to-point delay prediction, and detailed analysis for system-level performance evaluation. (Full device support via MAX+PLUS II is planned for the second half of 1995.) External timing parameters represent pin-to-pin timing delays. Switching waveforms for these timing parameters (including SRAM read and SRAM write cycles) are shown in Figure 9.

Figure 9. Switching Waveforms (Part 1 of 2)

Combinatorial Mode



Registered Mode

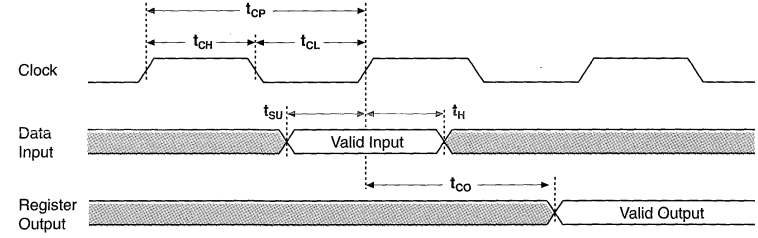
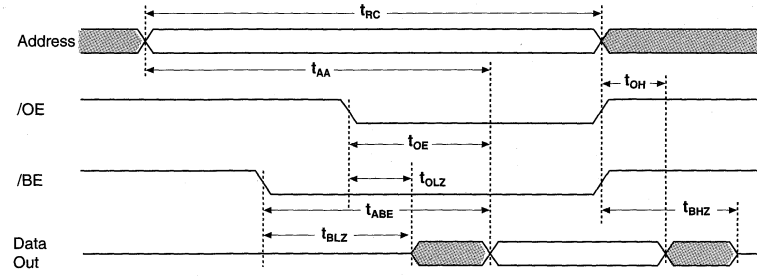
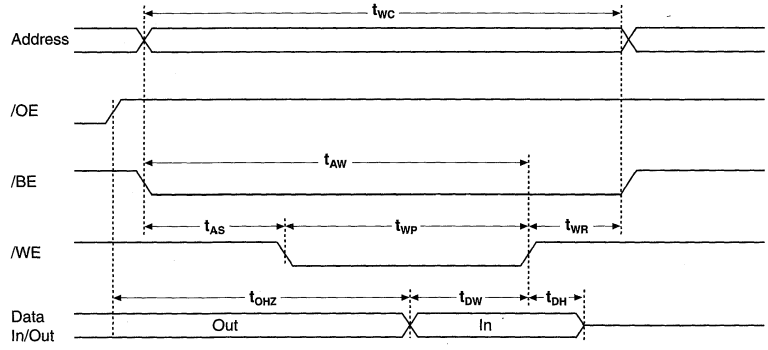


Figure 9. Switching Waveforms (Part 2 of 2)

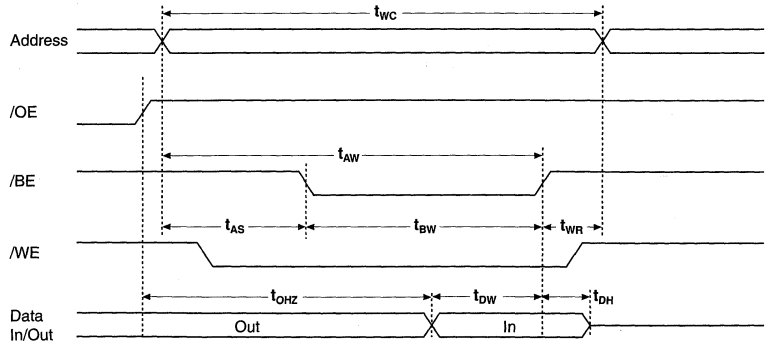
SRAM Read Cycle



SRAM Write Cycle 1 (/WE-Controlled Timing)



SRAM Write Cycle 2 (/BE-Controlled Timing)

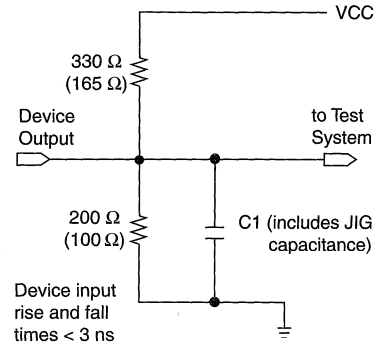


Generic Testing

FLASHlogic devices are fully functionally tested and guaranteed. Complete testing of each programmable FLASH or EPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in Figure 10. Test patterns can be used and erased during early stages of the device production flow.

Figure 10. FLASHlogic AC Test Conditions

Power-supply transients can affect AC measurements. For accurate measurements, avoid simultaneous transitions of multiple outputs. Do not perform threshold tests under AC conditions. Large-amplitude, fast ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, they can significantly reduce observable noise immunity. Numbers in parentheses are for EPX880 and EPX8160 devices.



Software Support

FLASHlogic devices are supported by industry-standard PC- and workstation-based EDA tools, including the Altera PLDshell Plus development system. In addition, MAX+PLUS II currently provides programming-only support; full compilation support is planned for the second half of 1995. See the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* in this data book for more information.

Go to the ***PLDshell Plus/PLDasm User's Guide*** for information on programming FLASHlogic devices using PLDshell.

Third-party software support is provided by the following vendors:

Table 6. Third-Party Software Support

Vendor	Software	Description
Data I/O	ABEL	Design software that describes and implements logic designs
Data I/O	Synario 2.0	Integrated text and graphic design and simulation environment
Logical Devices	CUPL	High-level, universal design software package
Minc	PLDesigner-XL(R)	Design tool for all types of programmable logic with automatic device selection, automatic partitioning, and functional simulation
OrCAD	PLD Tools and Schematic Design Tool	Includes schematic entry, test vector generation, and multiple forms of input
OrCAD	Verification and Simulation Tool	Series of software tools for performing timing-based simulation of designs
Viewlogic	Workview, PRO Series, and Powerview	Integrated schematic capture and simulation environments

Simulation models are provided by the following vendors:

- Synopsys SmartModel—Device model support for behavioral simulation through a variety of simulators
- Viewlogic—Simulation model for Viewlogic verification tools

Device Programming

FLASHlogic devices can be programmed with MAX+PLUS II software on 486- or Pentium-based PCs using an Altera Logic Programmer card, the Master Programming Unit (MPU), and the appropriate device adapter. The MPU performs continuity checking to ensure adequate electrical contact between the adapter and the device. See the *Altera Programming Hardware Data Sheet* in this data book for more information.

FLASHlogic devices can also be programmed in-system with PLDshell Plus software using Altera's FLASHlogic Download Cable (PL-FLDLC). Data I/O and other programming hardware manufacturers also provide programming support for FLASHlogic devices. See *Programming Hardware Manufacturers* in this data book for more information.

QFP Carrier & Development Socket

FLASHlogic devices in QFP packages with 160 or more pins can be ordered in plastic carriers to protect the fragile QFP leads. The carrier can be used with a prototype development socket and programming hardware available from Altera. This carrier makes it possible to program, test, erase, and reprogram a device without exposing the leads to mechanical stress.

Go to the *QFP Carrier & Development Socket Data Sheet* in this data book for more information.

Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND, *Note (2)*	–2.0	7.0	V
V_{PP}	Programming supply voltage: EPX740 & EPX780		–2.0	13.5	V
V_{PP}	Programming supply voltage: EPX880 & EPX8160		–2.0	12.6	V
V_I	DC input voltage		–0.5	V_{CC} + 0.5	V
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–10	85	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage: 5.0 V		4.75	5.25	V
V_{CCO}	Output supply voltage: 5.0 V		4.75	5.25	V
V_{CCO}	Output supply voltage: 3.3 V		3.0	3.6	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CCO}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
t_R	Input rise time			500	ns
t_F	Input fall time			500	ns

DC Operating Conditions *Note (3)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage		2.0	V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
V_{OH}	5.0-V TTL high-level output voltage	EPX740 & EPX780: I_{OH} = –4.0 mA DC, V_{CCO} = min. EPX880 & EPX8160: I_{OH} = –16.0 mA DC, V_{CCO} = min.	2.4		V
	5.0-V CMOS high-level output voltage	EPX740 & EPX780: I_{OH} = –20 µA DC, V_{CCO} = min. EPX880 & EPX8160: I_{OH} = –100 µA DC, V_{CCO} = min.	V_{CCO} – 0.2		V
	3.3-V high-level output voltage	EPX740 & EPX780: I_{OH} = –20 µA DC, V_{CCO} = min. EPX880 & EPX8160: I_{OH} = –100 µA DC, V_{CCO} = min.	V_{CCO} – 0.2		V
V_{OL}	5.0-V low-level output voltage	EPX740 & EPX780: I_{OL} = 12 mA DC, V_{CCO} = min. EPX880 & EPX8160: I_{OL} = 24 mA DC, V_{CCO} = min.		0.45	V
	3.3-V low-level output voltage	EPX740 & EPX780: I_{OL} = 20 µA DC, V_{CCO} = min. EPX880 & EPX8160: I_{OL} = 12 mA DC, V_{CCO} = min.		0.2	V
I_I	Input leakage current	V_{CCO} = max., GND < V_{IN} < V_{CCO}, *Note (4)*	–10	10	µA
I_{OZ}	Output leakage current	EPX740 & EPX780: V_{CCO} = max., GND < V_{OUT} < V_{CCO}	–50	50	µA
		EPX880 & EPX8160: V_{CCO} = max., V_{OUT} = V_{CCO}	–50	50	µA
		EPX880 & EPX8160: V_{CCO} = max., V_{OUT} = GND	–100	100	µA
I_{SC}	Output short circuit current, *Note (5)*	V_{CCO} = max., V_{OUT} = 0.5 V	–30	–120	mA

Programming Conditions *Notes (3), (6)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PP}	EPX740 & EPX780: programming voltage		12.5	12.75	13.00	V
	EPX880 & EPX8160: programming voltage		11.4	12	12.6	V
I_{PP1}	V_{PP} read current, IC current, or standby current	V_{PP} > V_{CC}		90	200	µA
		V_{PP} ≤ V_{CC}		15	40	µA
I_{PP2}	EPX740 & EPX780: V_{PP} programming or program verify current	V_{PP} = V_{PPH} Programming in progress		50	100	mA
	EPX880 & EPX8160: V_{PP} programming or program verify current	V_{PP} = V_{PPH} Programming in progress		30	60	mA
I_{PP3}	V_{PP} erase and erase verify current	V_{PP} = V_{PPH}		30	60	mA
E_{CNT}	Erase and reprogram count limit				100	

I_{CC} Supply Current Values *Note (7)*

Symbol	Parameter	Conditions	EPX740	EPX740Z	EPX780	EPX780Z	EPX880	EPX8160	Unit
I_{CC1}	V_{CC} supply current, (standby, typical)	V_{CC} = Max., V_{IN} = V_{CC} or GND, standby mode *Note (8)*	20	1	20	1	1	1	mA
I_{CC}	V_{CC} supply current, (active, typical)	V_{IN} = V_{CC} or GND, no load, *Note (8)*	1	1	1.5	1.5	1.5	2.5	mA/MHz

Capacitance *Notes (7), (9)*

Symbol	Parameter	Conditions	Typ	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 2 V, f = 1.0 MHz	10	12	pF
$C_{I/O}$	I/O pin capacitance	V_{OUT} = 2 V, f = 1.0 MHz	12	15	pF
C_{CLK}	Clock pin capacitance	V_{OUT} = 2 V, f = 1.0 MHz	15	18	pF
C_{VPP}	V_{PP} pin capacitance	f = 1.0 MHz	12	15	pF

Notes to tables:

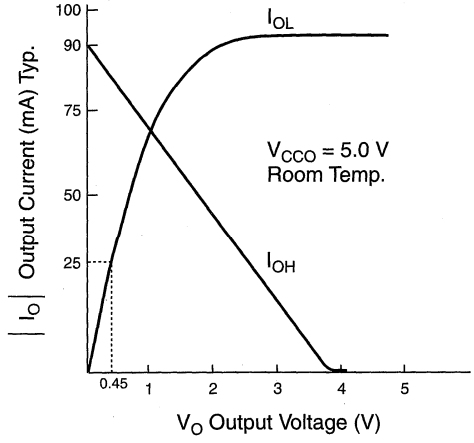
(1) See *Operating Requirements for Altera Devices* in this data book.
(2) The minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods of less than 20 ns under no-load conditions.
(3) Operating conditions: T_A = 0° C to 70° C, V_{CC} = 5.0 V ± 5% for commercial use.
T_A = –40° C to 85° C, V_{CC} = 5.0 V ± 10% for industrial use.
(4) Input leakage current on JTAG pins is tested at ± 20 µA.
(5) No more than 1 output should be tested at a time. The duration of the test should not exceed 1 second.
(6) Typical values are for T_A = 25° C, V_{CC} = 5.0 V, V_{PP} = 12.0 V.
(7) Typical values are for T_A = 25° C, V_{CC} = 5.0 V.
(8) Measured with a 20-bit, loadable, enabled, up/down counter programmed into each LAB pair.
(9) Capacitance measured at 25° C. Sample-tested only.

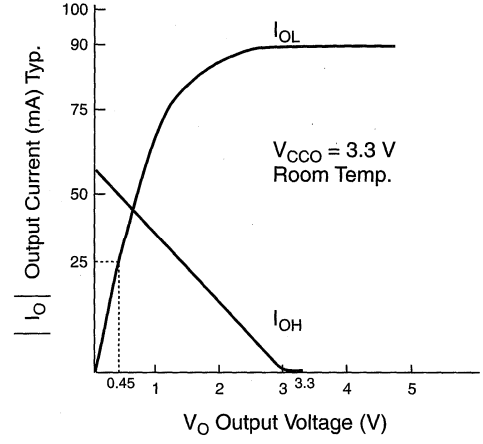
Figure 11 shows the typical output drive characteristics for FLASHlogic devices.

Figure 11. Output Drive Characteristics of FLASHlogic Devices

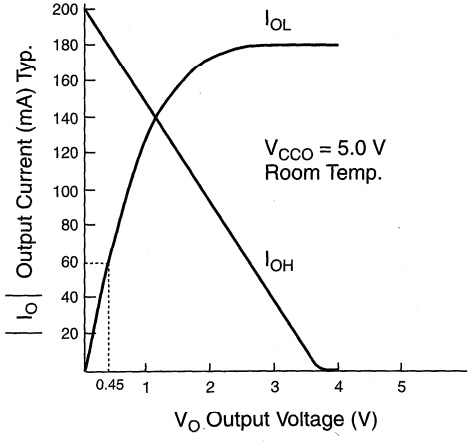
The output drive characteristics for EPX880 devices are preliminary.

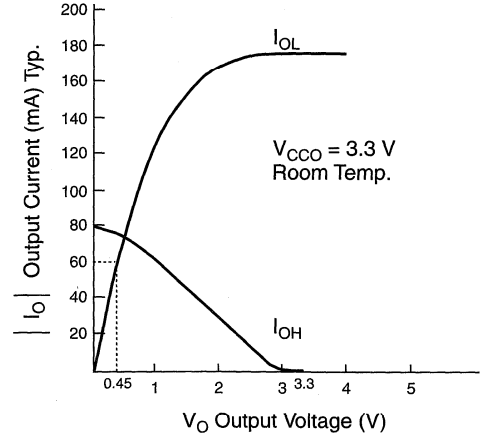
EPX740 & EPX780 Devices





EPX880 & EPX8160 Devices





AC Operating Characteristics: EPX740 & EPX780 *Note (1)*

External Timing Parameters / ***Combinatorial Mode***			EPX740-10Z EPX740-10 EPX780-10Z EPX780-10		EPX740-12 EPX780-12 *Note (2)*		EPX740-15Z EPX740-15 EPX780-15Z EPX780-15		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD}	Input or I/O to output valid	C1 = 35 pF		10		12		15	ns
t_{PZX}	Input or I/O to output enable	C1 = 35 pF		12		15		18	ns
t_{PXZ}	input or I/O to output disable	C1 = 5 pF		12		15		18	ns
t_{CLR}	Array output clear time			15		18		20	ns
t_{COMP}	Comparator input or I/O feedback to output valid			10		12		15	ns

External Timing Parameters / ***Register Mode—Synchronous Clock***			EPX740-10Z EPX780-10Z		EPX740-10 EPX780-10		EPX740-12 EPX780-12 *Note (2)*		EPX740-15Z EPX740-15 EPX780-15Z EPX780-15		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
f_{MAX}	Maximum frequency	*Note (3)*	100		100		80		66.7		MHz
t_{SU}	Input setup time		6		6		7.5		11		ns
t_{H}	Input hold time		0		0		0		0		ns
t_{CH}	Clock high time		4.5		4.5		5		7		ns
t_{CL}	Clock low time		4.5		4.5		5		7		ns
t_{CP}	Clock period		10		10		12.5		15		ns
t_{CO1}	Clock-to-output delay	C1 = 35 pF		6		6.5		7.5		9	ns
t_{CNT}	Minimum clock period			12		12.5		15		20	ns
f_{CNT}	Internal maximum frequency	*Note (4)*	83.3		80		66		50		MHz

External Timing Parameters / ***Register Mode—Delayed Synchronous Clock***			EPX740-10Z EPX780-10Z		EPX740-10 EPX780-10		EPX740-12 EPX780-12 *Note (2)*		EPX740-15Z EPX740-15 EPX780-15Z EPX780-15		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
f_{MAX}	Maximum frequency	*Note (3)*	92.9		92.9		74		62.5		MHz
t_{SU}	Input setup time		4.5		4.5		6		8		ns
t_{H}	Input hold time		2		2		2		2		ns
t_{CH}	Clock high time		4.5		4.5		5		7		ns
t_{CL}	Clock low time		4.5		4.5		5		7		ns
t_{CP}	Clock period		10.5		10.5		12.5		15		ns
t_{CO1}	Clock-to-output delay	C1 = 35 pF		8		8.5		10		12	ns
t_{CNT}	Minimum clock period			12.5		13		16		20	ns
f_{CNT}	Internal maximum frequency	*Note (4)*	80		76.9		62.5		50		MHz

External Timing Parameters			EPX740-10Z EPX780-10Z		EPX740-10 EPX780-10		EPX740-12 EPX780-12 *Note (2)*		EPX740-15Z EPX740-15 EPX780-15Z EPX780-15		
Register Mode—Array Clock											
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
f_{AMAX}	Maximum frequency	*Note (3)*	80		80		66		62.5		MHz
t_{ASU}	Input setup time		2		2		2.5		3		ns
t_{AH}	Input hold time		5		5		6		6		ns
t_{ACH}	Clock high time		5		5		6		7		ns
t_{ACL}	Clock low time		5		5		6		7		ns
t_{ACP}	Clock period		12.5		12		66		15		ns
t_{ACO}	Clock-to-output delay	C1 = 35 pF		12		12		14.5		17	ns
t_{ACNT}	Minimum clock period			13.5		14		17		20	ns
f_{ACNT}	Internal maximum frequency	*Note (4)*	71.4		71.4		58.8		50		MHz

External Timing Parameters			EPX740-10Z EPX740-10 EPX780-10Z EPX780-10		EPX740-12 EPX780-12 *Note (2)*		EPX740-15Z EPX740-15 EPX780-15Z EPX780-15		
SRAM Read									
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{RC}	Read cycle time		15		20		20		ns
t_{AA}	Address access time			15		20		20	ns
t_{ABE}	Block enable access time			15		20		20	ns
t_{OE}	Output enable to output valid	*Note (5)*		12		15		15	ns
t_{OH}	Output hold from address change		2		3		3		ns
t_{BLZ}	Block enable to output in low impedance	*Note (5)*	3		5		5		ns
t_{BHZ}	Block disable to output in high impedance	C1 = 5 pF, *Note (5)*		10		15		15	ns
t_{OLZ}	Output enable to output in low impedance	*Note (5)*	3		5		5		ns

External Timing Parameters		EPX740-10Z EPX740-10 EPX780-10Z EPX780-10		EPX740-12 EPX780-12 *Note (2)*		EPX740-15Z EPX740-15 EPX780-15Z EPX780-15		
Register SRAM Read—Synchronous								
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{SU}	Input or I/O setup time to clock	11.5		13		16		ns
t_{H}	Input or I/O hold time to clock	0		0		0		ns
t_{CO1}	Clock-to-output valid		6.5		7.5		9	ns
t_{CL}	Clock low time	4.5		5.5		7		ns
t_{CH}	Clock high time	4.5		5.5		7		ns
t_{CP}	Clock period	15		17		20		ns

External Timing Parameters		EPX740-10Z EPX740-10 EPX780-10Z EPX780-10		EPX740-12 EPX780-12 *Note (2)*		EPX740-15Z EPX740-15 EPX780-15Z EPX780-15		
Register SRAM Read—Delayed Synchronous								
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{SU}	Input or I/O setup time to clock	10		11		13		ns
t_{H}	Input or I/O hold time to clock	2		2		2		ns
t_{CO1}	Clock-to-output valid		8.5		9.5		12	ns
t_{CL}	Clock low time	4.5		5.5		7		ns
t_{CH}	Clock high time	4.5		5.5		7		ns
t_{CP}	Clock period	15		17.5		20		ns

External Timing Parameters			EPX740-10Z EPX740-10 EPX780-10Z EPX780-10		EPX740-12 EPX780-12 *Note (2)*		EPX740-15Z EPX740-15 EPX780-15Z EPX780-15		
SRAM Write									
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{WC}	Write cycle time		15		18		20		ns
t_{BW}	Block enable to end of write		10		12		13		ns
t_{AW}	Address valid to end of write		13		15		17		ns
t_{AS}	Address setup time		3		4		4		ns
t_{WP}	Write pulse width		10		12		13		ns
t_{WR}	Write recovery time		2		3		3		ns
t_{DW}	Data valid to end of write		10		12		13		ns
t_{DH}	Data hold time		2		3		3		ns
t_{OHZ}	Output disable to valid data in	C1 = 5 pF, *Notes (5), (6)*	10		15		13		ns

AC Operating Characteristics: EPX880 & EPX8160

External Timing Parameters			EPX880-10 EPX8160-10 *Note (2)*		EPX880-12 EPX8160-12 *Note (2)*		
Combinatorial Mode							
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD}	Input or I/O to output valid	C1 = 35 pF		10		12	ns
t_{PZX}	Input or I/O to output enable	C1 = 35 pF		12		14	ns
t_{PXZ}	Input or I/O to output disable	C1 = 5 pF		12		14	ns
t_{CLR}	Array output clear time			15		18	ns
t_{COMP}	Comparator input or I/O feedback to output valid			10		12	ns

External Timing Parameters			EPX880-10 EPX8160-10 *Note (2)*		EPX880-12 EPX8160-12 *Note (2)*		
Register Mode—Synchronous Clock							
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
f_{MAX}	Maximum frequency	*Note (3)*	100		83.3		MHz
t_{SU}	Input setup time		6.5		8		ns
t_{H}	Input hold time		0		0		ns
t_{CH}	Clock high time		4.5		5.5		ns
t_{CL}	Clock low time		4.5		5.5		ns
t_{CP}	Clock period		10		12		ns
t_{CO}	Clock-to-output delay	C1 = 35 pF		6		7.5	
t_{CNT}	Minimum clock period			12.5		15.5	
f_{CNT}	Internal maximum frequency	*Note (4)*	80		64.5		MHz

External Timing Parameters			EPX880-10 EPX8160-10 *Note (2)*		EPX880-12 EPX8160-12 *Note (2)*		
Register Mode—Delayed Synchronous Clock							
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
f_{MAX}	Maximum frequency	*Note (3)*	92.9		80		MHz
t_{SU}	Input setup time		5		6		ns
t_{H}	Input hold time		2		2		ns
t_{CH}	Clock high time		4.5		5.5		ns
t_{CL}	Clock low time		4.5		5.5		ns
t_{CP}	Clock period		10.5		12.5		ns
t_{CO}	Clock-to-output delay	C1 = 35 pF		8		9.5	ns
t_{CNT}	Minimum clock period			13		15.5	ns
f_{CNT}	Internal maximum frequency	*Note (4)*	76.9		64.5		MHz

External Timing Parameters			EPX880-10 EPX8160-10 *Note (2)*		EPX880-12 EPX8160-12 *Note (2)*		
Register Mode—Array Clock							
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
f_{AMAX}	Maximum frequency	*Note (3)*	80		66.7		MHz
t_{ASU}	Input setup time		2		2.5		ns
t_{AH}	Input hold time		5		6		ns
t_{ACH}	Clock high time		5		5.5		ns
t_{ACL}	Clock low time		5		5.5		ns
t_{ACP}	Clock period		12.5		15		ns
t_{ACO}	Clock-to-output delay	C1 = 35 pF		12		14.5	ns
t_{ACNT}	Minimum clock period			14		17	ns
f_{ACNT}	Internal maximum frequency	*Note (4)*	71.4		58.8		MHz

External Timing Parameters			EPX880-10 EPX8160-10 *Note (2)*		EPX880-12 EPX8160-12 *Note (2)*		
SRAM Read *Note (1)*							
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{RC}	Read cycle time		15		18		ns
t_{AA}	Address access time			15		18	ns
t_{ABE}	Block enable access time			15		18	ns
t_{OE}	Output enable to output valid	*Note (5)*		12		15	ns
t_{OH}	Output hold from address change		2		3		ns
t_{BLZ}	Block enable to output in low impedance	*Note (5)*	3		4		ns
t_{BHZ}	Block disable to output in high impedance	C1 = 5 pF, *Note (5)*		12		15	ns
t_{OLZ}	Output enable to output in low impedance	*Note (5)*	3		4		ns

External Timing Parameters			EPX880-10 EPX8160-10 *Note (2)*		EPX880-12 EPX8160-12 *Note (2)*		
Register SRAM Read—Synchronous *Note (1)*							
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{SU}	Input or I/O setup time to clock		11		13		ns
t_{H}	Input or I/O hold time from clock		0		0		ns
t_{CO1}	Clock-to-output valid			6		7.5	ns
t_{CL}	Clock low time		4.5		5.5		ns
t_{CH}	Clock high time		4.5		5.5		ns
t_{CP}	Clock period		15		17		ns

External Timing Parameters			EPX880-10 EPX8160-10 *Note (2)*		EPX880-12 EPX8160-12 *Note (2)*		
Register SRAM Read—Delayed Synchronous *Note (1)*							
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{SU}	Input or I/O setup time to clock		10		11		ns
t_{H}	Input or I/O hold time from clock		2		2		ns
t_{CO1}	Clock-to-output valid			8		9.5	ns
t_{CL}	Clock low time		4.5		5.5		ns
t_{CH}	Clock high time		4.5		5.5		ns
t_{CP}	Clock period		15.5		17.5		ns

External Timing Parameters			EPX880-10 EPX8160-10 *Note (2)*		EPX880-12 EPX8160-12 *Note (2)*		
SRAM Write *Note (1)*							
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{WC}	Write cycle time		15		18		ns
t_{BW}	Block enable to end of write		10		12		ns
t_{AW}	Address valid to end of write		13		15		ns
t_{AS}	Address set-up time		3		4		ns
t_{WP}	Write pulse width		10		12		ns
t_{WR}	Write recovery time		2		3		ns
t_{DW}	Data valid to end of write		10		12		ns
t_{DH}	Data hold time		2		3		ns
t_{OHZ}	Output disable to valid data in	C1 = 5 pF *Notes (5), (6)*	12		15		ns

Notes to tables:

(1) Operating conditions: T_A = 0° C to 70° C, V_{CC} = 5.0 V ± 5% for commercial use.
T_A = –40° C to 85° C, V_{CC} = 5.0 V ± 10% for industrial use.

(2) The parameters for the EPX740-12, EPX780-12, EPX880-10, EPX880-12 are preliminary.

(3) The f_{MAX} values represent the highest frequency for pipelined data.

(4) Measured with a 10-bit loadable, enabled, up/down binary counter programmed into each LAB.

(5) These signals are measured at ± 0.5 V from steady-state voltage as driven by specified output load. Z → H and Z → L are measured at 1.5 V on output.

(6) These specifications do not apply when separate data-in and data-out buses are used.

Calculating the Supply Current

Supply current (I_{CC}) versus frequency (f_{MAX}) for FLASHlogic devices is calculated using the following equation:

$$I_{CC} = I_{CCOUTPUT} + I_{CCACTIVE}$$

The $I_{CCOUTPUT}$ value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines provided in the *Operating Requirements for Altera Devices Data Sheet* in this data book. The $I_{CCACTIVE}$ value depends on the switching frequency and the application logic. The following equation shows the formula for calculating $I_{CCACTIVE}$:

$$I_{CCACTIVE} = (A \times MC) + (C \times MC) \times f_{MAX}$$

The parameters for this equation are:

MC = Number of macrocells used in the design
f_{MAX} = Highest Clock frequency to the device

Table 7 lists the values for the constants A and C.

Table 7. FLASHlogic I_{CC} Equation Constants

Device	Constant A	Constant C
EPX740	0.500	0.0250
EPX740Z	0.025	0.0250
EPX780	0.250	0.0188
EPX780Z	0.0125	0.0188
EPX880 *(1)*	0.0125	0.0188
EPX8160	0.0062	0.0156

Note:
(1) This data is preliminary.

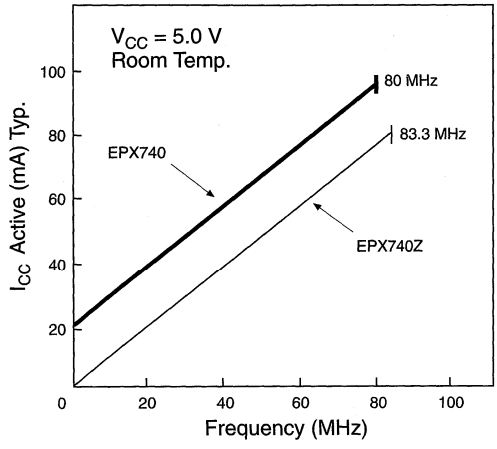
The formula for calculating $I_{CCACTIVE}$ provides an estimate based on typical conditions using a typical pattern of a 20-bit, loadable, enabled, up/down binary counter with no output load in each pair of LABs. Actual I_{CC} should be verified during operation since this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

Figure 12 shows the typical supply current versus frequency curves for FLASHlogic devices.

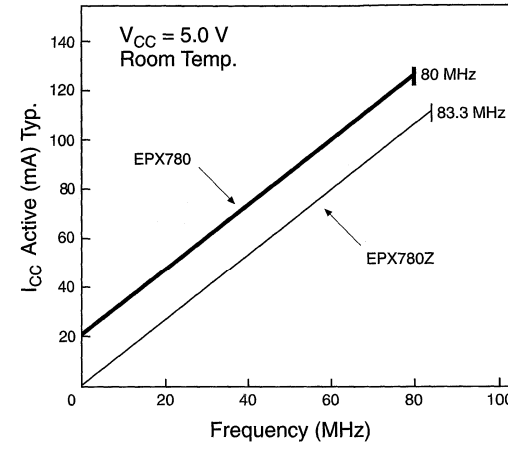
Figure 12. I_{CC} versus Frequency for FLASHlogic Devices

The output drive characteristics for EPX880 devices are preliminary.

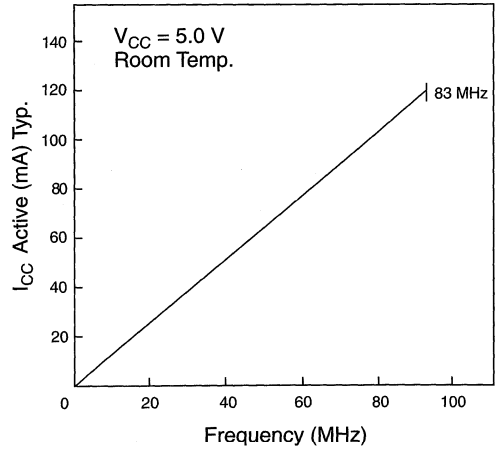
EPX740 & EPX740Z



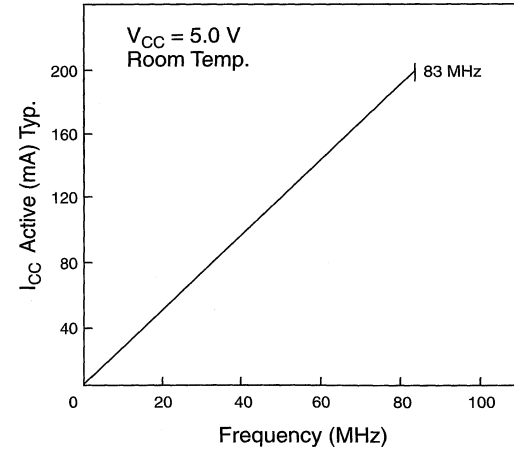
EPX780 & EPX780Z



EPX880



EPX8160



Power-Up Cycle

Because V_{CC} rise can vary significantly from one application to another, the power-up cycle time varies. For a monotonic V_{CC} rise (1 ms/V minimum), the power-up cycle is complete when V_{CC} reaches its minimum value. The power-up cycle is complete 100 µs after V_{CC} reaches the minimum value.

Internal power-up reset circuits ensure that all flipflops are reset to a logic low after the device has powered up. Also, the JTAG TAP controller is put into the Test-Logic-Reset state. During power-up, EPX8160 I/O pins are held high by an active-weak pull-up resistor; EPX740, EPX780, and EPX880 I/O pins are tri-stated. Upon completion of the power-up cycle, the outputs on an unprogrammed device are placed in a high-impedance state.

Power-On Reset (POR) Feature

FLASHlogic device configuration data can be reloaded from EPROM or FLASH memory at any time by issuing a JTAG RESET instruction or by holding V_{PP} at a logic low (0.8 V maximum) for a minimum of 300 ns. By holding V_{PP} low during power-up, the power-up cycle can be delayed. The power-up cycle is completed within a delay of t_{RESET} after V_{PP} reaches 2.0 V (see Table 8). During normal operation, V_{PP} must be held at a logic high (2.4 V minimum) or tied to the V_{PP} supply (12.0 V).

During reconfiguration or reprogramming, the JTAG RESET instruction is automatically issued by PENGN or JED2JTAG (PLDshell Plus software utilities). It is not necessary to pull V_{PP} low after a reconfiguration or reprogram cycle.

Table 8. Reset Characteristics

Symbol	Parameter	Value	Conditions
t_{RESET}	JTAG reset time	150 µs maximum	Software Control $V_{PP} \geq 2.0$ V

Go to *Application Note 45 (Configuring FLASHlogic Devices)*, for more information on configuring or programming FLASHlogic devices using the JTAG interface.

Pin Descriptions

Table 9 lists the dedicated pin names and descriptions.

Table 9. Dedicated Pins

Pin Name	Description
VCC, *Note (1)*	Supply voltage. Must be connected to 5.0 V.
GND	Ground connection.
VPP, *Note (1)*	Programming voltage. When programming EPX740 and EPX780 devices, 12.75 V must be supplied to this pin. When programming EPX880 and EPX8160 devices, 12.0 V must be supplied to this pin. When the EPX740, EPX780, and EPX880 devices are not in programming mode, this pin can be connected to VCC or VPP, or left floating. When the EPX8160 devices are not in programming mode, this pin can be connected to VCC or VPP. The EPX8160 device requires that VPP be held low (0.8 V maximum) for a minimum of 300 ns to reset the device.
IN*n*	Input-only pins. These pins are not available in all packages. Unused inputs should be connected to VCC or GND.
TDI	Test data input. This pin is the boundary-scan serial data input to FLASHlogic devices. JTAG instructions and data are shifted into FLASHlogic devices on the TDI input pin on the rising edge of TCK. TDI can be left floating if unused.
TDO	Test data output. This is the boundary-scan serial data output from FLASHlogic devices. JTAG instructions and data are shifted out of FLASHlogic devices on the TDO output pin on the falling edge of TCK.
TCK	Test Clock input. This input provides the boundary-scan Clock for FLASHlogic devices. TCK Clocks shift information and data into and out of the FLASHlogic devices during boundary-scan or programming modes. The maximum operating frequency of the boundary-scan test Clock is 8 MHz. TCK can be left floating if unused.
TMS	Test control input. This input provides the boundary-scan test mode select for FLASHlogic devices. TMS can be left floating if unused.

Note:

(1) Proper power decoupling is required on all power pins. A 0.1-µF decoupling capacitor is recommended between each power pin and ground.

Table 10 lists the user-defined pin names and descriptions.

Table 10. User-Defined Pins

Pin Name	Description
VCCO*n*, *Note (1)*	Supply voltage for the outputs of the LABs. Connecting these pins to 5.0 V causes the LAB to output 5.0-V signals. Connecting these pins to 3.3 V causes the LAB to output 3.3-V signals. These pins must always be connected to the desired output drive voltage.
CLK*n*	Global Clock signals.
I/O*n*	Pins configurable as inputs or outputs. Unused I/O pins should be connected as shown in the Report File. The reserved pins must be left unconnected.

Note:
(1) Proper power decoupling is required on all power pins. A 0.1-µF decoupling capacitor is recommended between each power pin and ground.

Device Pin-Outs

Tables 11 through 16 show the pin-outs for FLASHlogic device packages.

Table 11. EPX740 Dedicated Pin-Outs

Dedicated Pin	44-Pin PLCC	68-Pin PLCC
CLK1	13	19
CLK2	35	53
TDI	22	33
TDO	21	32
TMS	44	67
TCK	43	66
VPP	14	20
VCCO0	12	18
VCCO1	12	17
VCCO2	34	51
VCCO3	34	52
VCC	23	35
GND	1, 15, 36, 37	1, 21, 34, 54, 55, 68
Dedicated Inputs	–	16, 15, 4, 3, 2, 50, 49, 38, 37, 36

Table 12. EPX740 I/O Pin-Outs *Note (1)*

LAB	MC	44-Pin J-Lead	68-Pin J-Lead	LAB	MC	44-Pin J-Lead	68-Pin J-Lead
0	0	16	22	1	10	11	14
0	1	–	23	1	11	10	13
0	2	–	24	1	12	9	12
0	3	17	25	1	13	8	11
0	4	–	26	1	14	7	10
0	5	18	27	1	15	6	9
0	6	–	28	1	16	5	8
0	7	19	29	1	17	4	7
0	8	–	30	1	18	3	6
0	9	20	31	1	19	2	5
2	20	33	48	3	30	38	56
2	21	32	47	3	31	–	57
2	22	31	46	3	32	–	58
2	23	30	45	3	33	39	59
2	24	29	44	3	34	–	60
2	25	28	43	3	35	40	61
2	26	27	42	3	36	–	62
2	27	26	41	3	37	41	63
2	28	25	40	3	38	–	64
2	29	24	39	3	39	42	65

Note:
(1) A dash (–) indicates that the macrocell is buried.

Table 13. EPX780 & EPX880 Dedicated Pin-Outs *Note (1), (2)*		
Dedicated Pin	**84-Pin PLCC**	**132-Pin PQFP**
CLK1	3	118
CLK2	45	52
TDI	11	132
TDO	10	131
TMS	52	65
TCK	53	66
VPP	4	119
VCCO0	25	117
VCCO1	2	116
VCCO2	24	19
VCCO3	67	86
VCCO4	25	20
VCCO5	66	85
VCCO6	44	50
VCCO7	67	51
VCC	26, 68	21, 87
GND	17, 23, 29, 38, 46, 59, 65, 71, 80	11, 17, 18, 27, 44, 53, 59, 77, 83, 84, 93, 110, 125
Dedicated Inputs	–	1, 2, 3, 4, 5, 33, 34, 35, 36, 37, 38, 67, 68, 69, 70, 71, 99, 100, 101, 102, 103, 104,

Notes:
(1) The pin-outs for EPX880 devices are preliminary.
(2) Contact Altera Marketing for the EPX880 160-pin package pin-outs.

Table 14. EPX780 & EPX880 I/O Pin-Outs (Part 1 of 2) *Notes (1), (2), (3)*

LAB	MC	84-Pin J-Lead	132-Pin QFP	LAB	MC	84-Pin J-Lead	132-Pin QFP
0	0	5	120	1	10	1	115
0	1	–	121	1	11	84	114
0	2	–	122	1	12	83	113
0	3	6	123	1	13	82	112
0	4	–	124	1	14	81	111
0	5	7	126	1	15	79	109
0	6	–	127	1	16	78	108
0	7	8	128	1	17	77	107
0	8	–	129	1	18	76	106
0	9	9	130	1	19	75	105
2	20	22	16	3	30	69	88
2	21	21	15	3	31	–	89
2	22	20	14	3	32	–	90
2	23	19	13	3	33	70	91
2	24	18	12	3	34	–	92
2	25	16	10	3	35	72	94
2	26	15	9	3	36	–	95
2	27	14	8	3	37	73	96
2	28	13	7	3	38	–	97
2	29	12	6	3	39	74	98

Table 14. EPX780 & EPX880 I/O Pin-Outs (Part 2 of 2) *Notes (1), (2), (3)*

LAB	MC	84-Pin J-Lead	132-Pin QFP	LAB	MC	84-Pin J-Lead	132-Pin QFP
4	40	27	22	5	50	64	82
4	41	–	23	5	51	63	81
4	42	–	24	5	52	62	80
4	43	28	25	5	53	61	79
4	44	–	26	5	54	60	78
4	45	30	28	5	55	58	76
4	46	–	29	5	56	57	75
4	47	31	30	5	57	56	74
4	48	–	31	5	58	55	73
4	49	32	32	5	59	54	72
6	60	43	49	7	70	47	54
6	61	42	48	7	71	–	55
6	62	41	47	7	72	–	56
6	63	40	46	7	73	48	57
6	64	39	45	7	74	–	58
6	65	37	43	7	75	49	60
6	66	36	42	7	76	–	61
6	67	35	41	7	77	50	62
6	68	34	40	7	78	–	63
6	69	33	39	7	79	51	64

Notes:
(1) The pin-outs for EPX880 devices are preliminary.
(2) A dash (–) indicates that the macrocell is buried.
(3) Contact Altera Marketing for the EPX880 160-pin package pin-outs.

Table 15. EPX8160 Dedicated Pin-Outs

Dedicated Pin	208-Pin PQFP
CLK1	184
CLK2	181
CLK3	77
CLK4	80
TDI	1
TDO	208
TMS	105
TCK	104
VPP0	182
VPP1	79
VCCO0/VCCO2	204
VCCO1/VCCO3	161
VCCO4/VCCO6	13
VCCO5/VCCO7	144
VCCO8/VCCO10	57
VCCO9/VCCO11	100
VCCO12/VCCO14	40
VCCO13/VCCO15	117
VCC	14, 39, 118, 143
GND	7, 15, 21, 32, 38, 46, 67, 78, 90, 111, 119, 125, 136, 142, 150, 171,183, 194
Dedicated Inputs	52, 53, 54, 55, 56, 59, 61, 63, 65, 69, 71, 73, 75, 82, 84, 86, 88, 92, 94, 96, 98, 101, 102, 103, 156, 157, 158, 159, 160, 163, 165, 167, 169, 173, 175, 177, 179, 186, 188, 190, 192, 196, 198, 200, 202, 205, 206, 207

Table 16. EPX8160 I/O Pin-Outs (Part 1 of 3) *Note (1)*

LAB	MC	208-Pin PQFP	LAB	MC	208-Pin PQFP
0	0	185	1	10	180
0	1	187	1	11	178
0	2	189	1	12	176
0	3	191	1	13	174
0	4	193	1	14	172
0	5	195	1	15	170
0	6	197	1	16	168
0	7	199	1	17	166
0	8	201	1	18	164
0	9	203	1	19	162
2	20	6	3	30	151
2	21	–	3	31	–
2	22	–	3	32	–
2	23	5	3	33	152
2	24	–	3	34	–
2	25	4	3	35	153
2	26	–	3	36	–
2	27	3	3	37	154
2	28	–	3	38	–
2	29	2	3	39	155
4	40	8	5	50	149
4	41	9	5	51	148
4	42	10	5	52	147
4	43	11	5	53	146
4	44	12	5	54	145
4	45	16	5	55	141
4	46	17	5	56	140
4	47	18	5	57	139
4	48	19	5	58	138
4	49	20	5	59	137

Table 16. EPX8160 I/O Pin-Outs (Part 2 of 3) *Note (1)*

LAB	MC	208-Pin PQFP	LAB	MC	208-Pin PQFP
6	60	26	7	70	131
6	61	–	7	71	–
6	62	–	7	72	–
6	63	25	7	73	132
6	64	–	7	74	–
6	65	24	7	75	133
6	66	–	7	76	–
6	67	23	7	77	134
6	68	–	7	78	–
6	69	22	7	79	135
8	80	76	9	90	81
8	81	74	9	91	83
8	82	72	9	92	85
8	83	70	9	93	87
8	84	68	9	94	89
8	85	66	9	95	91
8	86	64	9	96	93
8	87	62	9	97	95
8	88	60	9	98	97
8	89	58	9	99	99
10	100	47	11	110	110
10	101	–	11	111	–
10	102	–	11	112	–
10	103	48	11	113	109
10	104	–	11	114	–
10	105	49	11	115	108
10	106	–	11	116	–
10	107	50	11	117	107
10	108	–	11	118	–
10	109	51	11	119	106

Table 16. EPX8160 I/O Pin-Outs (Part 3 of 3) *Note (1)*

LAB	MC	208-Pin PQFP	LAB	MC	208-Pin PQFP
12	120	45	13	130	112
12	121	44	13	131	113
12	122	43	13	132	114
12	123	42	13	133	115
12	124	41	13	134	116
12	125	37	13	135	120
12	126	36	13	136	121
12	127	35	13	137	122
12	128	34	13	138	123
12	129	33	13	139	124
14	140	27	15	150	130
14	141	–	15	151	–
14	142	–	15	152	–
14	143	28	15	153	129
14	144	–	15	154	–
14	145	29	15	155	128
14	146	–	15	156	–
14	147	30	15	157	127
14	148	–	15	158	–
14	149	31	15	159	126

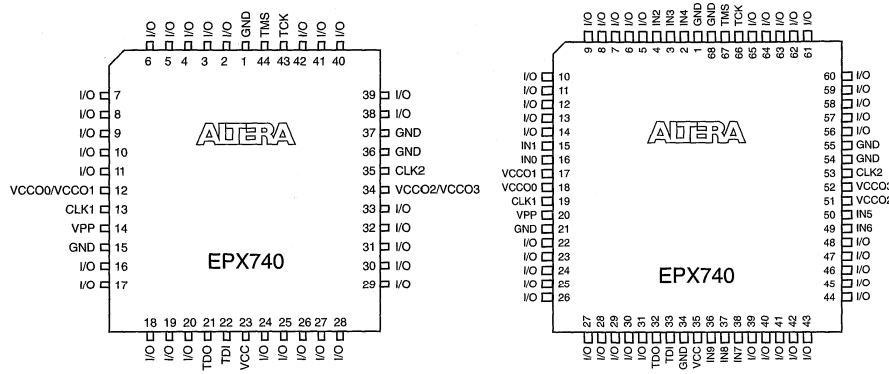
Note:
(1) A dash (–) indicates that the macrocell is buried.

Package Diagrams

Figures 13 through 16 show the package pin-out diagrams for FLASHlogic devices.

Figure 13. EPX740 Package Pin-Out Diagrams

Package outlines are not drawn to scale. See Tables 11 and 12 for pin-out information.

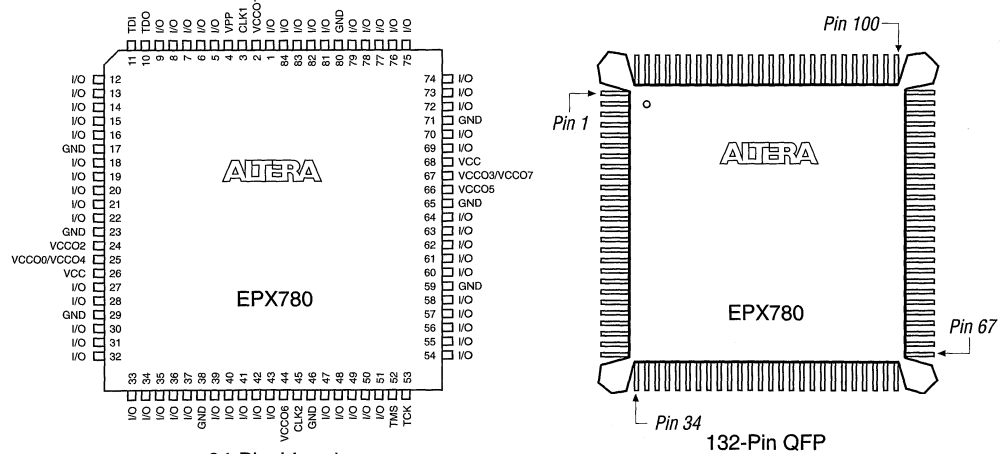


44-Pin J-Lead

68-Pin J-Lead

Figure 14. EPX780 Package Pin-Out Diagrams

Package outlines are not drawn to scale. See Tables 13 and 14 for pin-out information.

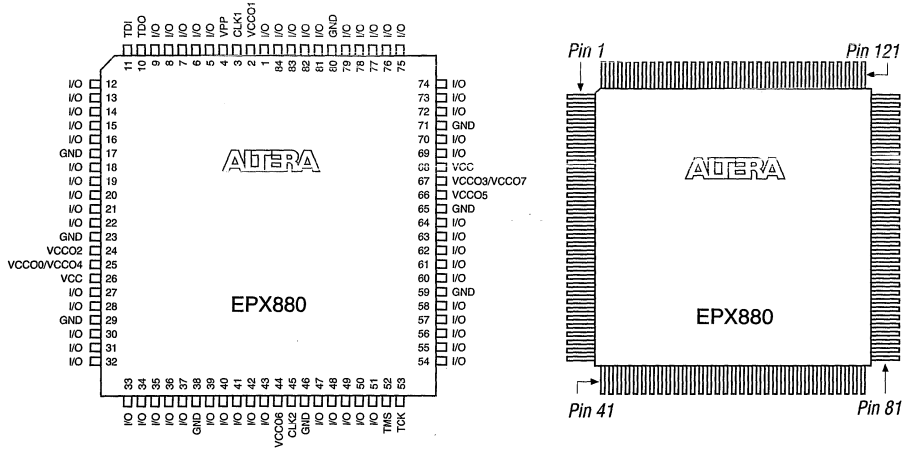


84-Pin J-Lead

132-Pin QFP

Figure 15. EPX880 Package Pin-Out Diagram

Package outline not drawn to scale. See Tables 13 and 14 for pin-out information.

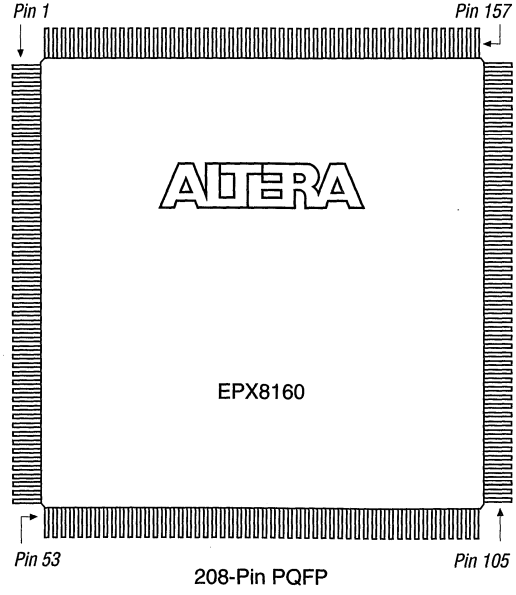


84-Pin J-Lead

160-Pin QFP

Figure 16. EPX8160 Package Pin-Out Diagram

Package outline not drawn to scale. See Tables 15 and 16 for pin-out information.



208-Pin PQFP

March 1995

MAX 5000 Programmable Logic Device Family

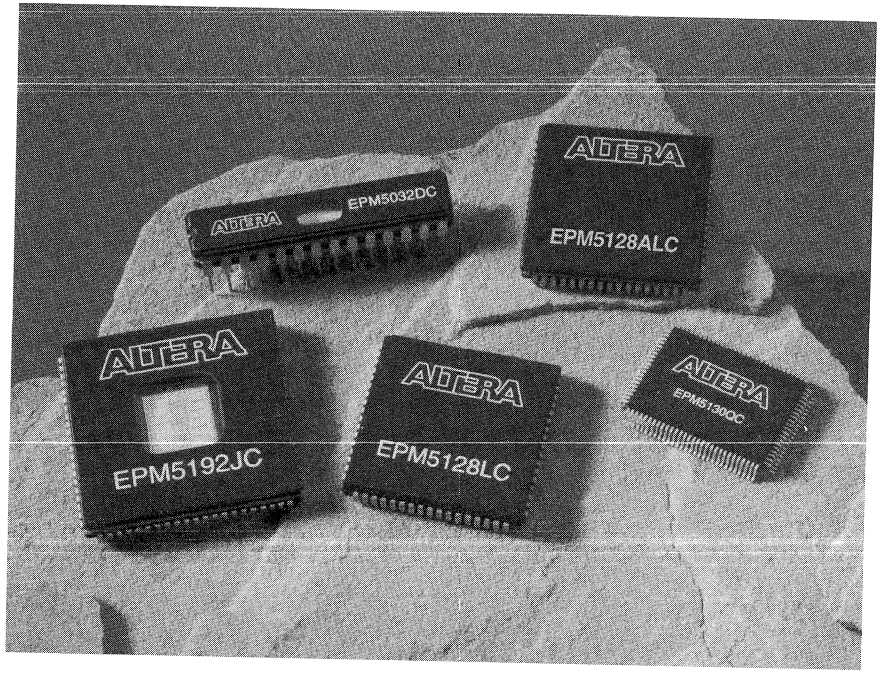
EPM5032 EPLD

EPM5064 EPLD

EPM5128 EPLD

EPM5130 EPLD

EPM5192 EPLD


ALTERA
EPM5032DC
ALTERA
EPM5128ALC
ALTERA
EPM5192JC
ALTERA
EPM5128LC
ALTERA
EPM5130QC

MAX 5000

Programmable Logic Device Family

March 1995, ver. 2 — Data Sheet

Features...

- Advanced Multiple Array MatriX (MAX) 5000 architecture combining speed and ease-of-use of PAL devices with density of programmable gate arrays
- Complete family of high-performance, erasable 0.65- and 0.8-micron CMOS EPROM EPLDs for designs ranging from fast 28-pin address decoders to 100-pin LSI custom peripherals (see Table 1)
- Fast, 10-ns combinatorial delays and 125-MHz counter frequencies
- Configurable expander product-term distribution allowing more than 32 product terms in a single macrocell
- 28 to 100 pins available in DIP, J-lead, PGA, SOIC, and QFP packages
- Programmable registers providing D, T, JK, and SR flipflop functionality with individual Clear, Preset, and Clock controls
- Programmable Security Bit for total protection of proprietary designs
- Software design support featuring Altera's MAX+PLUS II development system on 486- or Pentium-based PCs, and Sun SPARCstation, HP 9000 Series 700, and IBM RISC System/6000 workstations

Table 1. MAX 5000 Device Features

Feature	EPM5032	EPM5064	EPM5128	EPM5130	EPM5192
Available gates	1,200	2,500	5,000	5,000	7,500
Usable gates	600	1,250	2,500	2,500	3,750
Macrocells	32	64	128	128	192
LABs	1	4	8	8	12
Expanders	64	128	256	256	384
Routing	global	PIA	PIA	PIA	PIA
Maximum user I/O pins	24	36	60	68, 84	72
t_{PD} (ns)	10	15	15	15	15
t_{ASU} (ns)	3	5	5	5	5
t_{CO} (ns)	6	8	8	8	8
f_{CNT} (MHz)	125	83.3	83.3	83.3	83.3

...and More Features

- Programming support with Altera's Master Programming Unit (MPU) or programming hardware from other manufacturers
- Additional design entry and simulation support provided by EDIF, Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Data I/O, Exemplar, Intergraph, Mentor Graphics, OrCAD, Synopsys, and Viewlogic

General Description

The MAX 5000 family combines innovative architecture and advanced process technologies to offer optimum performance, flexibility, and the highest logic-to-pin ratio of any general-purpose programmable logic device family. The MAX 5000 family provides 600 to 3,750 usable gates, pin-to-pin delays as fast as 10 ns, and counter frequencies of up to 125 MHz. See Table 2.

The MAX 5000 architecture supports 100% TTL emulation and high-density integration of multiple SSI, MSI, and LSI logic functions. For example, an EPM5192 can replace over 100 7400-series devices; it can integrate complete subsystems into a single package, saving board area and reducing power consumption. MAX 5000 EPLDs are available in a wide range of packages; including windowed ceramic and plastic dual in-line (CerDIP and PDIP), windowed ceramic and plastic J-lead chip carrier (JLCC and PLCC), windowed ceramic pin-grid array (PGA), plastic small-outline integrated circuit (SOIC), and windowed ceramic and plastic quad flat pack (CQFP and PQFP) packages. See Table 3.

Table 2. MAX 5000 Timing Parameter Availability

Device	Speed (t_{PDI})							
	10 ns	12 ns	15 ns	17 ns	20 ns	25 ns	30 ns	35 ns
EPM5032	✓(1)	✓(1)	✓	✓	✓	✓	–	–
EPM5064	–	–	✓(1)	–	✓(1)	✓	✓	✓
EPM5128	–	–	✓	–	✓	✓	✓	✓
EPM5130	–	–	✓(1)	–	✓(1)	✓	✓	✓
EPM5192	–	–	✓	–	✓	✓	✓	✓

Note:
(1) Timing parameters for this speed grade are preliminary.

Table 3. MAX 5000 Pin Count, Package Options & Maximum User I/O Note (1)

Device	Pin Count				
	28	44	68	84	100
EPM5032	CerDIP PDIP JLCC PLCC SOIC	–	–	–	–
EPM5064	–	JLCC PLCC	–	–	–
EPM5128	–	–	JLCC PLCC PGA	–	–
EPM5130	–	–	–	JLCC PLCC	PGA CQFP PQFP
EPM5192	–	–	–	JLCC PLCC PGA	PQFP

Note:
(1) Contact Altera for information on available device packages.

MAX 5000 EPLDs have between 32 and 192 macrocells that are combined into groups called Logic Array Blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register that provides D, T, JK, or SR operation with independent programmable Clock, Clear, and Preset functions. To build complex logic functions, each macrocell can be supplemented with shareable expander product terms ("shared expanders") to provide more than 32 product terms per macrocell.

The MAX 5000 family is supported by Altera's MAX+PLUS II development system, a single integrated package that offers schematic, text, and waveform design entry; compilation and logic synthesis; simulation; and device programming. MAX+PLUS II provides EDIF, VHDL, Verilog HDL, and other netlist interfaces for additional design entry and simulation support from other industry-standard PC- and workstation-based EDA tools. MAX+PLUS II runs on 486- and Pentium-based PCs, as well as Sun SPARCstation, HP 9000 Series 700, and IBM RISC System/6000 workstations.

Developed on a 0.8-micron CMOS EPROM process, MAX 5000 EPLDs offer pin-to-pin logic delays as fast as 15 ns and counter frequencies as high as 76.9 MHz.

MAX 5000A EPLDs are developed with a state-of-the-art 0.65-micron CMOS EPROM process, offering pin-to-pin delays as fast as 10 ns and counter frequencies as high as 125 MHz. MAX 5000 and MAX 5000A EPLDs are fully pin-, function-, and programming-file-compatible.

The MAX 5000 family is supported by Altera's MAX+PLUS II development system, a single, integrated package that offers schematic, text—including the Altera Hardware Description Language (AHDL)—and waveform design entry; compilation and logic synthesis; simulation and timing analysis; and device programming. MAX+PLUS II provides EDIF 2 0 0 and 3 0 0, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and workstation-based EDA tools. MAX+PLUS II runs on 486- and Pentium-based PCs, and Sun SPARCstation, HP 9000 Series 700, IBM RISC System / 6000 workstations.

For more information, go to the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* in this data book.

Functional Description

This section provides a functional description of MAX 5000 EPLDs, which have the following architectural features:

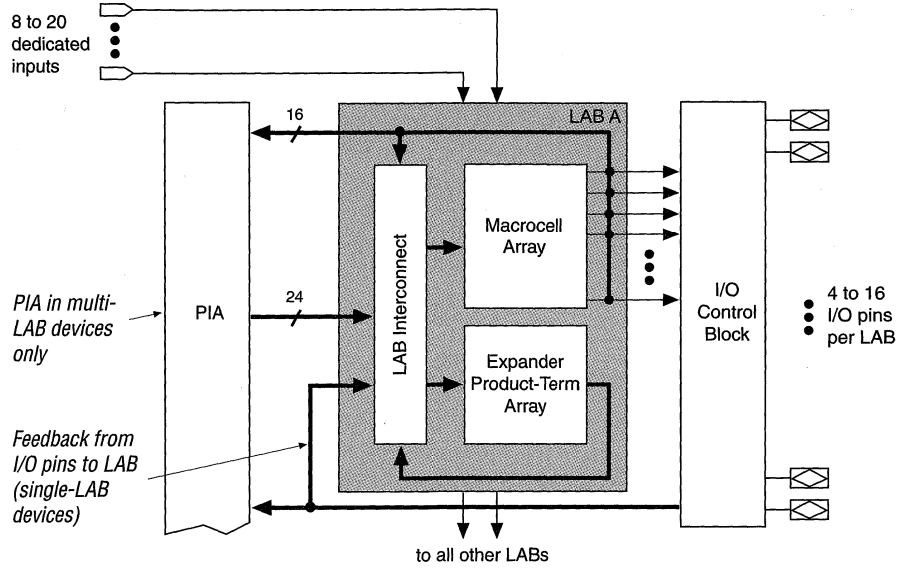
- Logic Array Blocks
- Macrocells
- Clocking options
- Expander product terms
- Programmable Interconnect Array
- I/O control blocks

The MAX 5000 architecture is based on the concept of linking high-performance, flexible logic array modules called Logic Array Blocks (LABs). Multiple LABs are linked via the Programmable Interconnect Array (PIA), a global bus that is fed by all I/O pins and macrocells. In addition to these basic elements, the MAX 5000 architecture includes 8 to 20 dedicated inputs, each of which can be used as a high-speed, general-purpose input. Alternatively, one of the dedicated inputs can be used as a high-speed global Clock for registers.

Logic Array Blocks

MAX 5000 EPLDs contain 1 to 12 LABs. The EPM5032 has a single LAB, while the EPM5064, EPM5128, EPM5130, and EPM5192 contain multiple LABs. Each LAB consists of a macrocell array and an expander product-term array. See Figure 1. The number of macrocells and expanders in the arrays varies with each device.

Figure 1. MAX 5000 Architecture

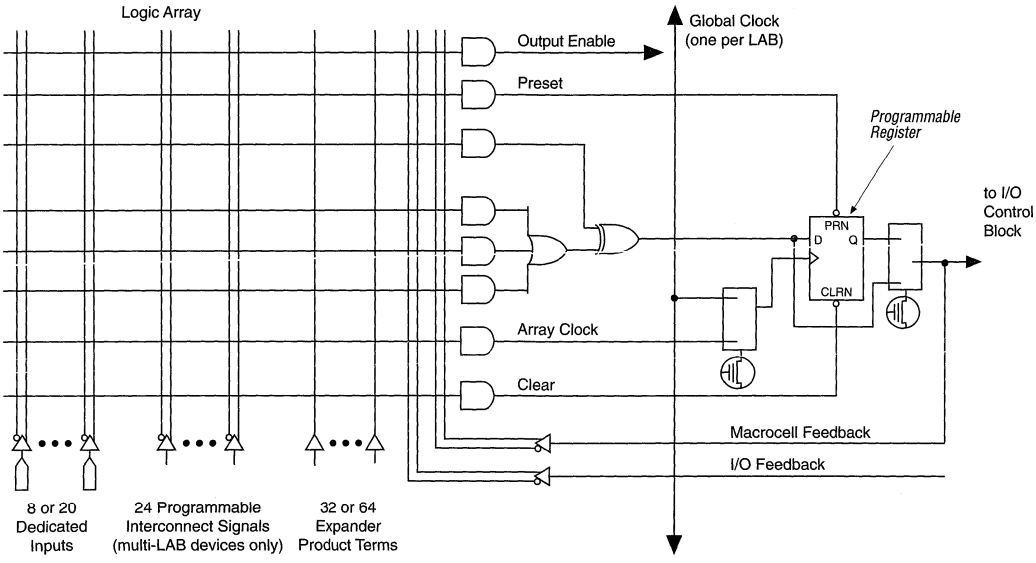


Macrocells are the primary resource for logic implementation. Additional logic capability is available from expanders, which can be used to supplement the capabilities of any macrocell. The expander product-term array consists of a group of unallocated, inverted product terms that can be used and shared by all macrocells in the LAB to create combinatorial and registered logic. These flexible macrocells and shareable expanders facilitate variable product-term designs without the inflexibility of fixed product-term architectures. All macrocell outputs are globally routed within an LAB via the LAB interconnect. The outputs of the macrocells also feed the I/O control block, which consists of groups of programmable tri-state buffers and I/O pins. In the EPM5064, EPM5128, EPM5130, and EPM5192, multiple LABs are connected by a Programmable Interconnect Array (PIA). All macrocells feed the PIA to provide efficient routing for high-fan-in designs.

Macrocells

The MAX 5000 macrocell consists of a programmable logic array and an independently configurable register (see Figure 2). The register can be programmed to emulate D, T, JK, or SR operation, as a flow-through latch, or bypassed for combinatorial operation. Combinatorial logic is implemented in the programmable logic array, in which three product terms that are ORed together feed one input to an XOR gate. The second input to the XOR gate is used for complex XOR arithmetic logic functions and for De Morgan's inversion.

Figure 2. MAX 5000 Macrocell



The output of the XOR gate feeds the programmable register or bypasses it for combinatorial operation.

Additional product terms—called secondary product terms—are used to control the Output Enable, Preset, Clear, and Clock signals. Preset and Clear product terms drive the active-low asynchronous Preset and asynchronous Clear inputs to the configurable flipflop. The Clock product term allows each register to have an independent Clock and supports positive- and negative-edge-triggered operation. Macrocells that drive an output pin can use the Output Enable product term to control the active-high tri-state buffer in the I/O control block. These secondary product terms allow exact emulation of 74-series macrofunctions.

The MAX 5000 macrocell configurability makes it possible to efficiently integrate complete subsystems into a single device.

Clocking Options

Each LAB supports either global or array clocking. Global clocking is provided by a dedicated Clock signal (CLK) that offers fast Clock-to-output delay times. Since each LAB has one global Clock, all flipflop Clocks within the LAB can be positive-edge-triggered from the CLK pin. If the CLK pin is not used as a global Clock, it can be used as a high-speed dedicated input.

In the array clocking mode, each flipflop is clocked by a product term. Any input pin or internal logic can be used as a Clock source. Array clocking allows each flipflop to be configured for positive- or negative-edge-triggered operation, giving the macrocell increased flexibility. Systems that require multiple Clocks are easily integrated into MAX 5000 EPLDs.

Each flipflop in an LAB can be clocked by a different array-generated Clock; however, global and array clocking modes cannot be mixed in the same LAB.

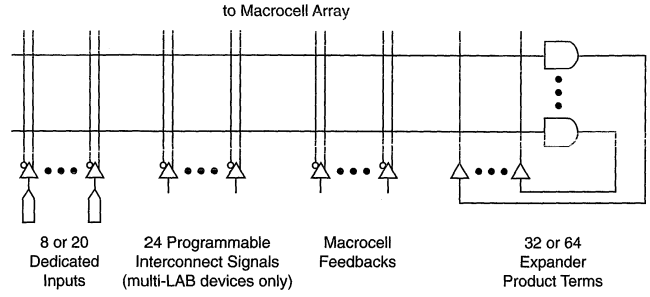
Expander Product Terms

While most logic functions can be implemented with the product terms available in each macrocell, some logic functions are more complex and require additional product terms. Although additional macrocells can be used to supply the needed logic resources, the MAX 5000 architecture may also use shared expander product terms that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

Each LAB has 32 shared expanders (except for EPM5032, which has 64). The expanders can be viewed as a pool of uncommitted product terms. The expander product-term array (see Figure 3) contains unallocated, inverted product terms that feed the macrocell array. Expanders can be used and shared by all product terms in the LAB. Wherever extra logic is needed (including register control functions), expanders can be used to implement the logic. These expanders provide the flexibility to implement register- and product-term-intensive designs in MAX 5000 EPLDs.

Figure 3. Expander Product Terms

Expander product terms are unallocated logic that can be used and shared by all macrocells in an LAB. Sharing allows efficient integration of complex combinatorial functions.



Expanders are fed by all signals in the LAB. One expander can feed all macrocells in the LAB or multiple product terms in the same macrocell. Since expanders also feed the secondary product terms of each macrocell, complex logic functions can be implemented without using additional macrocells. Expanders can also be cross-coupled to build additional flipflops, latches, or input registers. A small delay (t_{SEXP}) is incurred when shared expanders are used.

Programmable Interconnect Array

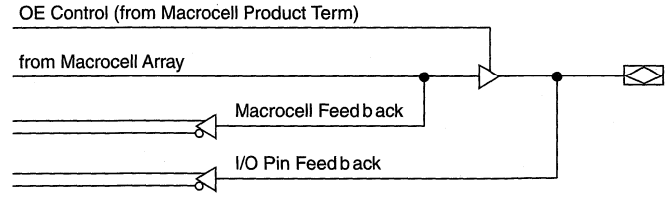
The higher-density MAX 5000 devices—EPM5064, EPM5128, EPM5130, and EPM5192—use a Programmable Interconnect Array (PIA) to route signals between the various LABs. The PIA, which is fed by all macrocell and I/O pin feedbacks, routes only the signals required for implementing logic in an LAB. While the routing delays of channel-based routing schemes in masked or field-programmable gate arrays (FPGAs) are cumulative, variable, and path-dependent, the MAX 5000 PIA has a fixed delay. The PIA thus eliminates skew between signals and makes timing performance easy to predict.

I/O Control Blocks

Each LAB has an I/O control block that allows each I/O pin to be individually configured for input, output, or bidirectional operation. See Figure 4. The I/O control block is fed by the macrocell array. A dedicated macrocell product term controls a tri-state buffer, which drives the I/O pad.

Figure 4. I/O Control Block

The decoupled I/O control block features dual feedback to maximize flexibility of device pins.



The MAX 5000 architecture provides dual I/O feedback in which macrocell and I/O pin feedbacks are independent. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic. Using an I/O pin as an input in single-LAB devices reduces the number of available expanders by two. In multi-LAB devices, I/O pins feed the PIA directly.

Design Security

All MAX 5000 EPLDs contain a programmable Security Bit that controls access to the data programmed into the device. When this bit is programmed, a proprietary design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security, since programmed data within EPROM cells is invisible. The Security Bit that controls this function, as well as all other program data, is reset when an EPLD is erased.

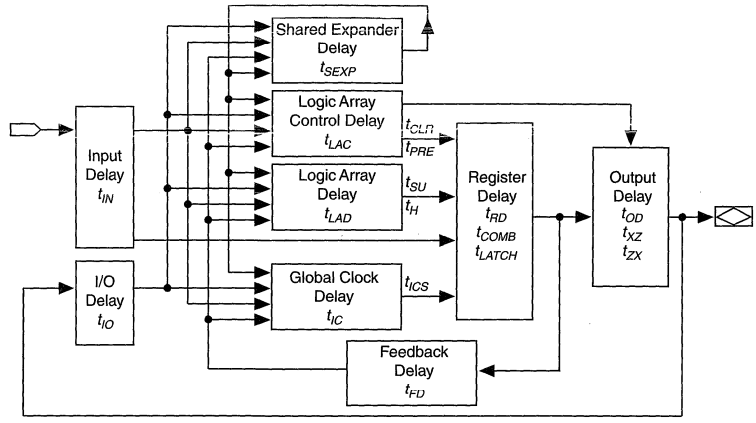
Timing Model

MAX 5000 EPLD timing can be analyzed with MAX+PLUS II software, with a variety of other industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 5. MAX 5000 EPLDs have fixed internal delays that allow the user to determine the worst-case timing for any design. MAX+PLUS II software provides timing simulation, point-to-point delay prediction, and detailed timing analysis.

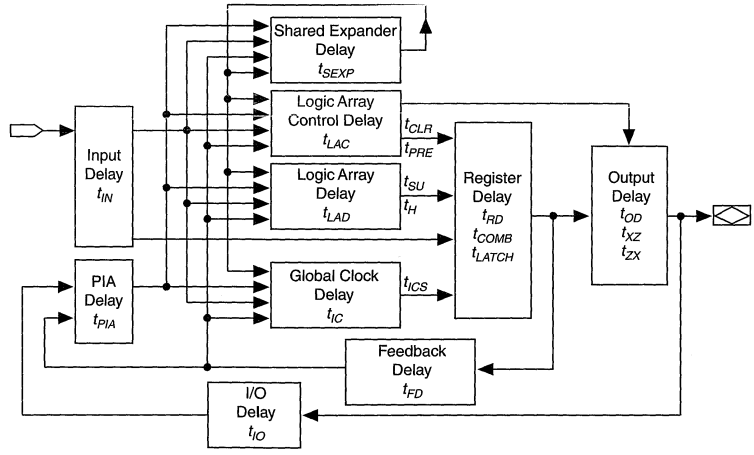
Figure 5. Timing Model

Design performance can be predicted with these timing models and the device performance specifications.

Single-LAB EPLDs



Multi-LAB EPLDs

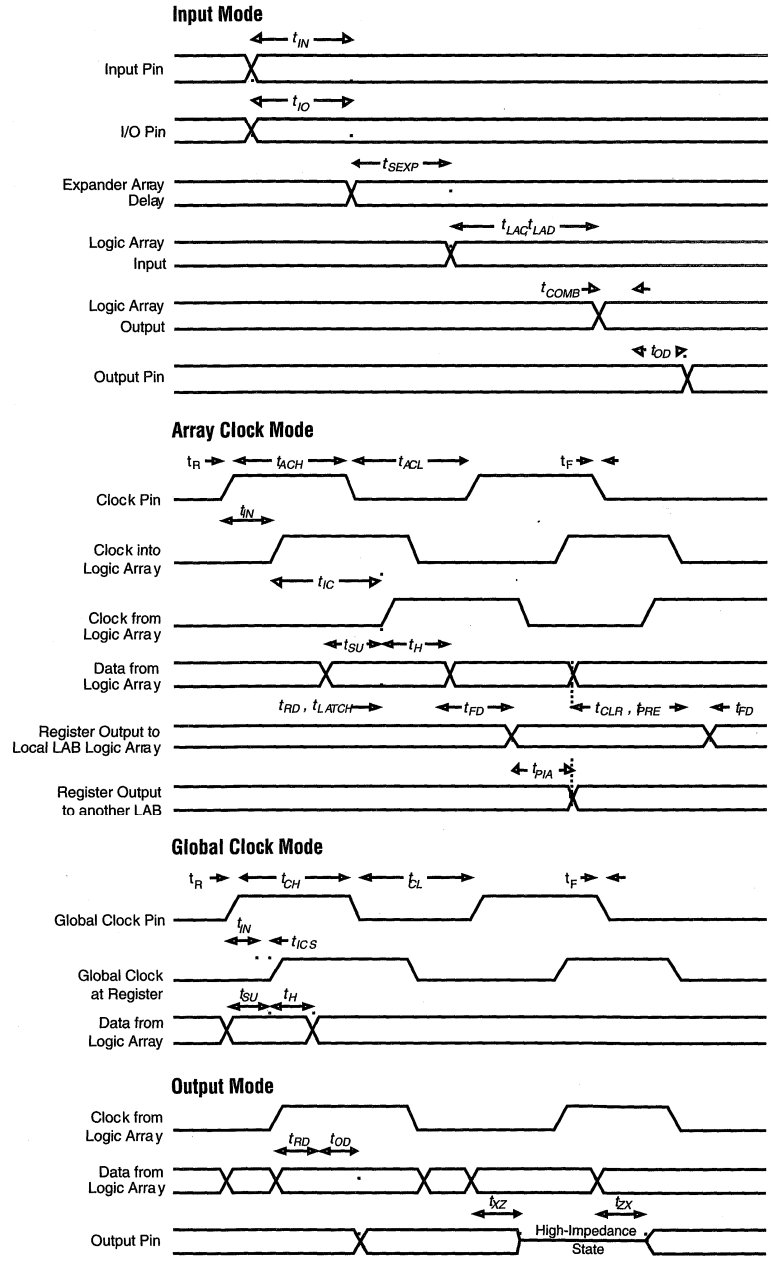


Timing information can be derived from the timing model and parameters for a particular EPLD. External timing parameters are calculated with the sum of internal parameters and represent pin-to-pin timing delays. Figure 6 shows the internal timing relationship for internal and external delay parameters. For more information on EPLD timing, refer to *Application Brief 100 (Understanding Classic, MAX 5000 & MAX 7000 Timing)* in this data book.

Figure 6. Switching Waveforms

In multi-LAB EPLDs, I/O pins that are used as inputs traverse the PIA.

t_R & t_F < 3 ns. Inputs are driven at 3 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.

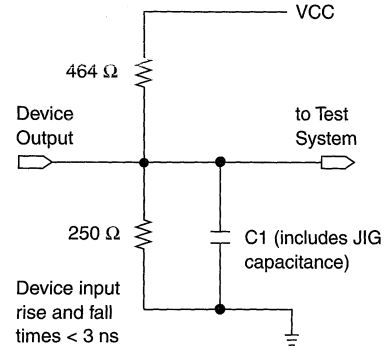


Generic Testing

MAX 5000 EPLDs are fully functionally tested and guaranteed. Complete testing of each programmable EPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those in Figure 7.

Figure 7. AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result.



Test patterns can be used and then erased during early stages of the device production flow. EPROM-based EPLDs in one-time-programmable windowless packages also contain on-board logic test circuitry to allow verification of function and AC specifications during this production flow.

Device Programming

All MAX 5000 EPLDs can be programmed on 486- and Pentium-based PCs with an Altera Logic Programmer card, the Master Programming Unit (MPU), and the appropriate device adapter. The MPU checks continuity to ensure adequate electrical contact between the adapter and the device. For more information, see *Altera Programming Hardware* in this data book.

MAX+PLUS II software can use text- or waveform-format test vectors created with the MAX+PLUS II Text or Waveform Editor to test a programmed device. For added design verification, designers can perform functional testing to compare the functional behavior of a MAX 5000 EPLD to the results of simulation. (This feature requires a device adapter with the "PLM-" prefix.)

Data I/O and other programming hardware manufacturers also offer programming support for Altera devices. For more information, see *Programming Hardware Manufacturers* in this data book.

QFP Carrier & Development Socket

MAX 5000 devices in 100-pin QFP packages are shipped in plastic carriers to protect the fragile QFP leads. Each carrier can be used with a prototype development socket and programming hardware available from Altera or Data I/O. This carrier technology makes it possible to program, test, erase, and reprogram devices without exposing the leads to mechanical stress. For detailed information and carrier dimensions, refer to the *QFP Carrier & Development Socket Data Sheet* in this data book.

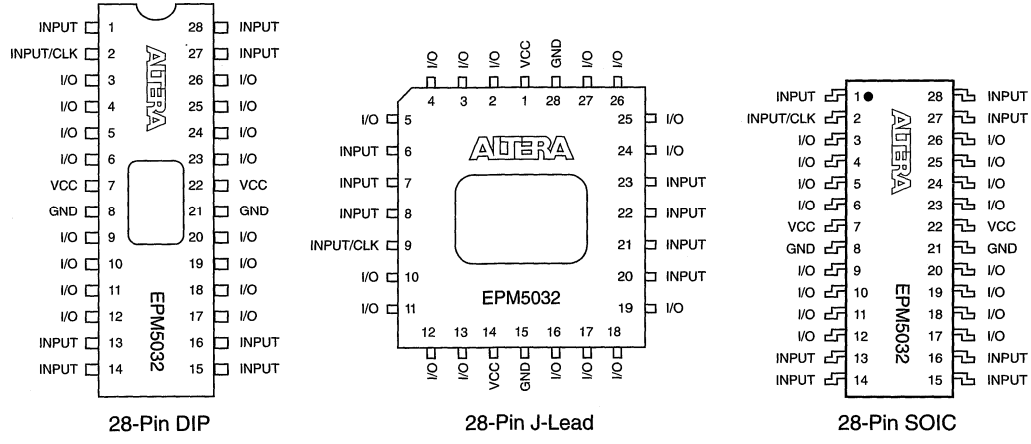
Notes:

Features

- High-speed, single-LAB MAX 5000 EPLD
  - t_{PD} as fast as 10 ns
  - Counter frequencies up to 125 MHz
  - Pipelined data rates up to 83 MHz
- 32 individually configurable macrocells
- 64 shareable expander product terms ("expanders") allowing 68 product terms on a single macrocell
- Programmable I/O architecture allowing up to 24 inputs or 16 outputs
- Available in 28-pin windowed ceramic and plastic one-time-programmable (OTP) packages (see Figure 8):
  - Dual in-line (CerDIP and PDIP)
  - J-lead chip carrier (JLCC and PLCC)
  - Small-outline integrated circuit (plastic SOIC only)
- Military devices available. For information, refer to the *Military Products Data Sheet* in this data book.

Figure 8. EPM5032 Package Pin-Out Diagrams

Package outlines not drawn to scale. Windows in ceramic packages only.



28-Pin DIP | 28-Pin J-Lead | 28-Pin SOIC

General Description

Altera EPM5032 EPLDs are MAX 5000 EPLDs optimized for speed. They can integrate multiple SSI, MSI TTL, or SSI and MSI TTL as well as CMOS logic devices. In addition, the EPM5032 can replace multiple 20-pin PAL or PLA devices and have logic left over for further integration. EPM5032 EPLDs contain 32 macrocells; the expander product-term array provides 64 expanders. The I/O control block contains 16 bidirectional I/O pins that can be configured for dedicated input, dedicated output, or bidirectional operation. All I/O pins feature dual feedback for maximum pin flexibility. See Figure 9.

Figure 9. EPM5032 Block Diagram

Numbers without parentheses are for DIP and SOIC packages. Numbers in parentheses are for J-lead packages.

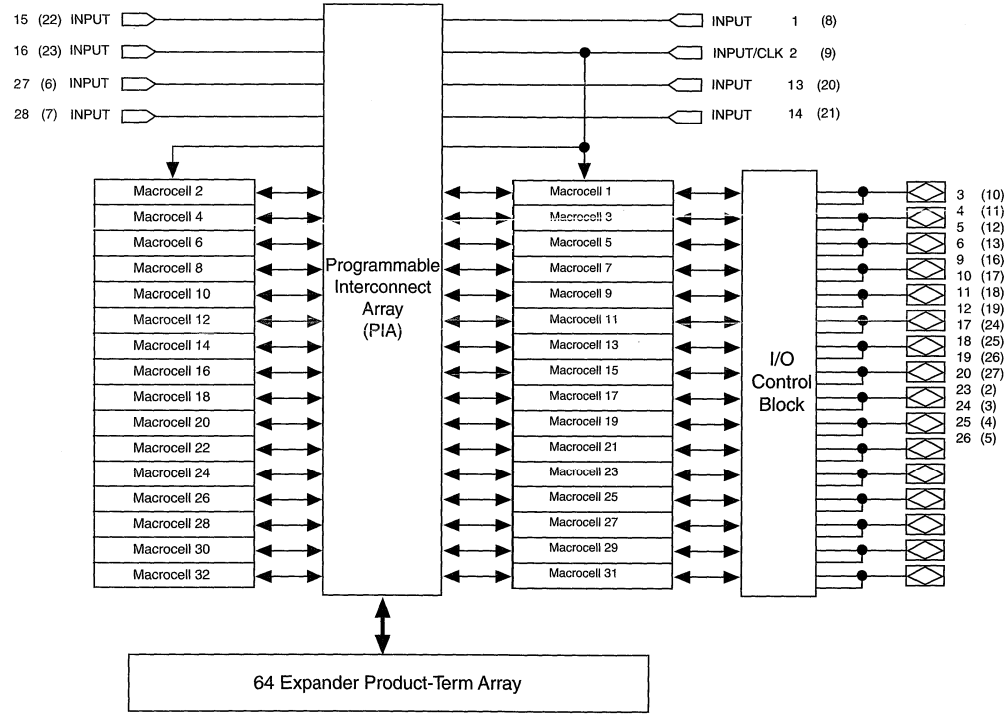
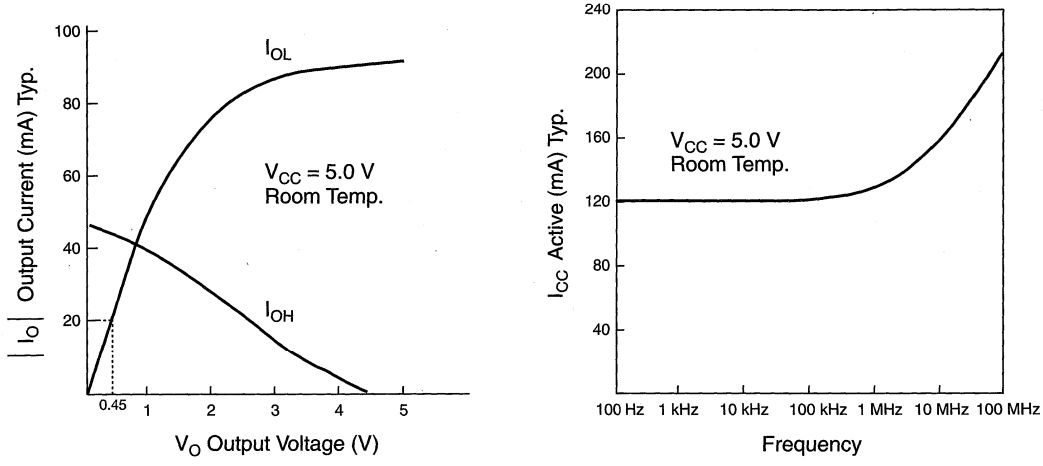


Figure 10 shows the output drive characteristics of EPM5032 I/O pins and typical supply current (I_{CC}) versus frequency.

Figure 10. Typical Output Drive Characteristics & I_{CC} vs. Frequency



Absolute Maximum Ratings See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*Note (1)*	–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			300	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1500	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias, *Note (2)*	–65 [–55]	150 [125]	° C
T_J	Junction temperature	Under bias, *Note (2)*		150 [175]	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	*Notes (3), (4)*	4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			100	ns
t_F	Input fall time			100	ns

DC Operating Conditions *Notes (5), (6)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage	*Note (2)*	2.0 [2.2]		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND, *Notes (3), (7)*		120	150 (200)	mA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, no load, f = 1.0 MHz, *Notes (3), (7)*		125	155 (225)	mA

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{IO}	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF

AC Operating Conditions *Note (6)*

External Timing Parameters			EPM5032A-10		EPM5032A-12		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		10		12	ns
t_{PD2}	I/O input to non-registered output			10		12	ns
t_{SU}	Global clock setup time		7		8		ns
t_{H}	Global clock hold time		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		6		7	ns
t_{CH}	Global clock high time		4		4.5		ns
t_{CL}	Global clock low time		4		4.5		ns
t_{ASU}	Array clock setup time		3		3		ns
t_{AH}	Array clock hold time		4		4		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		10		12	ns
t_{ACH}	Array clock high time		4		4.5		ns
t_{ACL}	Array clock low time		4		4.5		ns
t_{CNT}	Minimum global clock period			8		9	ns
f_{CNT}	Max. internal global clock frequency	*Note (7)*	125		111.1		MHz
t_{ACNT}	Minimum array clock period			8		9	ns
f_{ACNT}	Max. internal array clock frequency	*Note (7)*	125		111.1		MHz
f_{MAX}	Maximum clock frequency	*Note (9)*	125		111.1		MHz

Internal Timing Parameters *Note (10)*			EPM5032A-10		EPM5032A-12		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			2.5		2.5	ns
t_{IO}	I/O input pad and buffer delay			2.5		2.5	ns
t_{SEXP}	Expander array delay			6		8	ns
t_{LAD}	Logic array delay			4		5	ns
t_{LAC}	Logic control array delay			4		4	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		3		4	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		7		7	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		7		7	ns
t_{SU}	Register setup time		3		3		ns
t_{LATCH}	Flow-through latch delay			1		1	ns
t_{RD}	Register delay			0.5		0.5	ns
t_{COMB}	Combinatorial delay			0.5		0.5	ns
t_{H}	Register hold time		4		4		ns
t_{IC}	Array clock delay			4		5	ns
t_{ICS}	Global clock delay			0		0	ns
t_{FD}	Feedback delay			0.5		0.5	ns
t_{PRE}	Register preset time			5		5	ns
t_{CLR}	Register clear time			5		5	ns

AC Operating Conditions *Note (6)*

External Timing Parameters			EPM5032-15		EPM5032-17		EPM5032-20		EPM5032-25		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		15		17		20		25	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		15		17		20		25	ns
t_{SU}	Global clock setup time		9		10		12		15		ns
t_{H}	Global clock hold time		0		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		10		10		12		15	ns
t_{CH}	Global clock high time		6		6		7		8		ns
t_{CL}	Global clock low time		6		6		7		8		ns
t_{ASU}	Array clock setup time		5		5		6		8		ns
t_{AH}	Array clock hold time		5		5		6		8		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		15		15		18		22	ns
t_{ACH}	Array clock high time	*Note (8)*	6		6		7		9		ns
t_{ACL}	Array clock low time		7		8		9		11		ns
t_{CNT}	Minimum global clock period			13		14		16		20	ns
f_{CNT}	Max. internal global clock frequency	*Note (7)*	76.9		71.4		62.5		50		MHz
t_{ACNT}	Minimum array clock period			13		14		16		20	ns
f_{ACNT}	Max. internal array clock frequency	*Note (7)*	76.9		71.4		62.5		50		MHz
f_{MAX}	Maximum clock frequency	*Note (9)*	83.3		83.3		71.4		62.5		MHz

Internal Timing Parameters *Note (10)*			EPM5032-15		EPM5032-17		EPM5032-20		EPM5032-25		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			3		3		5		7	ns
t_{IO}	I/O input pad and buffer delay			3		3		5		7	ns
t_{SEXP}	Expander array delay			8		8		10		15	ns
t_{LAD}	Logic array delay			7		9		10		13	ns
t_{LAC}	Logic control array delay			4		4		4		4	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		4		4		4		4	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		7		7		7		7	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		7		7		7		7	ns
t_{SU}	Register setup time		4		3		4		5		ns
t_{LATCH}	Flow-through latch delay			1		1		1		1	ns
t_{RD}	Register delay			1		1		1		1	ns
t_{COMB}	Combinatorial delay			1		1		1		1	ns
t_{H}	Register hold time		5		7		8		10		ns
t_{IC}	Array clock delay			7		7		8		10	ns
t_{ICS}	Global clock delay			2		2		2		3	ns
t_{FD}	Feedback delay			1		1		1		1	ns
t_{PRE}	Register preset time			5		5		6		9	ns
t_{CLR}	Register clear time			5		5		6		9	ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Numbers in brackets are for MIL-STD-883-compliant versions only.
(3) Numbers in parentheses are for military- and industrial-temperature-range versions, as well as for MIL-STD-883-compliant versions.
(4) Maximum V_{CC} rise time for the EPM5032 is 10 ms. Maximum V_{CC} rise time for the EPM5032A is 200 ms.
(5) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(6) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C for military use.
(7) This parameter is measured with a device programmed as a 32-bit counter. I_{CC} measured at 0° C.
(8) This parameter is measured with a positive-edge-triggered Clock at the register. For negative-edge clocking, the t_{ACH} and t_{ACL} parameters must be swapped.
(9) The f_{MAX} values represent the highest frequency for pipelined data.
(10) For information on internal timing parameters, refer to *Application Brief 100 (Understanding Classic, MAX 5000 & MAX 7000 Timing)* in this data book.

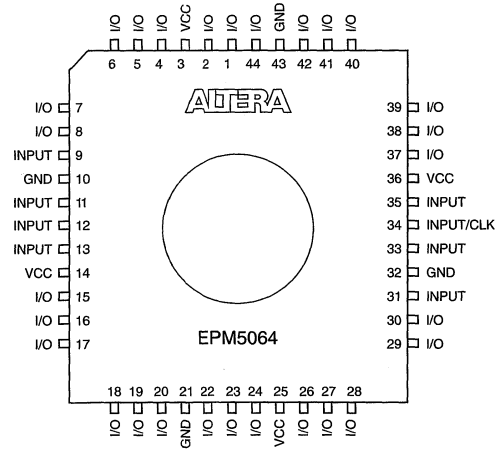
Notes:

Features

- High-density, 64-macrocell, general-purpose MAX 5000 EPLD
- High-speed multi-LAB architecture
  - t_{PD} as fast as 15 ns
  - Counter frequencies up to 83.3 MHz
  - Pipelined data rates up to 100 MHz
- 128 shareable expander product terms ("expanders") allowing over 32 product terms in a single macrocell
- Programmable I/O architecture allowing up to 36 inputs or 28 outputs
- Available in 44-pin windowed ceramic and one-time-programmable (OTP) J-lead chip carrier (JLCC and PLCC) packages, see Figure 11
- Easy integration of 10 standard PALs in 1/2-square-inch of board space
- Military devices available. For information, refer to the *Military Products Data Sheet* in this data book.

Figure 11. EPM5064 Package Pin-Out Diagram

Package outline not drawn to scale. Windows in ceramic packages only.



44-Pin J-Lead

General Description

Altera EPM5064 EPLDs are user-configurable, high-performance MAX 5000 EPLDs that serve as high-density replacements for 74-series SSI, MSI TTL, and CMOS logic. In addition, these devices can integrate multiple 20- and 24-pin low-density PLDs. For example, the EPM5064 can integrate the logic contained in over 10 standard 20-pin PALs.

The EPM5064 consists of 64 macrocells equally divided into 4 Logic Array Blocks (LABs) with 16 macrocells. Each LAB also contains 32 expander product terms. They each have 8 dedicated input pins, one of which can be used as a global system Clock that provides enhanced Clock-to-output delays. The device has 28 I/O pins that can be configured for input, output, or bidirectional operation. All I/O pins feature dual-feedback for maximum pin flexibility. Two of the LABs have 8 I/O pins, ensuring high speed for 8-bit bus functions; the other two LABs have 6 I/O pins. See Figure 12.

Figure 12. EPM5064 Block Diagram

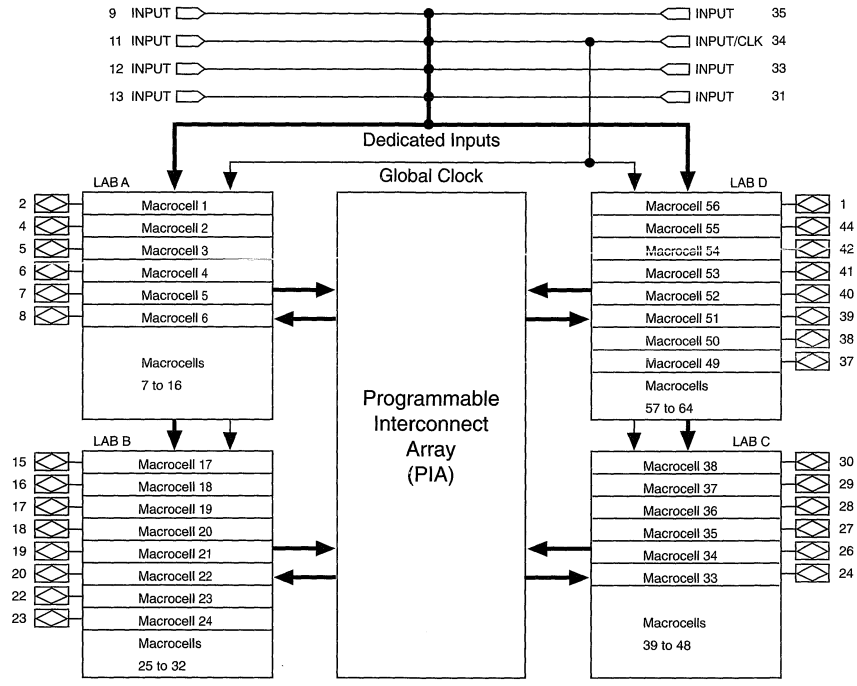
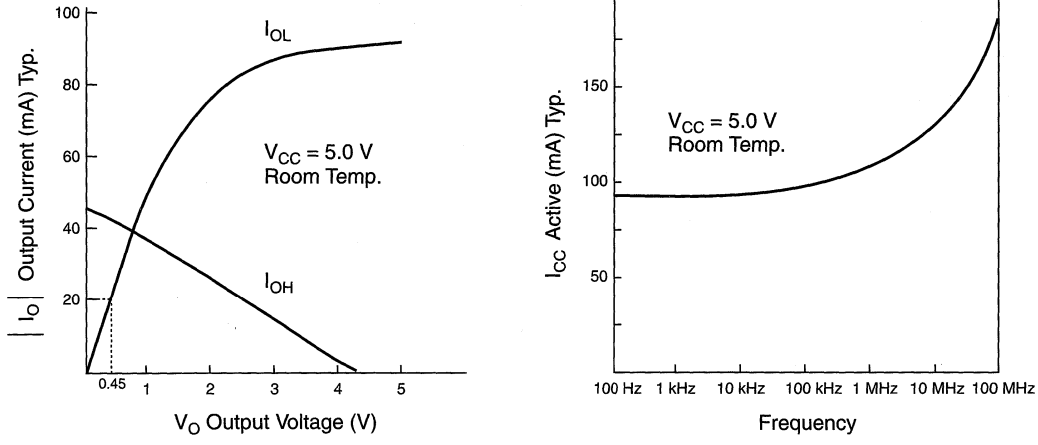


Figure 13 shows the output drive characteristics of EPM5064 I/O pins and typical supply current (I_{CC}) versus frequency. The high integration density of this device can greatly reduce system power requirements.

Figure 13. Typical Output Drive Characteristics & I_{CC} vs. Frequency



Absolute Maximum Ratings

See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*Note (1)*	–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			400	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			2000	mW
T_{STG}	Storage temperature	No bias	–65	150	°C
T_{AMB}	Ambient temperature	Under bias	–65	135	°C
T_J	Junction temperature	Under bias		150	°C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	*Notes (2),(3)*	4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	°C
T_A	Operating temperature	For industrial use	–40	85	°C
T_C	Case temperature	For military use	–55	125	°C
t_R	Input rise time			100	ns
t_F	Input fall time			100	ns

DC Operating Conditions *Notes (4), (5)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND, *Notes (2), (6)*		90	125 (200)	mA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, no load, f = 1.0 MHz, *Notes (2), (6)*		95	135 (225)	mA

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{IO}	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF

AC Operating Conditions *Note (5)*

External Timing Parameters			EPM5064A-15		EPM5064A-20		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		15		20	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		25		33	ns
t_{SU}	Global clock setup time		10		13		ns
t_{H}	Global clock hold time		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		8		9	ns
t_{CH}	Global clock high time		5		7		ns
t_{CL}	Global clock low time		5		7		ns
t_{ASU}	Array clock setup time		5		6		ns
t_{AH}	Array clock hold time		5		6		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		15		20	ns
t_{ACH}	Array clock high time		5		7		ns
t_{ACL}	Array clock low time		5		7		ns
t_{CNT}	Minimum global clock period			12		15	ns
f_{CNT}	Max. internal global clock frequency	*Note (6)*	83.3		66.7		MHz
t_{ACNT}	Minimum array clock period			12		15	ns
f_{ACNT}	Max. internal array clock frequency	*Note (6)*	83.3		66.7		MHz
f_{MAX}	Maximum clock frequency	*Note (8)*	100.0		71.4		MHz

Internal Timing Parameters *Note (9)*			EPM5064A-15		EPM5064A-20		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			3		4	ns
t_{IO}	I/O input pad and buffer delay			3		4	ns
t_{SEXP}	Expander array delay			8		10	ns
t_{LAD}	Logic array delay			8		12	ns
t_{LAC}	Logic control array delay			5		5	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		3		3	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		5		5	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		5		5	ns
t_{SU}	Register setup time		2		1		ns
t_{LATCH}	Flow-through latch delay			1		1	ns
t_{RD}	Register delay			1		1	ns
t_{COMB}	Combinatorial delay			1		1	ns
t_{H}	Register hold time		7		10		ns
t_{IC}	Array clock delay			6		8	ns
t_{ICS}	Global clock delay			0		0	ns
t_{FD}	Feedback delay			1		1	ns
t_{PRE}	Register preset time			3		3	ns
t_{CLR}	Register clear time			3		3	ns
t_{PIA}	Programmable Interconnect Array delay			10		13	ns

AC Operating Conditions *Note (5)*

External Timing Parameters			EPM5064-1		EPM5064-2		EPM5064		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		25		30		35	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		40		45		55	ns
t_{SU}	Global clock setup time		15		20		25		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		14		16		20	ns
t_{CH}	Global clock high time		8		10		12.5		ns
t_{CL}	Global clock low time		8		10		12.5		ns
t_{ASU}	Array clock setup time		5		6		10		ns
t_{AH}	Array clock hold time		6		8		10		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		25		30		35	ns
t_{ACH}	Array clock high time	*Note (7)*	11		14		16		ns
t_{ACL}	Array clock low time	*Note (7)*	9		11		14		ns
t_{CNT}	Minimum global clock period			20		25		30	ns
f_{CNT}	Max. internal global clock frequency	*Note (6)*	50		40		33.3		MHz
t_{ACNT}	Minimum array clock period			20		25		30	ns
f_{ACNT}	Max. internal array clock frequency	*Note (6)*	50		40		33.3		MHz
f_{MAX}	Maximum clock frequency	*Note (8)*	62.5		50		40		MHz

Internal Timing Parameters *Note (9)*			EPM5064-1		EPM5064-2		EPM5064		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			5		7		11	ns
t_{IO}	I/O input pad and buffer delay			6		6		11	ns
t_{SEXP}	Expander array delay			12		14		20	ns
t_{LAD}	Logic array delay			12		14		14	ns
t_{LAC}	Logic control array delay			10		12		13	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		5		5		6	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		10		11		13	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		10		11		13	ns
t_{SU}	Register setup time		6		8		12		ns
t_{LATCH}	Flow-through latch delay			3		4		4	ns
t_{RD}	Register delay			1		2		2	ns
t_{COMB}	Combinatorial delay			3		4		4	ns
t_{H}	Register hold time		4		6		8		ns
t_{IC}	Array clock delay			14		16		16	ns
t_{ICS}	Global clock delay			3		2		1	ns
t_{FD}	Feedback delay			1		1		2	ns
t_{PRE}	Register preset time			5		6		7	ns
t_{CLR}	Register clear time			5		6		7	ns
t_{PIA}	Prog. Interconnect Array delay			14		16		20	ns

Notes to tables:

(1) Minimum DC input is -0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.

(2) Numbers in parentheses are for military- and industrial-temperature-range versions.

(3) Maximum V_{CC} rise time for the EPM5064/EPM5064A is 200 ms.

(4) Typical values are for T_A = 25° C and V_{CC} = 5 V.

(5) Operating conditions: $V_{CC} = 5\ V \pm 5\%$, T_A = 0° C to 70° C for commercial use.
$V_{CC} = 5\ V \pm 10\%$, T_A = –40° C to 85° C for industrial use.
$V_{CC} = 5\ V \pm 10\%$, T_C = –55° C to 125° C for military use.

(6) Measured with a 16-bit counter programmed into each LAB. I_{CC} measured at 0° C.

(7) This parameter is measured with a positive-edge-triggered Clock at the register. For negative-edge clocking, the t_{ACH} and t_{ACL} parameters must be swapped.

(8) The f_{MAX} values represent the highest frequency for pipelined data.

(9) For information on internal timing parameters, refer to *Application Brief 100 (Understanding Classic, MAX 5000 & MAX 7000 Timing)* in this data book.

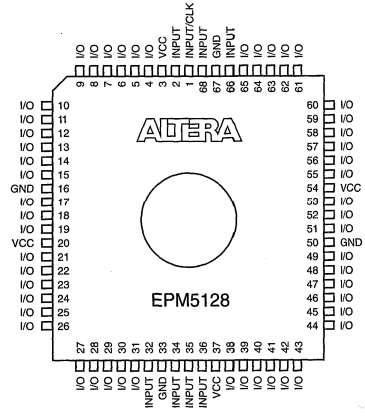
Notes:

Features

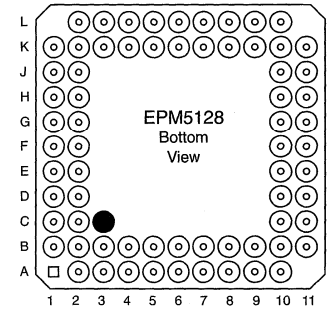
- High-density, 128-macrocell, general-purpose MAX 5000 EPLD
- High-speed multi-LAB architecture
  - t_{PD} as fast as 15 ns
  - Counter frequencies up to 83.3 MHz
  - Pipelined data rates up to 100 MHz
- 256 shareable expander product terms ("expanders") allowing over 32 product terms in a single macrocell
- Programmable I/O architecture allowing up to 60 inputs or 52 outputs
- Available in windowed ceramic and plastic one-time-programmable (OTP) packages (see Figure 14):
  - 68-pin J-lead chip carrier (JLCC and PLCC)
  - 68-pin grid array (ceramic PGA only)
- Military devices available. For information, refer to the *Military Products Data Sheet* in this data book.

Figure 14. EPM5128 Package Pin-Out Diagrams

Package outlines not drawn to scale. See Tables 4 and 5 in this data sheet for pin-out information. Windows in ceramic packages only.



68-Pin J-Lead



68-Pin PGA

General Description

Altera EPM5128 EPLDs are user-configurable, high-performance MAX 5000 EPLDs that provide high-density replacements for 74-series SSI, MSI TTL, and CMOS logic. For example, a 74161 counter uses only 3% of the EPM5128 EPLD. These devices can replace over 60 TTL MSI and SSI components and integrate multiple 20- and 24-pin low-density PLDs.

The EPM5128 consists of 128 macrocells equally divided into 8 Logic Array Blocks (LABs) of 16 macrocells. Each LAB also contains 32 expander product terms. They each have 8 dedicated input pins, one of which can be used as a global system Clock. These devices contain 52 I/O pins that can be configured for input, output, or bidirectional operation. Four of the LABs have 8 I/O pins; the other 4 have 5 I/O pins. See Figure 15.

Figure 15. EPM5128 Block Diagram

Numbers without parentheses are for J-lead packages. Numbers in parentheses are for PGA packages

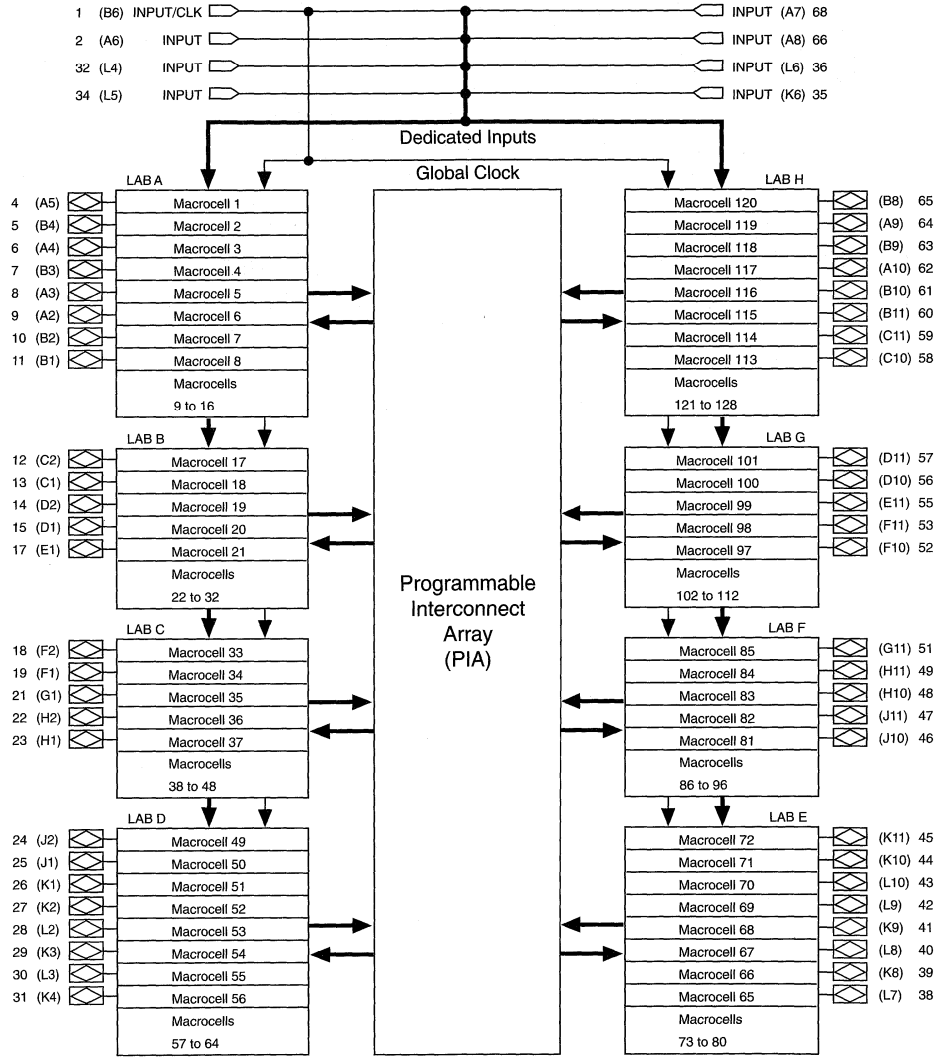
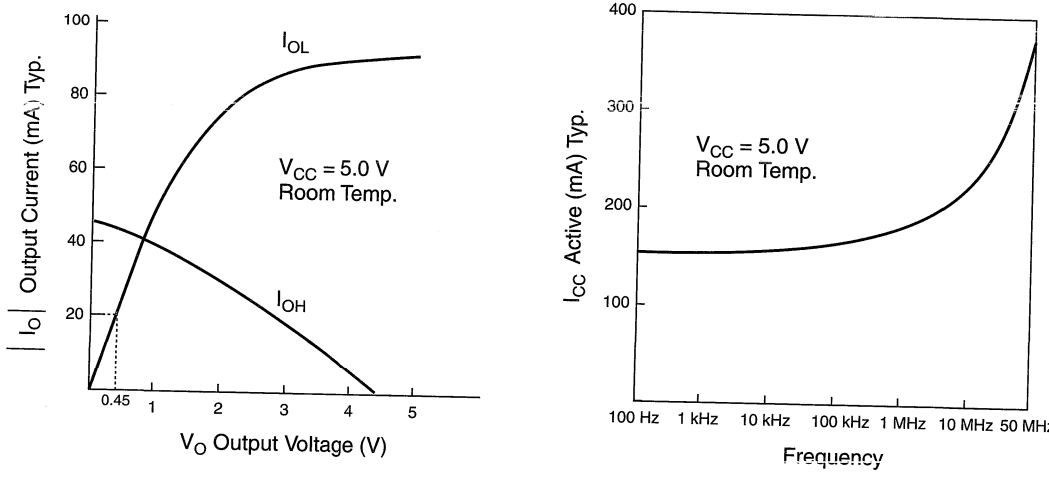


Figure 16 shows the output drive characteristics of EPM5128 I/O pins and typical supply current (I_{CC}) versus frequency.

Figure 16. Typical Output Drive Characteristics & I_{CC} vs. Frequency



Absolute Maximum Ratings

See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*Note (1)*	–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			500	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			2500	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias, *Note (2)*	–65 [–55]	135 [125]	° C
T_J	Junction temperature	Under bias, *Note (2)*		150 [175]	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	*Notes (3), (4)*	4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			100	ns
t_F	Input fall time			100	ns

DC Operating Conditions *Notes (5), (6)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage	*Note (2)*	2.0 [2.2]		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND, *Notes (3), (7)*		150	225 (300)	mA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *Notes (3), (7)*		155	250 (350)	mA

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{IO}	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF

AC Operating Conditions *Note (6)*

External Timing Parameters			EPM5128A-15		EPM5128A-20		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		15		20	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		25		33	ns
t_{SU}	Global clock setup time		10		13		ns
t_{H}	Global clock hold time		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		8		9	ns
t_{CH}	Global clock high time		5		7		ns
t_{CL}	Global clock low time		5		7		ns
t_{ASU}	Array clock setup time		5		6		ns
t_{AH}	Array clock hold time		5		6		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		15		20	ns
t_{ACH}	Array clock high time		5		7		ns
t_{ACL}	Array clock low time		5		7		ns
t_{CNT}	Minimum global clock period			12		15	ns
f_{CNT}	Max. internal global clock frequency	*Note (7)*	83.3		66.7		MHz
t_{ACNT}	Minimum array clock period			12		15	ns
f_{ACNT}	Max. internal array clock frequency	*Note (7)*	83.3		66.7		MHz
f_{MAX}	Maximum clock frequency	*Note (9)*	100.0		71.4		MHz

Internal Timing Parameters *Note (10)*			EPM5128A-15		EPM5128A-20		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			3		4	ns
t_{IO}	I/O input pad and buffer delay			3		4	ns
t_{SEXP}	Expander array delay			8		10	ns
t_{LAD}	Logic array delay			8		12	ns
t_{LAC}	Logic control array delay			5		5	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		3		3	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		5		5	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		5		5	ns
t_{SU}	Register setup time		2		1		ns
t_{LATCH}	Flow-through latch delay			1		1	ns
t_{RD}	Register delay			1		1	ns
t_{COMB}	Combinatorial delay			1		1	ns
t_{H}	Register hold time		7		10		ns
t_{IC}	Array clock delay			6		8	ns
t_{ICS}	Global clock delay			0		0	ns
t_{FD}	Feedback delay			1		1	ns
t_{PRE}	Register preset time			3		3	ns
t_{CLR}	Register clear time			3		3	ns
t_{PIA}	Prog. Interconnect Array delay			10		13	ns

AC Operating Conditions *Note (6)*

External Timing Parameters			EPM5128-1		EPM5128-2		EPM5128		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		25		30		35	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		40		45		55	ns
t_{SU}	Global clock setup time		15		20		25		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		14		16		20	ns
t_{CH}	Global clock high time		8		10		12.5		ns
t_{CL}	Global clock low time		8		10		12.5		ns
t_{ASU}	Array clock setup time		5		6		10		ns
t_{AH}	Array clock hold time		6		8		10		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		25		30		35	ns
t_{ACH}	Array clock high time	*Note (8)*	11		14		16		ns
t_{ACL}	Array clock low time	*Note (8)*	9		11		14		ns
t_{CNT}	Minimum global clock period			20		25		30	ns
f_{CNT}	Max. internal global clock frequency	*Note (7)*	50		40		33.3		MHz
t_{ACNT}	Minimum array clock period			20		25		30	ns
f_{ACNT}	Max. internal array clock frequency	*Note (7)*	50		40		33.3		MHz
f_{MAX}	Maximum clock frequency	*Note (9)*	62.5		50		40		MHz

Internal Timing Parameters *Note (10)*			EPM5128-1		EPM5128-2		EPM5128		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			5		7		11	ns
t_{IO}	I/O input pad and buffer delay			6		6		11	ns
t_{SEXP}	Expander array delay			12		14		20	ns
t_{LAD}	Logic array delay			12		14		14	ns
t_{LAC}	Logic control array delay			10		12		13	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		5		5		6	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		10		11		13	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		10		11		13	ns
t_{SU}	Register setup time		6		8		12		ns
t_{LATCH}	Flow-through latch delay			3		4		4	ns
t_{RD}	Register delay			1		2		2	ns
t_{COMB}	Combinatorial delay			3		4		4	ns
t_{H}	Register hold time		4		6		8		ns
t_{IC}	Array clock delay			14		16		16	ns
t_{ICS}	Global clock delay			3		2		1	ns
t_{FD}	Feedback delay			1		1		2	ns
t_{PRE}	Register preset time			5		6		7	ns
t_{CLR}	Register clear time			5		6		7	ns
t_{PIA}	Prog. Interconnect Array delay			14		16		20	ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Numbers in brackets are for MIL-STD-883-compliant versions.
(3) Numbers in parentheses are for military- and industrial-temperature-range versions, as well as for MIL-STD-883-compliant versions.
(4) Maximum V_{CC} rise time for the EPM5128/EPM5128A is 200 ms.
(5) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(6) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C for military use.
(7) Measured with a 16-bit counter programmed into each LAB. I_{CC} measured at 0° C.
(8) This parameter is measured with a positive-edge-triggered Clock at the register. For negative-edge clocking, the t_{ACH} and t_{ACL} parameters must be swapped.
(9) The f_{MAX} values represent the maximum frequency for pipelined data.
(10) For information on internal timing parameters, refer to *Application Brief 100 (Understanding Classic, MAX 5000 & MAX 7000 Timing)* in this data book.

Pin-Out Information

Tables 4 and 5 provide pin-out information for the EPM5128.

Table 4. EPM5128 Dedicated Pin-Outs

Dedicated Pin	68-Pin J-Lead	68-Pin PGA
INPUT/CLK	1	B6
INPUT	2, 32, 34, 35, 36, 66, 68	A6, L4, L5, L6, K6, A8, A7
GND	16, 33, 50, 67	B7, E2, G10, K5
VCC	3, 20, 37, 54	B5, E10, G2, K7

Table 5. EPM5128 I/O Pin-Outs (Part 1 of 2)

MC	LAB	68-Pin J-Lead	68-Pin PGA	MC	LAB	68-Pin J-Lead	68-Pin PGA
1	A	4	A5	17	B	12	C2
2	A	5	B4	18	B	13	C1
3	A	6	A4	19	B	14	D2
4	A	7	B3	20	B	15	D1
5	A	8	A3	21	B	17	E1
6	A	9	A2	22	B	–	–
7	A	10	B2	23	B	–	–
8	A	11	B1	24	B	–	–
9	A	–	–	25	B	–	–
10	A	–	–	26	B	–	–
11	A	–	–	27	B	–	–
12	A	–	–	28	B	–	–
13	A	–	–	29	B	–	–
14	A	–	–	30	B	–	–
15	A	–	–	31	B	–	–
16	A	–	–	32	B	–	–
33	C	18	F2	49	D	24	J2
34	C	19	F1	50	D	25	J1
35	C	21	G1	51	D	26	K1
36	C	22	H2	52	D	27	K2
37	C	23	H1	53	D	28	L2
38	C	–	–	54	D	29	K3
39	C	–	–	55	D	30	L3
40	C	–	–	56	D	31	K4
41	C	–	–	57	D	–	–
42	C	–	–	58	D	–	–
43	C	–	–	59	D	–	–
44	C	–	–	60	D	–	–
45	C	–	–	61	D	–	–
46	C	–	–	62	D	–	–
47	C	–	–	63	D	–	–
48	C	–	–	64	D	–	–

Table 5. EPM5128 I/O Pin-Outs (Part 2 of 2)

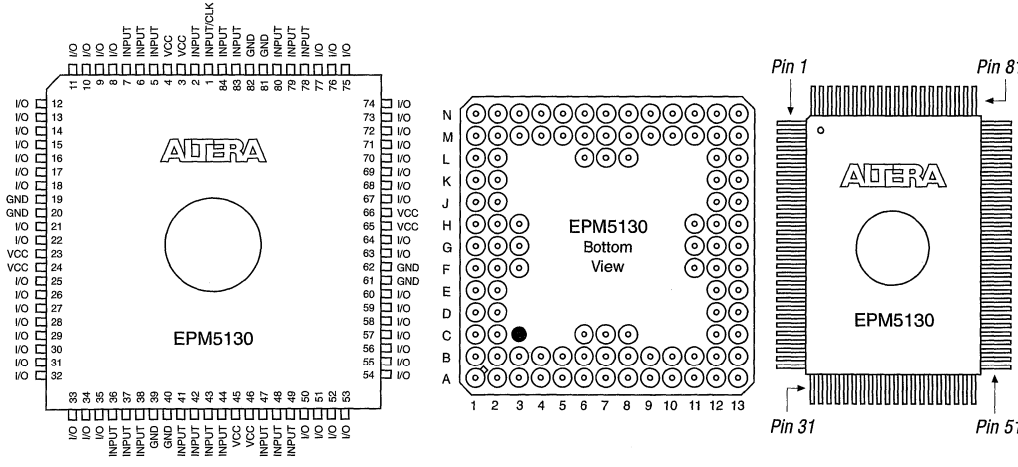
MC	LAB	68-Pin J-Lead	68-Pin PGA	MC	LAB	68-Pin J-Lead	68-Pin PGA
65	E	38	L7	81	F	46	J10
66	E	39	K8	82	F	47	J11
67	E	40	L8	83	F	48	H10
68	E	41	K9	84	F	49	H11
69	E	42	L9	85	F	51	G11
70	E	43	L10	86	F	–	–
71	E	44	K10	87	F	–	–
72	E	45	K11	88	F	–	–
73	E	–	–	89	F	–	–
74	E	–	–	90	F	–	–
75	E	–	–	91	F	–	–
76	E	–	–	92	F	–	–
77	E	–	–	93	F	–	–
78	E	–	–	94	F	–	–
79	E	–	–	95	F	–	–
80	E	–	–	96	F	–	–
97	G	52	F10	113	H	58	C10
98	G	53	F11	114	H	59	C11
99	G	55	E11	115	H	60	B11
100	G	56	D10	116	H	61	B10
101	G	57	D11	117	H	62	A10
102	G	–	–	118	H	63	B9
103	G	–	–	119	H	64	A9
104	G	–	–	120	H	65	B8
105	G	–	–	121	H	–	–
106	G	–	–	122	H	–	–
107	G	–	–	123	H	–	–
108	G	–	–	124	H	–	–
109	G	–	–	125	H	–	–
110	G	–	–	126	H	–	–
111	G	–	–	127	H	–	–
112	G	–	–	128	H	–	–

Features

- High-density, 128-macrocell, general-purpose MAX 5000 EPLD
- 128 macrocells optimized for pin-intensive applications, easily integrating over 60 TTL MSI and SSI components
- High-speed multi-LAB architecture
  - t_{PD} as fast as 15 ns
  - Counter frequencies up to 83.3 MHz
  - Pipelined data rates up to 100 MHz
- High pin count for 16- or 32-bit data paths
- 256 shareable expander product terms ("expanders") allowing over 32 product terms in a single macrocell
- 20 high-speed dedicated inputs for fast latching of 16-bit functions
- Fast Clock-to-output delays for bus-oriented functions
- Programmable I/O architecture with up to 84 inputs or 64 outputs in 100-pin packages, or up to 68 inputs or 48 outputs in 84-pin packages
- Available in windowed ceramic and one-time-programmable (OTP) packages (see Figure 17):
  - 84-pin J-lead chip carrier (JLCC and PLCC)
  - 100-pin pin-grid array (ceramic PGA only)
  - 100-pin quad flat pack (CQFP and PQFP)
- Military devices available. For information, refer to the *Military Products Data Sheet* in this data book.

Figure 17. EPM5130 Package Pin-Out Diagrams

Package outlines not drawn to scale. See Tables 6 and 7 in this data sheet for pin-out information. Windows in ceramic packages only.



84-Pin J-Lead 100-Pin PGA 100-Pin QFP

General Description

Altera EPM5130 EPLDs are user-configurable, high-performance MAX 5000 EPLDs optimized for pin-intensive designs. They provide high-density replacements for 74-series SSI, MSI TTL, and CMOS logic. These EPLDs can quickly integrate multiple 20- and 24-pin low-density PLDs and high-pin-count subsystems, such as custom DMA controllers. In addition, they can handle a 32-bit data path application with enough I/O to implement the required control signals.

The EPM5130 consists of 128 macrocells equally divided into 8 Logic Array Blocks (LABs), each containing 16 macrocells and 32 expander product terms. Expander product terms can be used and shared by all macrocells in the device to ensure efficient use of device resources. Because the LAB is very compact, the high speeds required by most I/O subsystems are maintained. See Figure 18.

The EPM5130 has 20 dedicated input pins that allow high-speed input latching of 16-bit functions. One of these inputs can be configured as a global Clock to provide enhanced Clock-to-output delays for bus-oriented functions. They also have 64 I/O pins, 8 in each LAB, that can be configured for input, output, or bidirectional operation. Dual feedback on the I/O pins provides the most efficient use of device pin resources.

Figure 18. EPM5130 Block Diagram

Numbers without parentheses are for QFP packages; numbers in parentheses are for PGA packages; numbers in brackets are for J-lead packages.

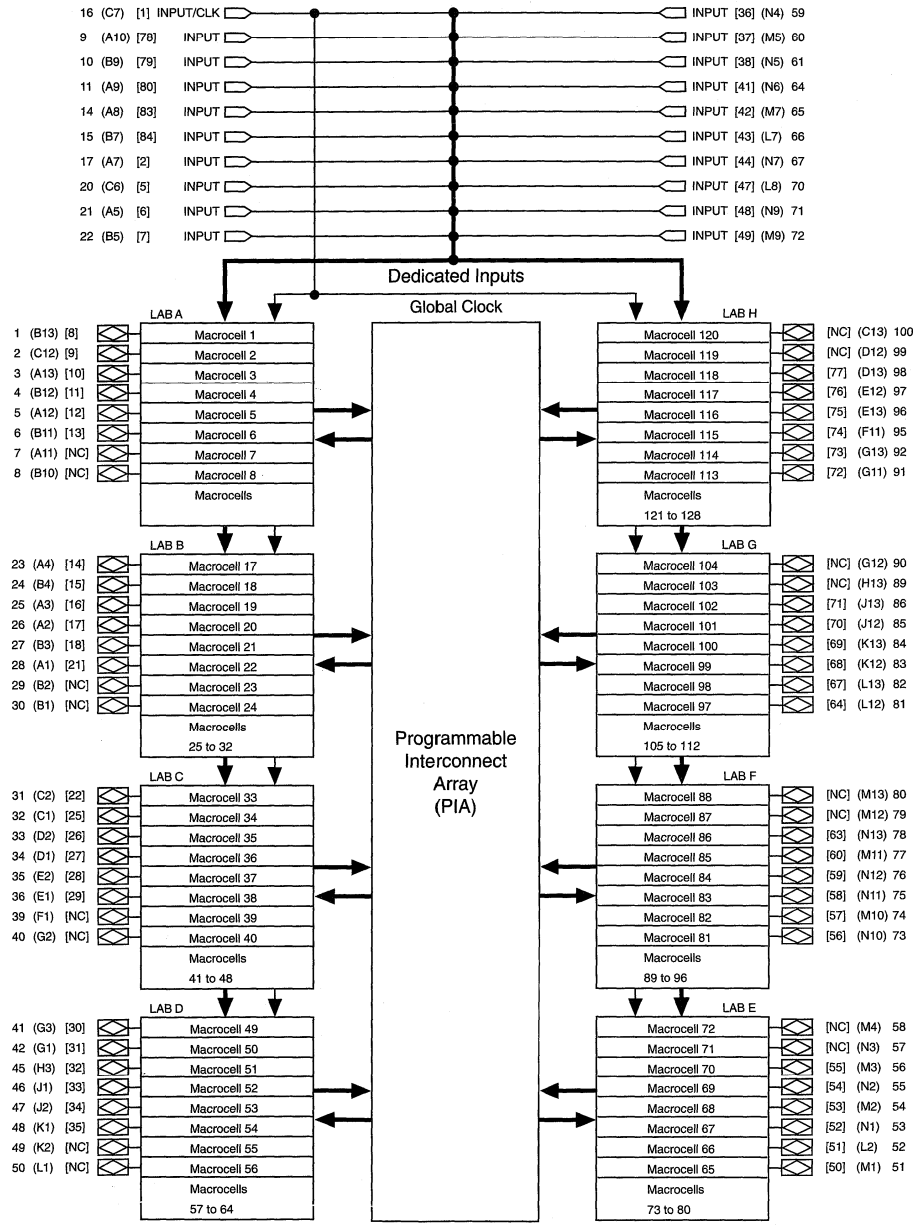
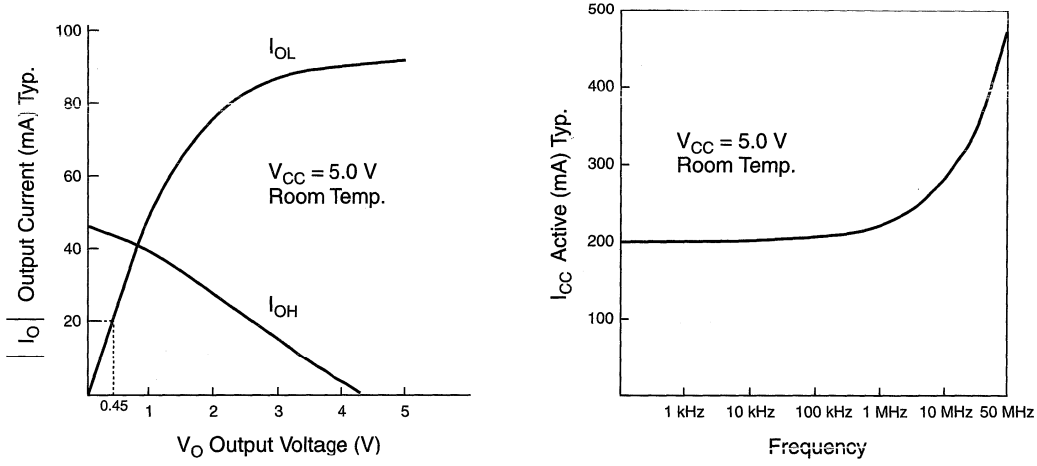


Figure 19 shows the output drive characteristics of EPM5130 I/O pins and typical supply current (I_{CC}) versus frequency.

Figure 19. Typical Output Drive Characteristics & I_{CC} vs. Frequency



Absolute Maximum Ratings

See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*Note (1)*	–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			500	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			2500	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias, *Note (2)*	–65 [–55]	135 [125]	° C
T_J	Junction temperature	Under bias, *Note (2)*		150 [175]	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	*Notes (3), (4)*	4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			100	ns
t_F	Input fall time			100	ns

DC Operating Conditions *Notes (5), (6)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage	*Note (2)*	2.0 [2.2]		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND, *Notes (3), (7)*		175	250 (325)	mA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *Notes (3), (7)*		180	275 (375)	mA

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{IO}	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF

AC Operating Conditions *Note (6)*

External Timing Parameters			EPM5130A-15		EPM5130A-20		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		15		20	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		25		33	ns
t_{SU}	Global clock setup time		10		13		ns
t_{H}	Global clock hold time		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		8		9	ns
t_{CH}	Global clock high time		5		7		ns
t_{CL}	Global clock low time		5		7		ns
t_{ASU}	Array clock setup time		5		6		ns
t_{AH}	Array clock hold time		5		6		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		15		20	ns
t_{ACH}	Array clock high time	*Note (8)*	5		7		ns
t_{ACL}	Array clock low time	*Note (5)*	5		7		ns
t_{CNT}	Minimum global clock period			12		15	ns
f_{CNT}	Max. internal global clock frequency	*Note (7)*	83.3		66.7		MHz
t_{ACNT}	Minimum array clock period			12		15	ns
f_{ACNT}	Max. internal array clock frequency	*Note (7)*	83.3		66.7		MHz
f_{MAX}	Maximum clock frequency	*Note (9)*	100.0		71.4		MHz

Internal Timing Parameters *Note (10)*			EPM5130A-15		EPM5130A-20		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			3		4	ns
t_{IO}	I/O input pad and buffer delay			3		4	ns
t_{SEXP}	Expander array delay			8		10	ns
t_{LAD}	Logic array delay			8		12	ns
t_{LAC}	Logic control array delay			5		5	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		3		3	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		5		5	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		5		5	ns
t_{SU}	Register setup time		2		1		ns
t_{LATCH}	Flow-through latch delay			1		1	ns
t_{RD}	Register delay			1		1	ns
t_{COMB}	Combinatorial delay			1		1	ns
t_{H}	Register hold time		7		10		ns
t_{IC}	Array clock delay			6		8	ns
t_{ICS}	Global clock delay			0		0	ns
t_{FD}	Feedback delay			1		1	ns
t_{PRE}	Register preset time			3		3	ns
t_{CLR}	Register clear time			3		3	ns
t_{PIA}	Prog. Interconnect Array delay			10		13	ns

AC Operating Conditions *Note (6)*

External Timing Parameters			EPM5130-1		EPM5130-2		EPM5130		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		25		30		35	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		40		45		55	ns
t_{SU}	Global clock setup time		15		20		25		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		14		16		20	ns
t_{CH}	Global clock high time		8		10		12.5		ns
t_{CL}	Global clock low time		8		10		12.5		ns
t_{ASU}	Array clock setup time		5		6		10		ns
t_{AH}	Array clock hold time		6		8		10		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		25		30		35	ns
t_{ACH}	Array clock high time	*Note (8)*	11		14		16		ns
t_{ACL}	Array clock low time	*Note (8)*	9		11		14		ns
t_{CNT}	Minimum global clock period			20		25		30	ns
f_{CNT}	Max. internal global clock frequency	*Note (7)*	50		40		33.3		MHz
t_{ACNT}	Minimum array clock period			20		25		30	ns
f_{ACNT}	Max. internal array clock frequency	*Note (7)*	50		40		33.3		MHz
f_{MAX}	Maximum clock frequency	*Note (9)*	62.5		50		40		MHz

Internal Timing Parameters *Note (10)*			EPM5130-1		EPM5130-2		EPM5130		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			5		7		11	ns
t_{IO}	I/O input pad and buffer delay			6		6		11	ns
t_{SEXP}	Expander array delay			12		14		20	ns
t_{LAD}	Logic array delay			12		14		14	ns
t_{LAC}	Logic control array delay			10		12		13	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		5		5		6	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		10		11		13	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		10		11		13	ns
t_{SU}	Register setup time		6		8		12		ns
t_{LATCH}	Flow-through latch delay			3		4		4	ns
t_{RD}	Register delay			1		2		2	ns
t_{COMB}	Combinatorial delay			3		4		4	ns
t_{H}	Register hold time		4		6		8		ns
t_{IC}	Array clock delay			14		16		16	ns
t_{ICS}	Global clock delay			3		2		1	ns
t_{FD}	Feedback delay			1		1		2	ns
t_{PRE}	Register preset time			5		6		7	ns
t_{CLR}	Register clear time			5		6		7	ns
t_{PIA}	Prog. Interconnect Array delay			14		16		20	ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Numbers in brackets are for MIL-STD-883-compliant versions only.
(3) Numbers in parentheses are for military- and industrial-temperature-range versions, as well as for MIL-STD-883-compliant versions.
(4) Maximum V_{CC} rise time for the EPM5130/EPM5130A is 200 ms.
(5) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(6) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C for military use.
(7) Measured with a 16-bit counter programmed into each LAB. I_{CC} measured at 0° C.
(8) This parameter is measured with a positive-edge-triggered Clock at the register. For negative-edge clocking, the t_{ACH} and t_{ACL} parameters must be swapped.
(9) The f_{MAX} values represent the highest frequency for pipelined data.
(10) For information on internal timing parameters, refer to *Application Brief 100 (Understanding Classic, MAX 5000 & MAX 7000 Timing)* in this data book.

Pin-Out Information

Tables 6 and 7 provide pin-out information for the EPM5130.

Table 6. EPM5130 Dedicated Pin-Outs

Dedicated Pin	84-Pin J-Lead	100-Pin PGA	100-Pin QFP
INPUT/CLK	1	C7	16
INPUT	2, 5, 6, 7, 36, 37, 38, 41, 42, 43, 44, 47, 48, 49, 78, 79, 80, 83, 84	A5, A7, A8, A9, A10, B5, B7, B9, C6, L7, L8, M5, M7, M9, N4, N5, N6, N7, N9	9, 10, 11, 14, 15, 16, 17, 20, 21, 22, 59, 60, 61, 64, 65, 66, 67, 70, 71, 72
GND	19, 20, 39, 40, 61, 62, 81, 82	B8, C8, F2, F3, H11, H12, L6, M6	12, 13, 37, 38, 62, 63, 87, 88
VCC	3, 4, 23, 24, 45, 46, 65, 66	A6, B6, F12, F13, H1, H2, M8, N8	18, 19, 43, 44, 68, 69, 93, 94

Table 7. EPM5130 I/O Pin-Outs (Part 1 of 2)

MC	LAB	84-Pin J-Lead	100-Pin PGA	100-Pin QFP	MC	LAB	84-Pin J-Lead	100-Pin PGA	100-Pin QFP
1	A	8	B13	1	17	B	14	A4	23
2	A	9	C12	2	18	B	15	B4	24
3	A	10	A13	3	19	B	16	A3	25
4	A	11	B12	4	20	B	17	A2	26
5	A	12	A12	5	21	B	18	B3	27
6	A	13	B11	6	22	B	21	A1	28
7	A	–	A11	7	23	B	–	B2	29
8	A	–	B10	8	24	B	–	B1	30
9	A	–	–	–	25	B	–	–	–
10	A	–	–	–	26	B	–	–	–
11	A	–	–	–	27	B	–	–	–
12	A	–	–	–	28	B	–	–	–
13	A	–	–	–	29	B	–	–	–
14	A	–	–	–	30	B	–	–	–
15	A	–	–	–	31	B	–	–	–
16	A	–	–	–	32	B	–	–	–
33	C	22	C2	31	49	D	30	G3	41
34	C	25	C1	32	50	D	31	G1	42
35	C	26	D2	33	51	D	32	H3	45
36	C	27	D1	34	52	D	33	J1	46
37	C	28	E2	35	53	D	34	J2	47
38	C	29	E1	36	54	D	35	K1	48
39	C	–	F1	39	55	D	–	K2	49
40	C	–	G2	40	56	D	–	L1	50
41	C	–	–	–	57	D	–	–	–
42	C	–	–	–	58	D	–	–	–
43	C	–	–	–	59	D	–	–	–
44	C	–	–	–	60	D	–	–	–
45	C	–	–	–	61	D	–	–	–
46	C	–	–	–	62	D	–	–	–
47	C	–	–	–	63	D	–	–	–
48	C	–	–	–	64	D	–	–	–

Table 7. EPM5130 I/O Pin-Outs (Part 2 of 2)

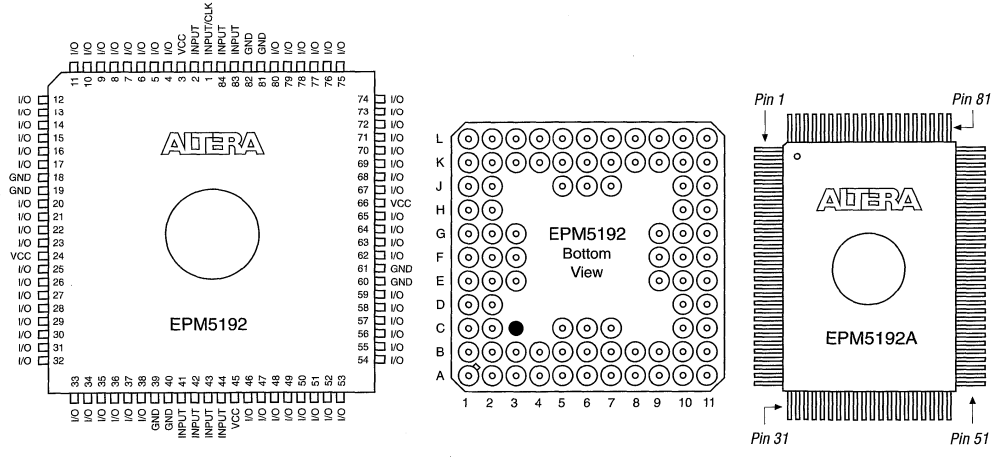
MC	LAB	84-Pin J-Lead	100-Pin PGA	100-Pin QFP	MC	LAB	84-Pin J-Lead	100-Pin PGA	100-Pin QFP
65	E	50	M1	51	81	F	56	N10	73
66	E	51	L2	52	82	F	57	M10	74
67	E	52	N1	53	83	F	58	N11	75
68	E	53	M2	54	84	F	59	N12	76
69	E	54	N2	55	85	F	60	M11	77
70	E	55	M3	56	86	F	63	N13	78
71	E	–	N3	57	87	F	–	M12	79
72	E	–	M4	58	88	F	–	M13	80
73	E	–	–	–	89	F	–	–	–
74	E	–	–	–	90	F	–	–	–
75	E	–	–	–	91	F	–	–	–
76	E	–	–	–	92	F	–	–	–
77	E	–	–	–	93	F	–	–	–
78	E	–	–	–	94	F	–	–	–
79	E	–	–	–	95	F	–	–	–
80	E	–	–	–	96	F	–	–	–
97	G	64	L12	81	113	H	72	G11	91
98	G	67	L13	82	114	H	73	G13	92
99	G	68	K12	83	115	H	74	F11	95
100	G	69	K13	84	116	H	75	E13	96
101	G	70	J12	85	117	H	76	E12	97
102	G	71	J13	86	118	H	77	D13	98
103	G	–	H13	89	119	H	–	D12	99
104	G	–	G12	90	120	H	–	C13	100
105	G	–	–	–	121	H	–	–	–
106	G	–	–	–	122	H	–	–	–
107	G	–	–	–	123	H	–	–	–
108	G	–	–	–	124	H	–	–	–
109	G	–	–	–	125	H	–	–	–
110	G	–	–	–	126	H	–	–	–
111	G	–	–	–	127	H	–	–	–
112	G	–	–	–	128	H	–	–	–

Features

- High-density, 192 macrocell, general-purpose MAX 5000 EPLD, easily integrating complete logic boards into a single package
- High-speed multi-LAB architecture
  - t_{PD} as fast as 15 ns
  - Counter frequencies up to 83.3 MHz
  - Pipelined data rates up to 100 MHz
- 384 shareable expander product terms ("expanders") offering flexibility for register and combinatorial logic expansion
- Programmable I/O architecture allowing up to 72 inputs or 64 outputs, and I/O tri-state buffers that facilitate connections to system buses
- Available in 84-pin windowed ceramic and plastic one-time-programmable (OTP) packages (see Figure 20):
  - 84-pin J-lead chip carrier (JLCC and PLCC)
  - 84-pin ceramic pin-grid array
  - 100-pin plastic quad flat pack (EPM5192A only)
- Military devices available. For information, refer to the *Military Products Data Sheet* in this data book.

Figure 20. EPM5192 Package Pin-Out Diagrams

Package outlines not drawn to scale. See Tables 8 and 9 in this data sheet for pin-out information. Windows in ceramic packages only.



84-Pin J-Lead | 84-Pin PGA | 100-Pin QFP

General Description

Altera EPM5192 EPLDs are user-configurable, high-performance MAX 5000 EPLDs that provide high-density replacements for 74-series SSI, MSI TTL, and CMOS logic. They can replace over 100 TTL SSI and MSI components and integrate the logic of over 20 22V10 devices. The EPM5192 consists of 192 macrocells equally divided into 12 Logic Array Blocks (LABs), each with 16 macrocells and 32 expanders. These compact LABs maintain high performance and efficient use of device resources. Each of these devices have 8 dedicated input pins, one of which can be used as a global Clock. They can mix global and array clocking, facilitating easy integration of multiple subsystems. The EPM5192 contains 64 I/O pins that can be configured for input, output, or bidirectional operation, providing an interface for high-speed, bus-oriented applications. See Figure 21.

Figure 21. EPM5192 Block Diagram

Numbers without parentheses are for J-lead packages. Numbers in parentheses are for PGA packages. Numbers in brackets are for EPM5192A QFP packages.

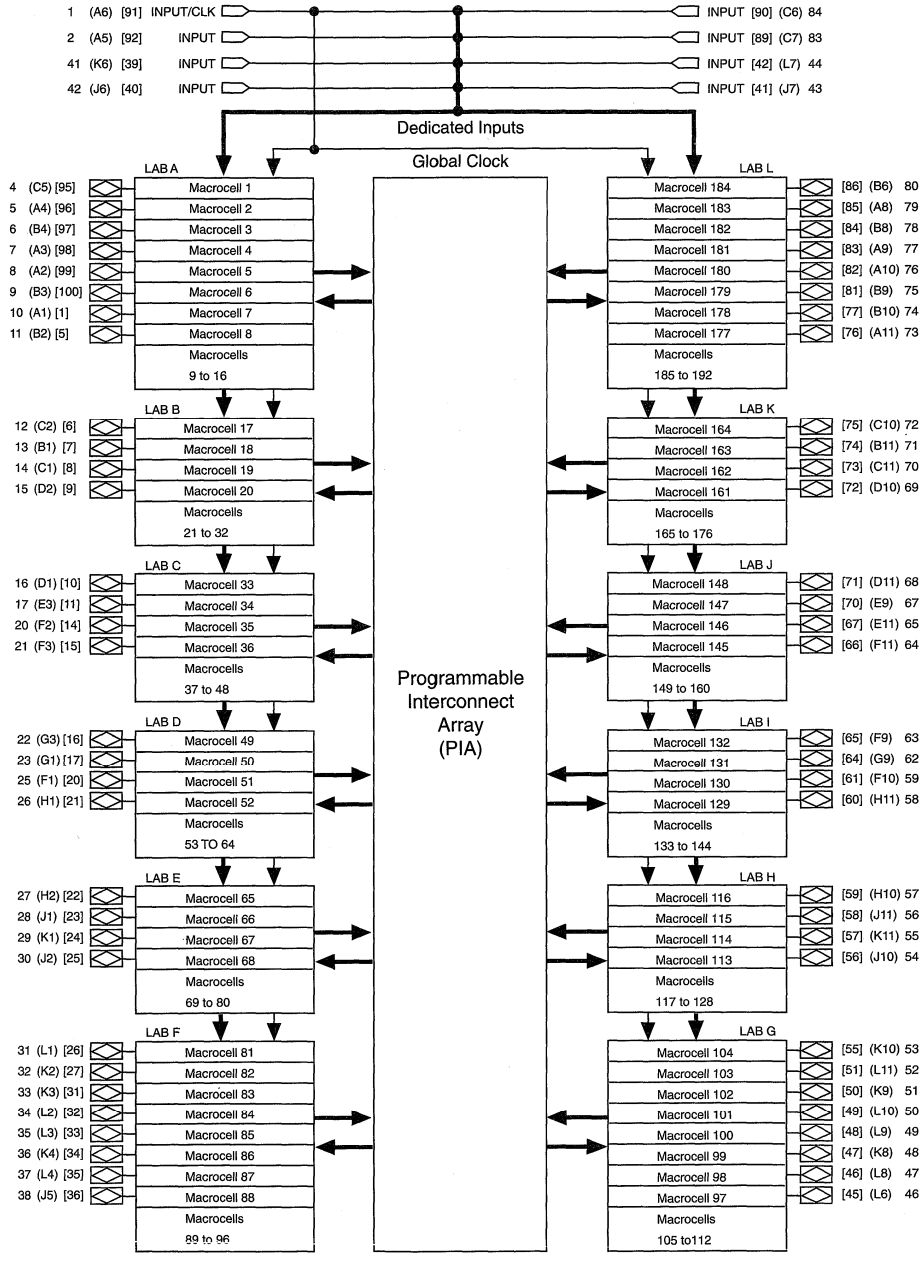
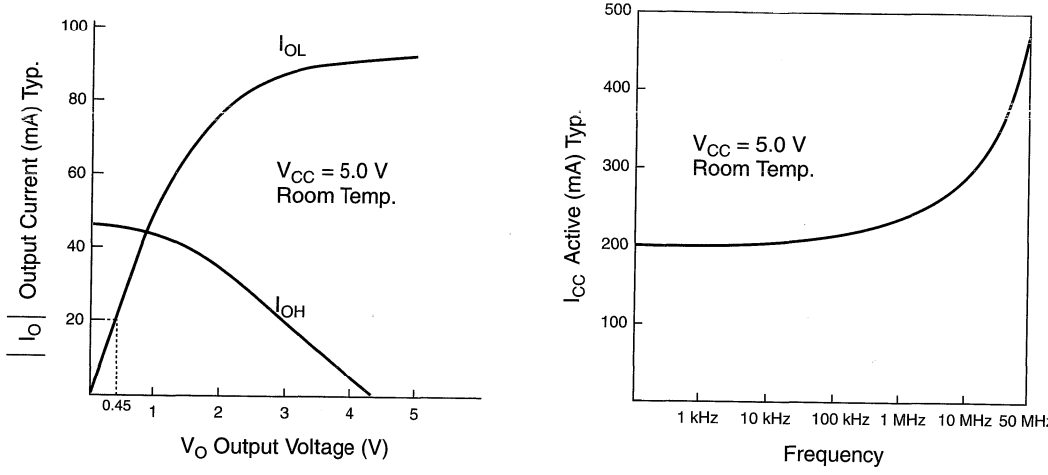


Figure 22 shows the output drive characteristics of EPM5192 I/O pins and typical supply current (I_{CC}) versus frequency.

Figure 22. Typical Output Drive Characteristics & I_{CC} vs. Frequency



Absolute Maximum Ratings

See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*Note (1)*	–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			500	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			2500	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias, *Note (2)*	–65 [–55]	135 [125]	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	*Notes (3), (4)*	4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			100	ns
t_F	Input fall time			100	ns

DC Operating Conditions

Notes (5), (6)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage	*Note (2)*	2.0 [2.2]		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND, *Notes (3), (7)*		250	360 (435)	mA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, no load, f = 1.0 MHz, *Notes (3), (7)*		270	380 (480)	mA

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{IO}	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF

AC Operating Conditions *Note (6)*

External Timing Parameters			EPM5192A-15		EPM5192A-20		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		15		20	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		25		33	ns
t_{SU}	Global clock setup time		10		13		ns
t_{H}	Global clock hold time		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		8		9	ns
t_{CH}	Global clock high time		5		7		ns
t_{CL}	Global clock low time		5		7		ns
t_{ASU}	Array clock setup time		5		6		ns
t_{AH}	Array clock hold time		5		6		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		15		20	ns
t_{ACH}	Array clock high time		5		7		ns
t_{ACL}	Array clock low time		5		7		ns
t_{CNT}	Minimum global clock period			12		15	ns
f_{CNT}	Max. internal global clock frequency	*Note (7)*	83.3		66.7		MHz
t_{ACNT}	Minimum array clock period			12		15	ns
f_{ACNT}	Max. internal array clock frequency	*Note (7)*	83.3		66.7		MHz
f_{MAX}	Maximum clock frequency	*Note (9)*	100.0		71.4		MHz

Internal Timing Parameters *Note (10)*			EPM5192A-15		EPM5192A-20		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			3		4	ns
t_{IO}	I/O input pad and buffer delay			3		4	ns
t_{SEXP}	Expander array delay			8		10	ns
t_{LAD}	Logic array delay			8		12	ns
t_{LAC}	Logic control array delay			5		5	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		3		3	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		5		5	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		5		5	ns
t_{SU}	Register setup time		2		1		ns
t_{LATCH}	Flow-through latch delay			1		1	ns
t_{RD}	Register delay			1		1	ns
t_{COMB}	Combinatorial delay			1		1	ns
t_{H}	Register hold time		7		10		ns
t_{IC}	Array clock delay			6		8	ns
t_{ICS}	Global clock delay			0		0	ns
t_{FD}	Feedback delay			1		1	ns
t_{PRE}	Register preset time			3		3	ns
t_{CLR}	Register clear time			3		3	ns
t_{PIA}	Prog. Interconnect Array delay			10		13	ns

AC Operating Conditions *Note (6)*

External Timing Parameters			EPM5192-1		EPM5192-2		EPM5192		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		25		30		35	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		40		45		55	ns
t_{SU}	Global clock setup time		15		20		25		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		14		16		20	ns
t_{CH}	Global clock high time		8		10		12.5		ns
t_{CL}	Global clock low time		8		10		12.5		ns
t_{ASU}	Array clock setup time		5		6		10		ns
t_{AH}	Array clock hold time		6		8		10		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		25		30		35	ns
t_{ACH}	Array clock high time	*Note (8)*	11		14		16		ns
t_{ACL}	Array clock low time	*Note (8)*	9		11		14		ns
t_{CNT}	Minimum global clock period			20		25		30	ns
f_{CNT}	Max. internal global clock frequency	*Note (7)*	50		40		33.3		MHz
t_{ACNT}	Minimum array clock period			20		25		30	ns
f_{ACNT}	Max. internal array clock frequency	*Note (7)*	50		40		33.3		MHz
f_{MAX}	Maximum clock frequency	*Note (9)*	62.5		50		40		MHz

Internal Timing Parameters *Note (10)*			EPM5192-1		EPM5192-2		EPM5192		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			5		7		11	ns
t_{IO}	I/O input pad and buffer delay			6		6		11	ns
t_{SEXP}	Expander array delay			12		14		20	ns
t_{LAD}	Logic array delay			12		14		14	ns
t_{LAC}	Logic control array delay			10		12		13	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		5		5		6	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		10		11		13	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		10		11		13	ns
t_{SU}	Register setup time		6		8		12		ns
t_{LATCH}	Flow-through latch delay			3		4		4	ns
t_{RD}	Register delay			1		2		2	ns
t_{COMB}	Combinatorial delay			3		4		4	ns
t_{H}	Register hold time		4		6		8		ns
t_{IC}	Array clock delay			14		16		16	ns
t_{ICS}	Global clock delay			3		2		1	ns
t_{FD}	Feedback delay			1		1		2	ns
t_{PRE}	Register preset time			5		6		7	ns
t_{CLR}	Register clear time			5		6		7	ns
t_{PIA}	Prog. Interconnect Array delay			14		16		20	ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Numbers in brackets are for MIL-STD-883-compliant versions only.
(3) Numbers in parentheses are for military- and industrial-temperature-range versions, as well as for MIL-STD-883-compliant versions.
(4) Maximum V_{CC} rise time for the EPM5192/EPM5192A is 200 ms.
(5) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(6) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C for military use.
(7) Measured with a 16-bit counter programmed into each LAB. I_{CC} measured at 0° C.
(8) This parameter is measured with a positive-edge-triggered Clock at the register. For negative-edge clocking, the t_{ACH} and t_{ACL} parameters must be swapped.
(9) The f_{MAX} values represent the highest frequency for pipelined data.
(10) For information on internal timing parameters, refer to *Application Brief 100 (Understanding Classic, MAX 5000 & MAX 7000 Timing)* in this data book.

Pin-Out Information

Tables 8 and 9 provide pin-out information for the EPM5192.

Table 8. EPM5192 Dedicated Pin-Outs

Dedicated Pin	84-Pin J-Lead	84-Pin PGA	100-Pin QFP
INPUT/CLK	1	A6	91
INPUT	2, 41, 42, 43, 44, 83, 84	A5, K6, J6, J7, L7, C7, C6	39, 40, 41, 42
GND	18, 19, 39, 40, 60, 61, 81, 82	A7, B7, E1, E2, G10, G11, K5, L5	2, 3, 4, 12, 13, 28, 29, 30, 37, 38, 52, 53, 54, 62, 63, 78, 79, 80, 87, 88
VCC	3, 24, 45, 66	B5, E10, G2, K7	18, 44, 68, 69, 93, 94

Table 9. EPM5192 I/O Pin-Outs (Part 1 of 3)

MC	LAB	84-Pin J-Lead	84-Pin PGA	100-Pin QFP	MC	LAB	84-Pin J-Lead	84-Pin PGA	100-Pin QFP
1	A	4	C5	95	17	B	12	C2	6
2	A	5	A4	96	18	B	13	B1	7
3	A	6	B4	97	19	B	14	C1	8
4	A	7	A3	98	20	B	15	D2	9
5	A	8	A2	99	21	B	–	–	–
6	A	9	B3	100	22	B	–	–	–
7	A	10	A1	1	23	B	–	–	–
8	A	11	B2	5	24	B	–	–	–
9	A	–	–	–	25	B	–	–	–
10	A	–	–	–	26	B	–	–	–
11	A	–	–	–	27	B	–	–	–
12	A	–	–	–	28	B	–	–	–
13	A	–	–	–	29	B	–	–	–
14	A	–	–	–	30	B	–	–	–
15	A	–	–	–	31	B	–	–	–
16	A	–	–	–	32	B	–	–	–
33	C	16	D1	10	49	D	22	G3	16
34	C	17	E3	11	50	D	23	G1	17
35	C	20	F2	14	51	D	25	F1	20
36	C	21	F3	15	52	D	26	H1	21
37	C	–	–	–	53	D	–	–	–
38	C	–	–	–	54	D	–	–	–
39	C	–	–	–	55	D	–	–	–
40	C	–	–	–	56	D	–	–	–
41	C	–	–	–	57	D	–	–	–
42	C	–	–	–	58	D	–	–	–
43	C	–	–	–	59	D	–	–	–
44	C	–	–	–	60	D	–	–	–
45	C	–	–	–	61	D	–	–	–
46	C	–	–	–	62	D	–	–	–
47	C	–	–	–	63	D	–	–	–
48	C	–	–	–	64	D	–	–	–

Table 9. EPM5192 I/O Pin-Outs (Part 2 of 3)

MC	LAB	84-Pin J-Lead	84-Pin PGA	100-Pin QFP	MC	LAB	84-Pin J-Lead	84-Pin PGA	100-Pin QFP
65	E	27	H2	22	81	F	31	L1	26
66	E	28	J1	23	82	F	32	K2	27
67	E	29	K1	24	83	F	33	K3	31
68	E	30	J2	25	84	F	34	L2	32
69	E	–	–	–	85	F	35	L3	33
70	E	–	–	–	86	F	36	K4	34
71	E	–	–	–	87	F	37	L4	35
72	E	–	–	–	88	F	38	J5	36
73	E	–	–	–	89	F	–	–	–
74	E	–	–	–	90	F	–	–	–
75	E	–	–	–	91	F	–	–	–
76	E	–	–	–	92	F	–	–	–
77	E	–	–	–	93	F	–	–	–
78	E	–	–	–	94	F	–	–	–
79	E	–	–	–	95	F	–	–	–
80	E	–	–	–	96	F	–	–	–
97	G	46	L6	45	113	H	54	J10	56
98	G	47	L8	46	114	H	55	K11	57
99	G	48	K8	47	115	H	56	J11	58
100	G	49	L9	48	116	H	57	H10	59
101	G	50	L10	49	117	H	–	–	–
102	G	51	K9	50	118	H	–	–	–
103	G	52	L11	51	119	H	–	–	–
104	G	53	K10	55	120	H	–	–	–
105	G	–	–	–	121	H	–	–	–
106	G	–	–	–	122	H	–	–	–
107	G	–	–	–	123	H	–	–	–
108	G	–	–	–	124	H	–	–	–
109	G	–	–	–	125	H	–	–	–
110	G	–	–	–	126	H	–	–	–
111	G	–	–	–	127	H	–	–	–
112	G	–	–	–	128	H	–	–	–

Table 9. EPM5192 I/O Pin-Outs (Part 3 of 3)

MC	LAB	84-Pin J-Lead	84-Pin PGA	100-Pin QFP	MC	LAB	84-Pin J-Lead	84-Pin PGA	100-Pin QFP
129	I	58	H11	60	145	J	64	F11	66
130	I	59	F10	61	146	J	65	E11	67
131	I	62	G9	64	147	J	67	E9	70
132	I	63	F9	65	148	J	68	D11	71
133	I	–	–	–	149	J	–	–	–
134	I	–	–	–	150	J	–	–	–
135	I	–	–	–	151	J	–	–	–
136	I	–	–	–	152	J	–	–	–
137	I	–	–	–	153	J	–	–	–
138	I	–	–	–	154	J	–	–	–
139	I	–	–	–	155	J	–	–	–
140	I	–	–	–	156	J	–	–	–
141	I	–	–	–	157	J	–	–	–
142	I	–	–	–	158	J	–	–	–
143	I	–	–	–	159	J	–	–	–
144	I	–	–	–	160	J	–	–	–
161	K	69	D10	72	177	L	73	A11	76
162	K	70	C11	73	178	L	74	B10	77
163	K	71	B11	74	179	L	75	B9	81
164	K	72	C10	75	180	L	76	A10	82
165	K	–	–	–	181	L	77	A9	83
166	K	–	–	–	182	L	78	B8	84
167	K	–	–	–	183	L	79	A8	85
168	K	–	–	–	184	L	80	B6	86
169	K	–	–	–	185	L	–	–	–
170	K	–	–	–	186	L	–	–	–
171	K	–	–	–	187	L	–	–	–
172	K	–	–	–	188	L	–	–	–
173	K	–	–	–	189	L	–	–	–
174	K	–	–	–	190	L	–	–	–
175	K	–	–	–	191	L	–	–	–
176	K	–	–	–	192	L	–	–	–

Notes:

March 1995

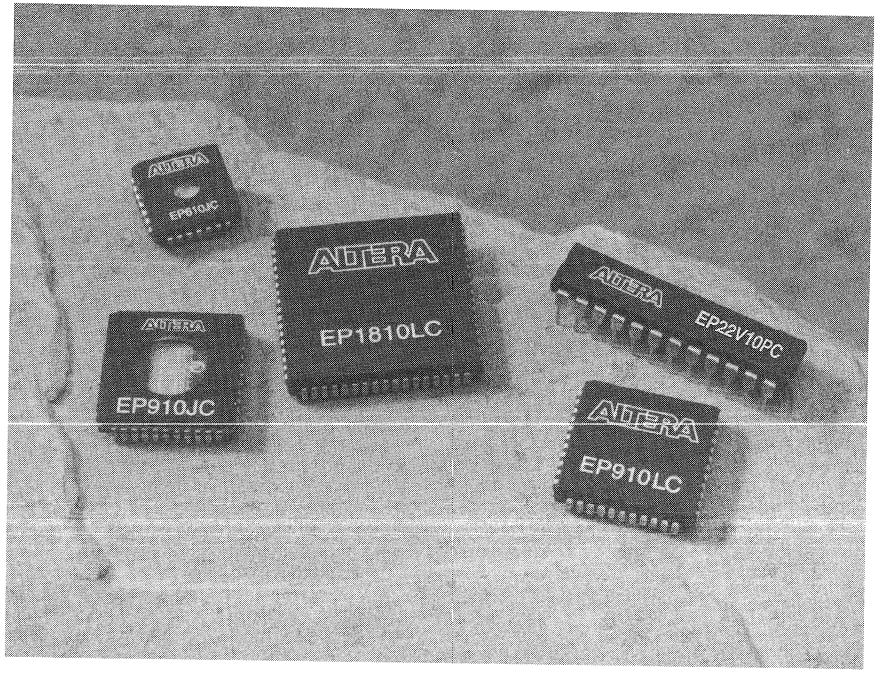
Classic EPLD Family

EP610 EPLD

EP910 EPLD

EP1810 EPLD

EP22V10 EPLD


ALTERA
EP910JC
ALTERA
EP1810LC
ALTERA
EP22V10PC
ALTERA
EP910JC
ALTERA
EP910LC

Classic
EPLD Family

March 1995, ver. 2 — Data Sheet

Features

- Complete device family with logic densities of up to 1,800 available gates (900 usable gates), see Table 1
- Device erasure and reprogramming with advanced, non-volatile EPROM configuration elements
- Fast pin-to-pin logic delays as low as 7.5 ns and internal counter frequencies as high as 111.1 MHz
- 24 to 68 pins available in DIP, J-lead, PGA, SOIC, and one-time-programmable (OTP) packages
- Programmable Security Bit for total protection of proprietary designs
- 100% generically testable to provide 100% programming yield
- Programmable registers providing D, T, JK, and SR flipflops with individual Clear and Clock controls
- Software design support featuring: Altera's MAX+PLUS II development system on 486- and Pentium-based PCs, and Sun SPARCstation, HP 9000 Series 700, and IBM RISC System/6000 workstations; Altera's PLDshell Plus software; and third-party development systems
- Programming support with Altera's Master Programming Unit (MPU); programming hardware from Data I/O and others
- Additional design entry and simulation support provided by EDIF, Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Data I/O, Exemplar, Intergraph, Mentor Graphics, OrCAD, Synopsys, and Viewlogic

Table 1. Classic Device Features

Feature	EP22V10 EP22V10E	EP610 EP610T	EP610I	EP910 EP910T	EP910I	EP1810 EP1810T
Available gates	400	600	600	900	900	1,800
Usable gates	200	300	300	450	450	900
Macrocells	10	16	16	24	24	48
Maximum user I/O pins	22	20	20	36	36	64
t_{PD} (ns) *Note (1)*	7.5	15 (35)	10	30	12	20 (45)
f_{CNT} (MHz) *Note (1)*	111.1	83.3 (28.6)	100	33.3	100	50 (22.2)

Note:
(1) Numbers in parentheses are for MIL-STD-883-compliant versions of the EP610 and EP1810. For more information, refer to "EP610 EPLDs" and "EP1810 EPLDs" in this data sheet, or the *Military Products Data Sheet* in this data book.

General Description

The Altera Classic device family offers the industry's most comprehensive solution to high-speed, low-power logic integration. Fabricated on advanced CMOS technology, Classic devices also have turbo-only and military versions, all of which are described in this data sheet.

Classic devices support 100% TTL emulation and can easily integrate multiple PAL- and GAL-type devices with densities ranging from 200 to 900 usable gates. The Classic family provides pin-to-pin logic delays as low as 7.5 ns and counter frequencies as high as 111.1 MHz. Classic devices are available in a wide range of packages, including ceramic and plastic dual in-line (CerDIP and PDIP), ceramic and plastic J-lead chip carrier (JLCC and PLCC), ceramic pin-grid array (PGA), and plastic small-outline integrated circuit (SOIC) packages.

Unlike equivalent bipolar devices, the EPROM-based Classic devices can reduce active power consumption without sacrificing performance. This reduced power consumption makes the Classic family well suited for a wide range of low-power applications. Classic devices are 100% generically tested and are easily erased with ultraviolet light. Designs and design changes can be implemented quickly, eliminating the need for post-programming testing.

EP610, EP910 & EP1810 Devices

EP610, EP910, and EP1810 devices use sum-of-products logic and a programmable register. The sum-of-products logic provides a programmable-AND/fixed-OR structure that can implement logic with up to eight product terms. The programmable register can be individually programmed for D, T, SR, or JK flipflop operation or can be bypassed for combinatorial operation. In addition, macrocell registers can be individually clocked either by a global Clock or by any input or feedback path to the AND array. Altera's proprietary programmable I/O architecture allows the designer to program output and feedback paths for combinatorial or registered operation in both active-high and active-low modes. These features make it possible to simultaneously implement a variety of logic functions.

The EP610, EP910, and EP1810 devices are supported by Altera's MAX+PLUS II development system, a single, integrated package that offers schematic, text—including the Altera Hardware Description Language (AHDL)—and waveform design entry; compilation and logic synthesis; simulation and timing analysis; and device programming. MAX+PLUS II provides EDIF 2 0 0 and 3 0 0, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and workstation-based EDA tools. MAX+PLUS II runs on 486- and Pentium-based PCs, and Sun SPARCstation, HP 9000 Series 700, and IBM RISC System/6000 workstations.

For more information, go to the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* in this data book.

In addition to the basic EP610, EP910, and EP1810 devices, Altera provides the following versions:

- Lower cost "T" devices
- "I" devices
- MIL-STD-883-compliant devices

Lower Cost "T" Devices

Altera offers Classic devices—EP610T, EP910T, and EP1810T—in which the Turbo Bit is permanently turned on (designated by a "T" suffix in the ordering code). These devices are available in plastic one-time-programmable (OTP) packages and provide a low-cost, high-speed solution for logic designs. They are completely pin-, function-, and programming file-compatible with their non-turbo counterparts. "T" devices do not have a non-turbo mode.

"I" Devices

The EP610 and EP910 devices acquired from Intel are designated by an "I" suffix in the ordering code. These devices are available in both windowed ceramic and OTP packages, and are pin-, function-, and programming file-compatible with other Classic devices.

MIL-STD-883-Compliant Devices

Altera MIL-STD-883-compliant devices—EP610 MIL-STD-compliant and EP1810 MIL-STD-compliant—comply with the military standard operating requirements listed in MIL-STD-883. For more information, see the *Military Products Data Sheet* in this data book or contact Altera Marketing at (408) 894-7104.

EP22V10 Devices

EP22V10 devices use industry-standard 22V10 architecture, and offer superior speeds at low power: the EP22V10-7 has a t_{PD} of 7.5 ns with a typical I_{CC} of 90 mA at 15 MHz; and the EP22V10E has an enhanced macrocell with an optional inverted Clock and additional feedback. EP22V10 devices are JEDEC File-compatible with the industry-standard 22V10 architecture.

EP22V10 devices are supported by industry-standard PC- and workstation-based EDA tools, including the Altera PLDshell Plus development system. For more information on PLDshell Plus, refer to the ***PLDshell Plus/PLDasm User's Guide.***

Go to "EP22V10 Devices" on page 377 for a functional description of EP22V10 devices.

Design Security

Classic devices contain a programmable Security Bit that controls access to the data programmed into the device. When this bit is programmed, a proprietary design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security, since data within EPROM configuration elements is invisible. The Security Bit that controls this function and other program data is reset when a device is erased.

Turbo Bit

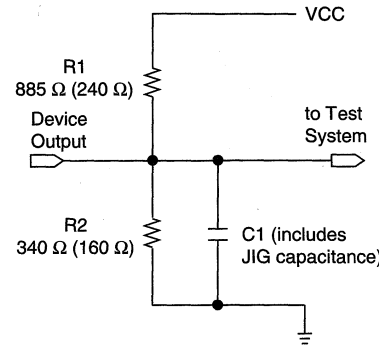
Many Classic devices contain a programmable Turbo Bit to control the automatic power-down feature that enables the low-standby-power mode (I_{CC1}). When the Turbo Bit is turned on, the low-standby-power mode is disabled. All AC values are tested with the Turbo Bit turned on. When the device is operating with the Turbo Bit turned off (non-turbo mode), a non-turbo adder must be added to the appropriate AC parameter to determine worst-case timing. The non-turbo adder is specified in the "AC Operating Conditions" tables for each Classic device that supports the turbo mode.

Generic Testing

Classic devices are fully functionally tested and guaranteed. Complete testing of each programmable EPROM configuration element and all internal logic elements ensures 100% programming yield. See Figure 1 for AC test measurement conditions.

Figure 1. AC Test Conditions

Power-supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in parentheses are for EP22V10 devices.



EPROM-based devices in one-time-programmable, windowless packages also contain on-board logic test circuitry to allow verification of function and AC specifications during standard production flow.

Device Programming

Classic devices, except EP22V10 devices, can be programmed on 486- and Pentium-based PCs with an Altera Logic Programmer card, the Master Programming Unit (MPU), and the appropriate device adapter. The MPU performs continuity checking to ensure adequate electrical contact between the adapter and the device.

Data I/O and other programming hardware manufacturers also offer programming support for Altera devices. See *Programming Hardware Manufacturers* in this data book for more information.

Functional Description

The EP610, EP910, and EP1810 architecture includes the following elements:

- Macrocells
- Programmable registers
- Output Enable/Clock select
- Feedback selection

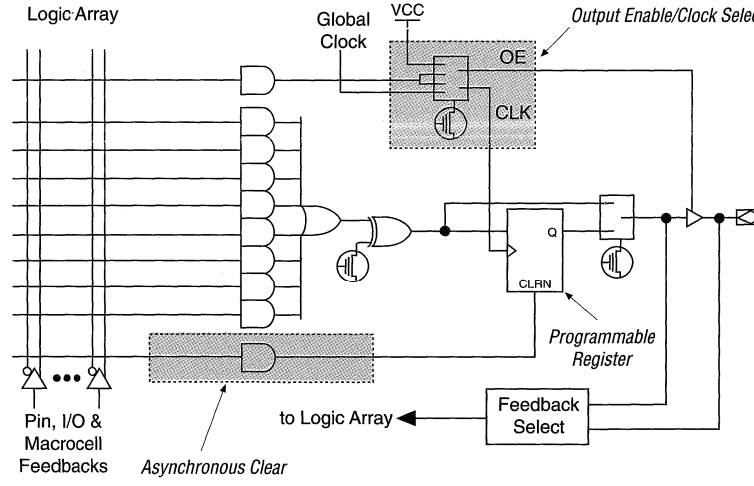
Go to "EP22V10 EPLDs" on page 377 for a complete description of the EP22V10 architecture.

Macrocells

EP610, EP910, and EP1810 macrocells, shown in Figure 2, can be individually configured for both sequential and combinatorial logic operation. Eight product terms form a programmable-AND array that feeds an OR gate for combinatorial logic implementation. An additional product term is used for asynchronous Clear control of the internal register; another product term implements either an Output Enable or a logic-array-generated Clock. Inputs to the programmable-AND array come from both the true and complement signals of the dedicated inputs; feedbacks from I/O pins that are configured as inputs; and feedbacks from macrocell outputs. Signals from dedicated inputs are globally routed and can feed the inputs of all device macrocells. The feedback multiplexer controls the routing of feedback signals from macrocells and from I/O pins configured as inputs.

Figure 2. Macrocell for EP610, EP910 & EP1810 Devices

For additional information on feedback select configurations, see Figure 4.



The eight product terms of the programmable-AND array feed the 8-input OR gate, which then feeds one input to an XOR gate. The other input to the XOR gate is connected to a programmable bit that allows the array output to be inverted. Altera's MAX+PLUS II software uses either the XOR gate to implement active-high or active-low logic, or De Morgan's inversion to reduce the number of product terms to implement a function.

Programmable Registers

To implement registered functions, each macrocell register can be individually programmed for D, T, JK, or SR operation. If necessary, the register can be bypassed for combinatorial operation. During design compilation, MAX+PLUS II selects the most efficient register operation for each registered function to minimize the logic resources needed by the design. Registers have an individual asynchronous Clear function controlled by a dedicated product term, and they are cleared automatically during power-up.

In addition, macrocell registers can be individually clocked either by a global Clock or by any input or feedback path to the AND array. Altera's proprietary programmable I/O architecture allows the designer to program output and feedback paths for combinatorial or registered operation in both active-high and active-low modes. These features make it possible to simultaneously implement a variety of logic functions.

Output Enable/Clock Select

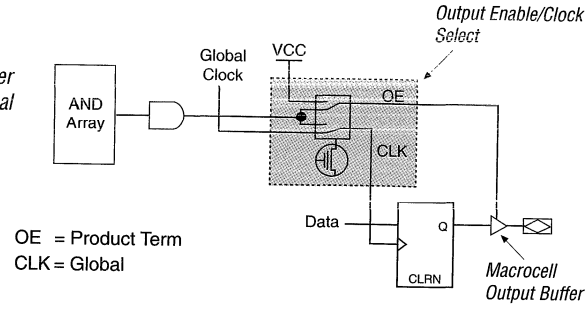
Figure 3 shows the two operating modes (Modes 0 and 1) provided by the Output Enable/Clock (OE/CLK) select. This OE/CLK select, which is controlled by a single programmable bit, can be individually configured for each macrocell. In Mode 0, the tri-state output buffer is controlled by a single product term. If the Output Enable is high, the output buffer is enabled. If the Output Enable is low, the output has a high-impedance value. In this mode, the macrocell flipflop is clocked by its global Clock input signal.

In Mode 1, the Output Enable buffer is always enabled, and the macrocell register can be triggered by an array Clock signal generated by a product term. This mode allows registers to be individually clocked by any signal on the AND array. With both true and complement signals in the AND array, the register can be configured to trigger on a rising or falling edge. This product-term-controlled Clock configuration also supports gated Clock structures.

Figure 3. Output Enable/Clock Select

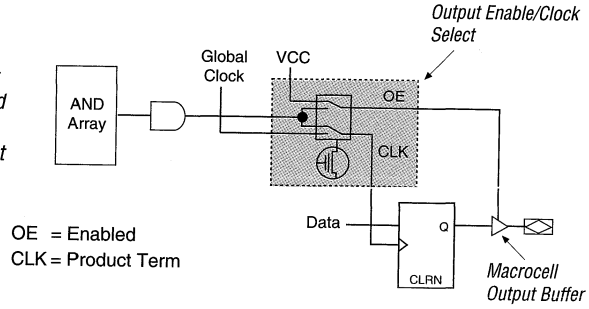
Mode 0

In Mode 0, the register is clocked by the global Clock signal. The output is enabled by the logic from the product term.



Mode 1

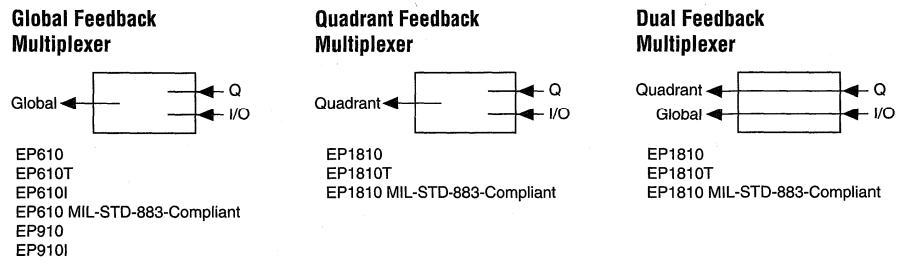
In Mode 1, the output is permanently enabled and the register is clocked by the product term, which allows gated Clocks to be generated.



Feedback Selection

Each macrocell in a Classic device provides feedback selection that is controlled by the feedback multiplexer. This feedback selection allows the user to feed either the macrocell output or the I/O pin input associated with the macrocell back into the AND array. The macrocell output can be either the Q output of the programmable register or the combinatorial output of the macrocell. Different devices have different feedback multiplexer configurations. See Figure 4.

Figure 4. Feedback Multiplexer Configurations



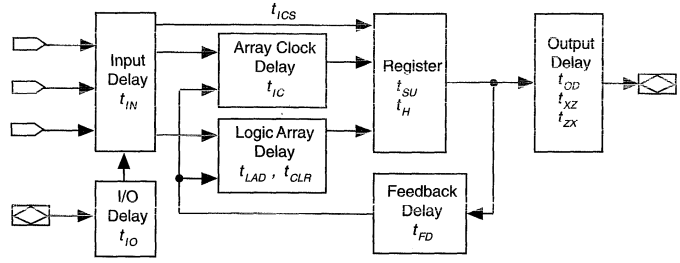
EP610, EP610I, EP910, and EP910I devices have a global feedback configuration; either the macrocell output (Q) or the I/O pin input (I/O) can feed back to the AND array so that it is accessible to all other macrocells.

EP1810 macrocells can have either of two feedback configurations: quadrant and dual. Most macrocells in EP1810 devices have a quadrant feedback configuration; either the macrocell output or I/O pin input can feed back to other macrocells in the same quadrant. Selected macrocells in EP1810 devices have a dual feedback configuration: the output of the macrocell feeds back to other macrocells in the same quadrant, and the I/O pin input feeds back to all macrocells in the device. If the associated I/O pin is not used, the macrocell output can optionally feed all macrocells in the device. In this case, the output of the macrocell passes through the tri-state buffer and uses the feedback path between the buffer and the I/O pin.

Timing Model

Device timing can be analyzed with the MAX+PLUS II software, with a variety of popular industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 5. Devices have fixed internal delays that allow the user to determine the worst-case timing for any design. The MAX+PLUS II software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for system-level performance evaluation.

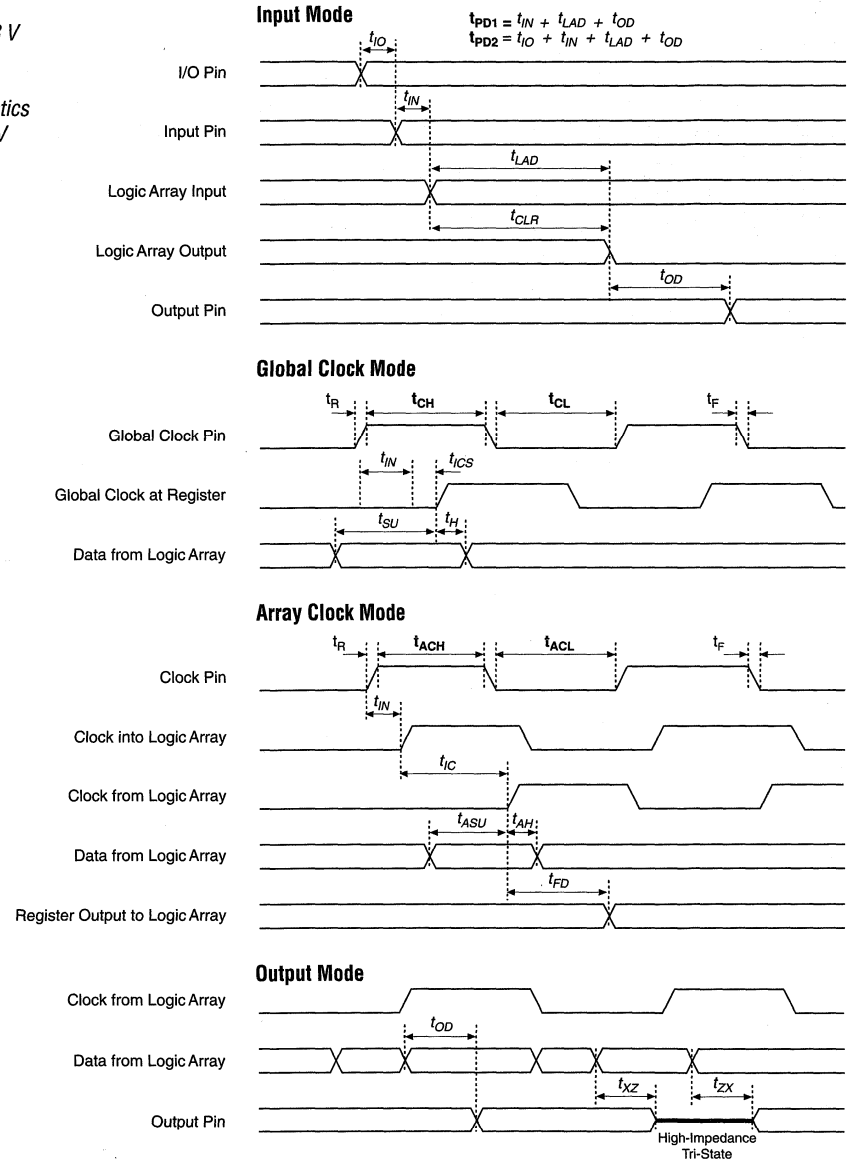
Figure 5. Timing Model



Timing information can be derived from the timing model and parameters for a particular device. External timing parameters represent pin-to-pin timing delays, and can be calculated from the sum of internal parameters. Figure 6 shows the internal timing relationship for internal and external delay parameters. For more information on device timing, refer to *Application Brief 100 (Understanding Classic, MAX 5000 & MAX 7000 Timing)* in this data book.

Figure 6. Switching Waveforms

t_R & t_F < 3 ns.
Inputs are driven at 3 V for a logic high and 0 V for a logic low.
All timing characteristics are measured at 1.5 V



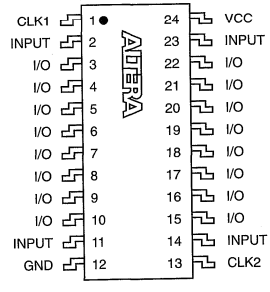
Notes:

Features

- High-performance, 16-macrocell Classic EPLD
  - Combinatorial speeds with t_{PD} as low as 10 ns
  - Counter frequencies of up to 100 MHz
  - Pipelined data rates of up to 100 MHz
- Programmable I/O architecture with up to 20 inputs or 16 outputs and 2 Clock pins
- The following devices are pin-, function-, and programming file-compatible: EP610, EP610I, EP610T, EP610 MIL-STD-883-compliant, EP600I, and PALCE610
- Programmable Clock option for independent clocking of all registers
- Macrocells individually programmable as D, T, JK, or SR flipflops, or for combinatorial operation
- Available in windowed ceramic and one-time-programmable (OTP) plastic packages (see Figure 7):
  - 24-pin small-outline integrated circuit (plastic SOIC only)
  - 24-pin dual in-line package (CerDIP and PDIP)
  - 28-pin plastic J-lead chip carrier (PLCC)

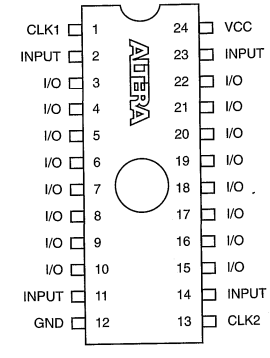
Figure 7. EP610 Package Pin-Out Diagrams

Package outlines not drawn to scale. Windows in ceramic packages only.



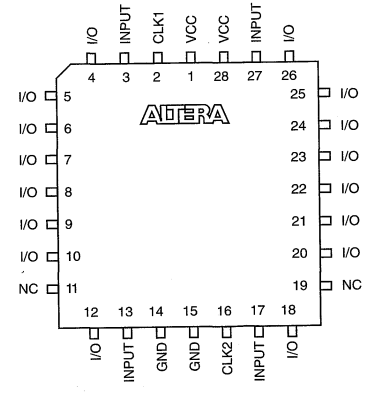
24-Pin SOIC

EP610
EP610T



24-Pin DIP

EP610
EP610T
EP610 MIL-STD-883-Compliant
EP610I



28-Pin J-Lead

EP610
EP610T
EP610I

Table 2 summarizes EP610 device features.

Table 2. EP610 Device Features

Feature	EP610	EP610T	EP610 MIL-STD-883-Compliant	EP610I
t_{PD}	15 ns	15 ns	35 ns	10 ns
Counter frequency	83 MHz	83 MHz	28.5 MHz	100 MHz
Pipeline data rates	83 MHz	83 MHz	37 MHz	100 MHz
Packages	24-pin SOIC 24-pin CerDIP 24-pin PDIP 28-pin PLCC	24-pin SOIC 24-pin PDIP 28-pin PLCC	24-pin CerDIP	24-pin CerDIP 24-pin PDIP 28-pin PLCC

General Description

EP610 devices have 16 macrocells, 4 dedicated input pins, 16 I/O pins, and 2 global Clock pins (see Figure 8). Each macrocell can access signals from the global bus, which consists of the true and complement forms of the dedicated inputs and the true and complement forms of either the output of the macrocell or the I/O input. CLK1 is a dedicated Clock input for the registers in macrocells 9 through 16. CLK2 is a dedicated Clock input for registers in macrocells 1 through 8.

Figure 8. EP610 Block Diagram

Numbers without parentheses are for DIP and SOIC packages. Numbers in parentheses are for J-lead packages.

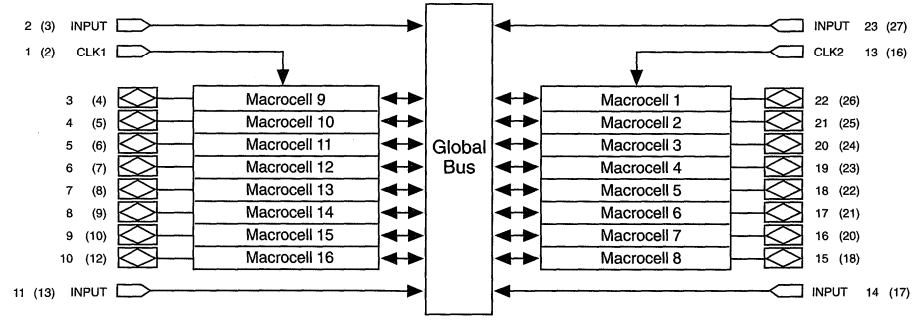
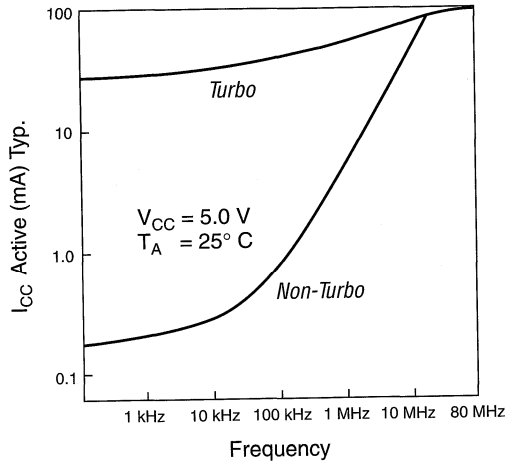


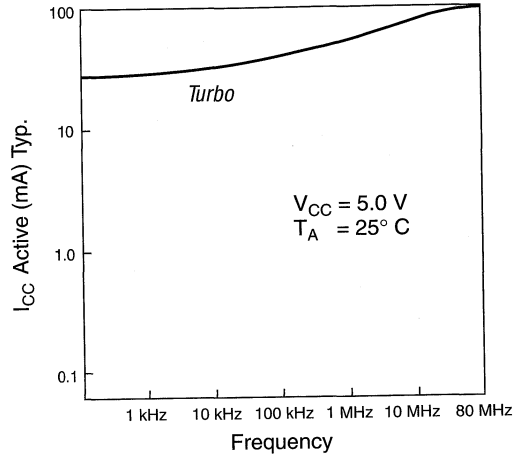
Figure 9 shows the typical supply current (I_{CC}) versus frequency for EP610 devices.

Figure 9. EP610 I_{CC} vs. Frequency

EP610 & EP610 MIL-STD-883-Compliant EPLDs



EP610T EPLDs

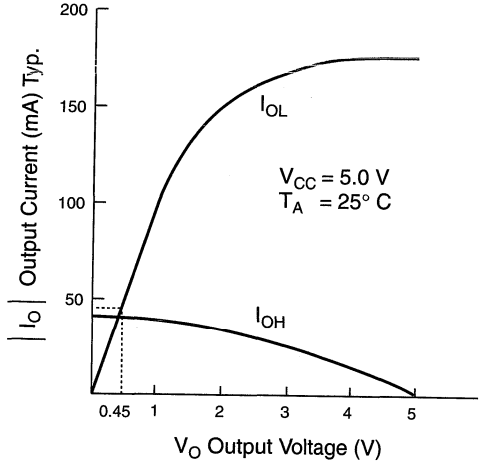


8 Classic

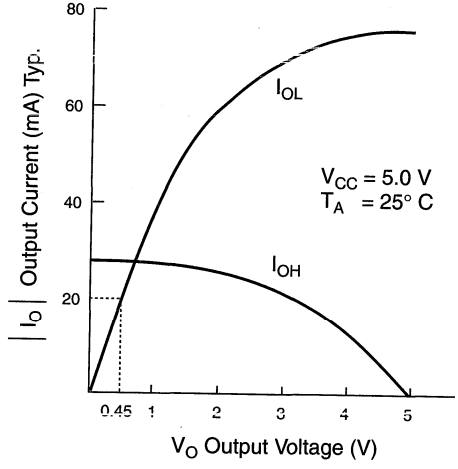
Figure 10 shows the maximum output drive characteristics of EP610 I/O pins.

Figure 10. EP610 Output Drive Characteristics

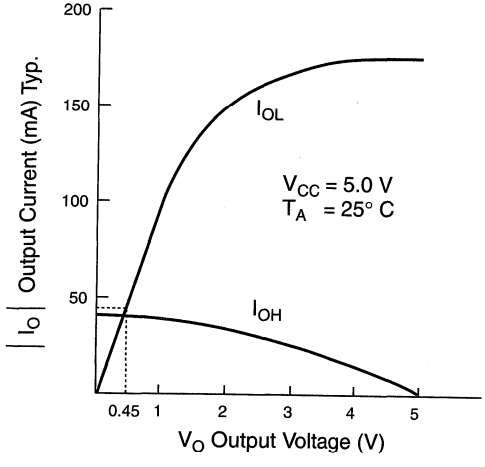
EP610-15 & EP610-20 EPLDs



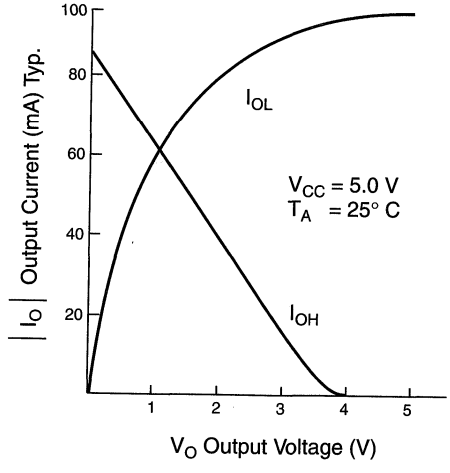
EP610-25, EP610-25T, EP610-30 & EP610-35



EP610-15T & EP610-20T EPLDs



EP610I EPLDs



Absolute Maximum Ratings *Note (1)*

			EP610 EP610T EP610 MIL-STD-883-Compliant		EP610I		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
V_{CC}	Supply voltage	With respect to GND, *Note (2)*	–2.0	7.0	–2.0	7.0	V
V_I	DC input voltage		–2.0	7.0	–0.5	V_{CC}+ 0.5	V
I_{MAX}	DC V_{CC} or GND current		–175	175			mA
I_{OUT}	DC output current, per pin		–25	25			mA
P_D	Power dissipation			1,000			mW
T_{STG}	Storage temperature	No bias	–65	150	–65	150	° C
T_{AMB}	Ambient temperature	Under bias, *Note (3)*	–65	135 (125)	–10	85	° C
T_J	Junction temperature	Under bias, *Note (3)*		(150)			° C

Recommended Operating Conditions *Note (4)*

			EP610 EP610T EP610 MIL-STD-883-Compliant		EP610I		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
V_{CC}	Supply voltage	*Notes (3), (5)*	4.75 (4.5)	5.25 (5.5)	4.75	5.25	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	–40	85	° C
T_C	Case temperature	For military use	–55	125			° C
t_R	Input rise time	*Notes (3), (6)*		100 (50)		500	ns
t_F	Input fall time	*Notes (3), (6)*		100 (50)		500	ns

DC Operating Conditions *Notes (3), (4), (7)*

Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC, *Note (8)*	2.4			V
V_{OH}	High-level CMOS output voltage	I_{OH} = –2 mA DC, *Note (8)*	3.84			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC, *Note (8)*			0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	–10		10	µA
I_{OZ}	Tri-state output leakage current	V_O = V_{CC} or GND	–10		10	µA

Capacitance *Note (9)*

			EP610 EP610T		EP610 MIL-STD-883-Compliant		EP610I		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		10		20		8	pF
$C_{I/O}$	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12		20		8	pF
C_{CLK1}	CLK1 pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20		20		10	pF
C_{CLK2}	CLK2 pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20		20		12	pF

I_{CC} Supply Current: EP610 & EP610T *Note (7)*

				EP610			EP610T			
Symbol	**Parameter**	**Conditions**	**Speed Grade**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{CC1}	V_{CC} supply current (non-turbo, standby)	V_I = V_{CC} or GND, No load, *Notes (10), (11), (12)*			20	150				µA
I_{CC2}	V_{CC} supply current (non-turbo, active)	V_I = V_{CC} or GND, No load, f = 1.0 MHz, *Notes (3), (12)*			5	10 (15)				mA
I_{CC3}	V_{CC} supply current (turbo, active)	*Notes (3), (11), (12)*	-15, -20		60	90 (115)		60	90	mA
			-25, -30, -35		45	60 (75)		60	90	mA

I_{CC} Supply Current: EP610 MIL-STD-883-Compliant & EP610I *Note (7)*

			EP610 MIL-STD-883-Compliant			EP610I			
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{CC1}	V_{CC} supply current (non-turbo, standby)	V_I = V_{CC} or GND, no load, *Notes (10), (11), (12)*			900		20	150	µA
I_{CC2}	V_{CC} supply current (non-turbo, active)	V_I = V_{CC} or GND, no load, f = 1.0 MHz, *Notes (10), (12)*			25		3	8	mA
I_{CC3}	V_{CC} supply current (turbo, active)	V_I = V_{CC} or GND, no load, f = 1.0 MHz, *Notes (10), (12)*			140		65	105	mA

Notes to tables:

(1) See *Operating Requirements for Altera Devices* in this data book.
(2) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions. For EP610-15, EP610-15T, EP610-20, and EP610-20T EPLDs: maximum V_{PP} = 14.0 V.
(3) Numbers in parentheses are for military- and industrial-temperature-range versions.
(4) Operating conditions: V_{CC} = 5.0 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5.0 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5.0 V ± 10%, T_A = –55° C to 125° C for military use.
(5) For EP610, EP610T, and EP610 MIL-STD-883-compliant devices, maximum V_{CC} rise time is 50 ms. For EP610I devices, V_{CC} rise time is unlimited with monotonic rise.
(6) For EP610-15 and EP610-20 EPLDs: t_R and t_F = 40 ns.
For EP610-15 and EP610-20 Clocks: t_R and t_F = 20 ns.
(7) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(8) For EP610 MIL-STD-883-compliant, tested at maximum operating temperature only.
(9) Capacitance measured at 25° C. Sample-tested only. Clock-pin capacitance for dedicated Clock inputs only. For EP610-25, EP610-30, EP610-35, EP610-25T, and EP610 MIL-STD-833 EPLDs: Pin 13 has a maximum capacitance of 50 pF; C_{IN}, C_{OUT}, and C_{CLK} = 20 pF.
(10) When the Turbo Bit is not set (non-turbo mode), an EP610 EPLD enters standby mode if no logic transitions occur for 100 ns after the last transition.
(11) Measured with a device programmed as a 16-bit counter. I_{CC} measured at 0° C.
(12) For EP610 MIL-STD-883-compliant, tested with non-output loading using a data pattern specified by Altera. Data path is programmed as a 16-bit counter.

AC Operating Conditions: EP610-15 & EP610-20 *Notes (1), (2)*

			EP610-15 EP610-15T		EP610-20 EP610-20T		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	*Note (3)*	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		15		20	20	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		17		22	20	ns
t_{PZX}	Input to output enable	C1 = 35 pF		15		20	20	ns
t_{PXZ}	Input to output disable	C1 = 5 pF, *Note (4)*		15		20	20	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		15		20	20	ns
t_{IO}	I/O input pad and buffer delay			2		2	0	ns
f_{MAX}	Maximum clock frequency	*Note (5)*	83.3		62.5		0	MHz
t_{SU}	Global clock input setup time		9		11		20	ns
t_{H}	Global clock input hold time		0		0		0	ns
t_{CH}	Global clock high time		6		8		0	ns
t_{CL}	Global clock low time		6		8		0	ns
t_{CO1}	Global clock to output delay			11		13	0	ns
t_{CNT}	Global clock minimum period			12		16	0	ns
f_{CNT}	Global clock internal maximum frequency	*Note (6)*	83.3		62.5		0	MHz
t_{ASU}	Array clock input setup time		6		8		20	ns
t_{AH}	Array clock input hold time		6		8		0	ns
t_{ACH}	Array clock high time		7		9		0	ns
t_{ACL}	Array clock low time		7		9		0	ns
t_{ACO1}	Array clock to output delay			15		20	20	ns
t_{ACNT}	Array clock minimum period			14		18	0	ns
f_{ACNT}	Array clock internal maximum frequency	*Note (6)*	71.4		55.6		0	MHz

AC Operating Conditions: EP610-25, EP610-30 & EP610-35 *Notes (1), (2)*

			EP610-25 EP610-25T		EP610-30		EP610-35		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	*Note (3)*	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		25		30		35	30	ns
t_{PD2}	I/O input to non-registered output			27		32		37	30	ns
t_{PZX}	Input to output enable			25		30		35	30	ns
t_{PXZ}	Input to output disable	C1 = 5 pF, *Note (4)*		25		30		35	30	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		27		32		37	30	ns
t_{IO}	I/O input pad and buffer delay			2		2		2	0	ns
f_{MAX}	Maximum frequency	*Note (5)*	47.6		41.7		37.0		0	MHz
t_{SU}	Global clock input setup time		21		24		27		30	ns
t_{H}	Global clock input hold time		0		0		0		0	ns
t_{CH}	Global clock high time		10		11		12		0	ns
t_{CL}	Global clock low time		10		11		12		0	ns
t_{CO1}	Global clock to output delay			15		17		20	0	ns
t_{CNT}	Global clock minimum period			25		30		35	0	ns
f_{CNT}	Global clock internal maximum frequency	*Note (6)*	40.0		33.3		28.6		0	MHz
t_{ASU}	Array clock input setup time		8		8		8		30	ns
t_{AH}	Array clock input hold time		12		12		12		0	ns
t_{ACH}	Array clock high time		10		11		12		0	ns
t_{ACL}	Array clock low time		10		11		12		0	ns
t_{ACO1}	Array clock to output delay			27		32		37	30	ns
t_{ACNT}	Array clock minimum period			25		30		35	0	ns
f_{ACNT}	Array clock internal maximum frequency	*Note (6)*	40.0		33.3		28.6		0	MHz

Notes to tables:

(1) Operating conditions: $V_{CC} = 5\ V \pm 5\%$, $T_A = 0°$ C to 70° C for commercial use.
$V_{CC} = 5\ V \pm 10\%$, $T_A = -40°$ C to 85° C for industrial use.
$V_{CC} = 5\ V \pm 10\%$, $T_C = -55°$ C to 125° C for military use.

(2) See *Application Brief 100 (Understanding Classic, MAX 5000 & MAX 7000 Timing)* for additional internal timing parameters.

(3) See "Turbo Bit" on page 336 of this data sheet. EP610T devices do not have a non-turbo mode.

(4) Sample-tested only for an output change of 500 mV.

(5) The f_{MAX} values represent the highest frequency for pipelined data.

(6) Measured with a device programmed as a 16-bit counter. I_{CC} measured at 0° C.

AC Operating Conditions: EP610 MIL-STD-883-Compliant *Notes (1), (2)*

Symbol	Parameter	Conditions	Min	Max	Unit
t_{PD1}	Input to non-registered output	C1 = 35 pF		35	ns
t_{PD2}	I/O input to non-registered output	*Notes (3), (4)*		37	ns
t_{PZX}	Input to output enable			35	ns
t_{PXZ}	Input to output disable	C1 = 5 pF, *Notes (3), (4), (5), (6)*		35	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF, *Notes (3), (4)*		37	ns
f_{MAX}	Maximum frequency	*Notes (3), (7), (8)*	37.0		MHz
t_{SU}	Global clock input setup time	*Notes (3), (4)*	27		ns
t_{H}	Global clock input hold time	*Note (3)*	0		ns
t_{CH}	Global clock high time	*Note (5)*	12		ns
t_{CL}	Global clock low time	*Note (5)*	12		ns
t_{CO1}	Global clock to output delay			20	ns
t_{CNT}	Global clock minimum period	*Notes (5), (9)*		35	ns
f_{CNT}	Global clock internal maximum frequency	*Note (9)*	28.5		MHz
t_{ASU}	Array clock input setup time	*Notes (3), (4), (5)*	8		ns
t_{AH}	Array clock input hold time	*Notes (3), (4), (5)*	12		ns
t_{ACH}	Array clock high time	*Notes (4), (5)*	12		ns
t_{ACL}	Array clock low time	*Notes (4), (5)*	12		ns
t_{ACO1}	Array clock to output delay	*Notes (3), (4)*		37	ns
t_{ACNT}	Array clock minimum period	*Notes (5), (9)*		35	ns
f_{ACNT}	Array clock internal maximum frequency	*Notes (5), (9)*	28.6		MHz

Notes to tables:

(1) Screening and characterization of AC delay parameters are conducted at 10 MHz or less. Operating conditions: $V_{CC} = 5\ V \pm 10\%$, $T_C = -55°\ C$ to $125°\ C$.

(2) See *Application Brief 100 (Understanding Classic, MAX 5000 & MAX 7000 Timing)* for additional internal timing parameters.

(3) All array-dependent delays are specified for an XOR pattern. This pattern includes two product terms and two pure inputs; all other product terms in the macrocell are held low by one EPROM cell. Other patterns may result in longer delays. Delays for patterns involving only one product term (such as t_{PXZ}) are specified for an XOR pattern in which only one pure input switches at a time.

(4) When the Turbo Bit is not set (non-turbo mode), a non-turbo adder of 30 ns (maximum) is added to this parameter to determine worst-case timing. Parameters may not be tested in non-turbo mode, but are guaranteed to the limits specified. Devices operating in non-turbo mode require one input or I/O transition to guarantee that the device will enter the correct power-up state.

(5) These parameters may not be tested, but are guaranteed to the limits specified in the table under "Absolute Maximum Ratings" on page 349.

(6) Not tested directly, but guaranteed by testing t_{PD}.

(7) The f_{MAX} values represent the highest frequency for pipelined data.

(8) Not tested directly, but derived from t_{SU}.

(9) Specified with device programmed as a 16-bit counter with no output loading.

AC Operating Conditions: EP610I *Notes (1), (2)*

		EP610I-10		EP610I-15		EP610I-25		Non-Turbo Adder	
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	*Note (3)*	**Units**
t_{PD1}	Input to non-registered output, *Note (4)*		10		15		25	25	ns
t_{PD2}	I/O input to non-registered output, *Note (4)*		10		15		25	25	ns
t_{PZX}	Input to output enable		15		18		25	25	ns
t_{PXZ}	Input to output disable, *Note (5)*		13		18		25	25	ns
t_{CLR}	Asynchronous output clear time		13		18		25	25	ns
f_{MAX}	Maximum frequency	111		83.3		66		0	MHz
t_{SU}	Global clock input setup time	7		12		15		25	ns
t_{H}	Global clock input hold time	0		0		0		0	ns
t_{CH}	Global clock high time	5		6		7.5		0	ns
t_{CL}	Global clock low time	5		6		7.5		0	ns
t_{CO1}	Global clock to output delay		6.5		8		10		ns
t_{CNT}	Global clock minimum period		10		15		25	25	ns
f_{CNT}	Global clock internal maximum frequency, *Note (6)*	100		66		40		0	MHz
t_{ASU}	Array clock input setup time	2		4		5		25	ns
t_{AH}	Array clock input hold time	3		6		8		0	ns
t_{ACH}	Array clock high time	5		7.5		10		0	ns
t_{ACL}	Array clock low time	5		7.5		10		0	ns
t_{ACO1}	Array clock to output delay		12		16		25	25	ns
t_{ACNT}	Array clock minimum period, *Note (6)*		10		15		25	25	ns
f_{ACNT}	Array clock internal maximum frequency, *Note (6)*	100		66		40		0	MHz

Notes to tables:

(1) Operating conditions: $V_{CC} = 5\ V \pm 5\%$, $T_A = 0°$ C to 70° C for commercial use.
$V_{CC} = 5\ V \pm 10\%$, $T_A = -40°$ C to 85° C for industrial use.

(2) See *Application Brief 100 (Understanding Classic, MAX 5000 & MAX 7000 Timing)* for additional internal timing parameters.

(3) See "Turbo Bit" on page 336 of this data sheet.

(4) Measured with eight outputs switching.

(5) Sample-tested only for an output change of 500 mV.

(6) Measured with a device programmed as a 16-bit counter.

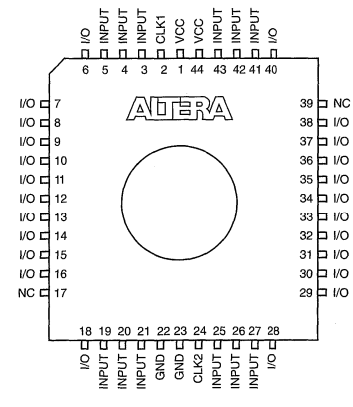
Notes:

Features

- High-performance, 24-macrocell Classic EPLD
  - Combinatorial speeds with t_{PD} as low as 12 ns
  - Counter frequencies of up to 100 MHz
  - Pipelined data rates of up to 100 MHz
- Programmable I/O architecture with up to 36 inputs or 24 outputs
- The following devices are compatible pin-, function-, and programming file-compatible: EP910, EP910T, and EP910I
- Programmable Clock option for independent clocking of all registers
- Macrocells individually programmable as D, T, JK, or SR flipflops, or for combinatorial operation
- Available in windowed ceramic and one-time-programmable (OTP) plastic packages (see Figure 11):
  - 44-pin J-lead chip carrier (JLCC and PLCC)
  - 40-pin dual in-line package (CerDIP and PDIP)

Figure 11. EP910 Package Pin-Out Diagrams

Package outlines not drawn to scale. Windows in ceramic packages only.



44-Pin J-Lead

EP910
EP910T
EP910I

40-Pin DIP

EP910
EP910T
EP910I

8 Classic

Table 3 summarizes EP910 features.

Table 3. EP910 Device Features

Feature	EP910-30	EP910-35	EP910-40	EP910T	EP910I
t_{PD}	30	35	40	30	12
Counter frequency	33 MHz	28 MHz	25 MHz	33 MHz	100 MHz
Pipeline data rates	41 MHz	37 MHz	32 MHz	41 MHz	100 MHz
Packages	44-pin JLCC 44-pin PLCC 40-pin CerDIP 40-pin PDIP	44-pin JLCC 44-pin PLCC 40-pin CerDIP 40-pin PDIP	44-pin JLCC 44-pin PLCC 40-pin CerDIP 40-pin PDIP	44-pin PLCC 40-pin PDIP	44-pin PLCC 40-pin CerDIP 40-pin PDIP

General Description

The Altera EP910 EPLD can implement up to 900 equivalent gates of SSI and MSI logic functions. The EP910 has 24 macrocells, 12 dedicated input pins, 24 I/O pins, and 2 global Clock pins (see Figure 12). Each macrocell can access signals from the global bus, which consists of the true and complement forms of the dedicated inputs and the true and complement forms of either the output of the macrocell or the I/O input. CLK1 and CLK2 are the dedicated Clock inputs for the registers in macrocells 13 through 24 and 1 through 12, respectively.

Figure 12. EP910 Block Diagram

Numbers without parentheses are for DIP packages. Numbers in parentheses are for J-lead packages.

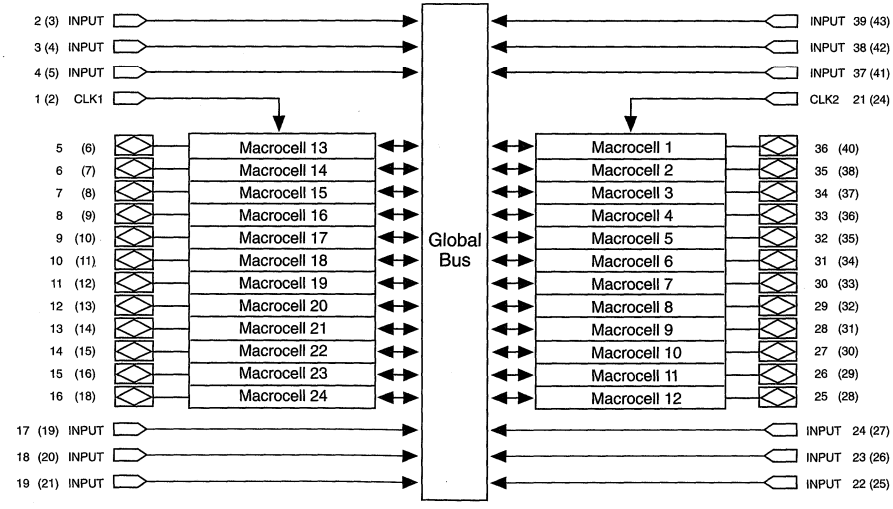


Figure 13 shows typical supply current (I_{CC}) versus frequency for EP910 devices.

Figure 13. EP910 I_{CC} vs. Frequency

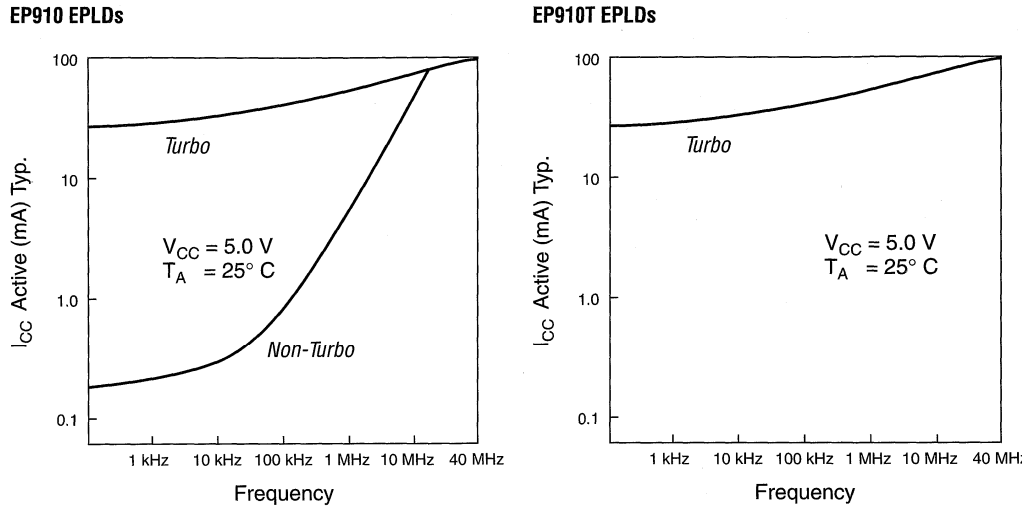
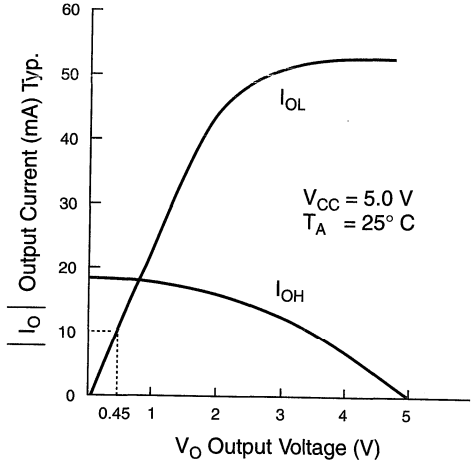


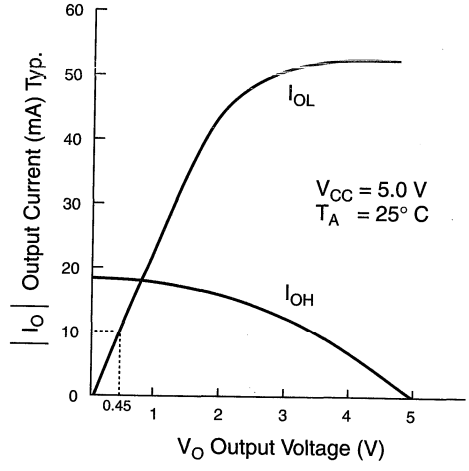
Figure 14 shows the output drive characteristics of EP910 I/O pins.

Figure 14. EP910 Output Drive Characteristics

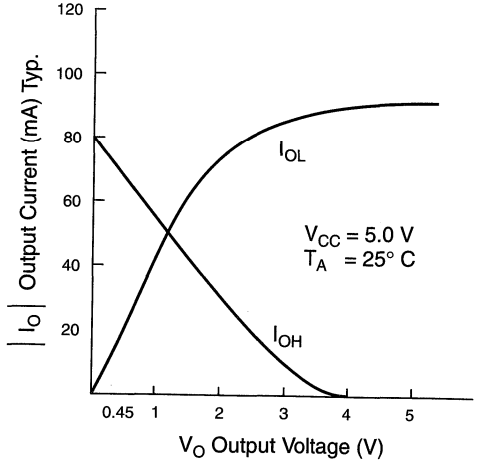
EP910 EPLDs



EP910T EPLDs



EP910I EPLDs



Absolute Maximum Ratings *Note (1)*

			EP910 EP910T		EP910I		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
V_{CC}	Supply voltage	*Notes (2), (3)*	–2.0	7.0	–2.0	7.0	V
V_I	DC input voltage	*Notes (2), (3)*	–2.0	7.0	–0.5	V_{CC} + 0.5	V
I_{MAX}	DC V_{CC} or GND current		–250	250			mA
I_{OUT}	DC output current, per pin		–25	25			mA
P_D	Power dissipation			1,200			mW
T_{STG}	Storage temperature	No bias	–65	150	–65	150	° C
T_{AMB}	Ambient temperature	*Note (4)*	–65	135	–10	85	° C

Recommended Operating Conditions *Note (5)*

			EP910 EP910T		EP910I		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
V_{CC}	Supply voltage	*Note (6)*	4.75 (4.5)	5.25 (5.5)	4.75	5.25	V
V_I	Input voltage		0	V_{CC}	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	0	70	° C
T_A	Operating temperature	For industrial use	–40	85			° C
T_C	Case temperature	For military use	–55	125			° C
t_R	Input rise time	*Note (7)*		100 (50)		500	ns
t_F	Input fall time	*Note (7)*		100 (50)		500	ns

DC Operating Conditions *Notes (5), (8), (9)*

Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OH}	High-level CMOS output voltage	I_{OH} = –2 mA DC	3.84			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC			0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	–10		10	µA
I_{OZ}	Tri-state output leakage current	V_O = V_{CC} or GND	–10		10	µA

Capacitance *Notes (8), (10)*

			EP910 EP910T		EP910I		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20		8	pF
C_{IO}	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20		8	pF
C_{CLK1}	CLK1 pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20		10	pF
C_{CLK2}	CLK2 pin capacitance	V_{IN} = 0 V, f = 1.0 MHz				12	pF

I_{CC} Supply Current *Notes (5), (8), (9)*

			EP910			EP910T			EP910I			
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{CC1}	V_{CC} supply current (non-turbo, standby)	V_I = V_{CC} or GND, no load, *Notes (11), (12)*		20	150					60	150	µA
I_{CC2}	V_{CC} supply current (non-turbo, active)	V_I = V_{CC} or GND, no load, f = 1.0 MHz, *Note (12)*		6	20					4	12	mA
I_{CC3}	V_{CC} supply current (turbo, active)			45	80 (100)		80	115		120	150	mA

Notes to tables:

(1) See *Operating Requirements for Altera Devices* in this data book.
(2) Voltage with respect to ground.
(3) For EP910 and EP910T EPLDs, the minimum DC input is –0.3 V; for EP910I EPLDs, the minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions.
(4) Under bias. Extended temperature versions are also available.
(5) Numbers in parentheses are for industrial temperature versions.
(6) Maximum V_{CC} rise time for EP910 and EP910T devices = 50 ms; for EP910I devices, maximum V_{CC} rise time is unlimited with monotonic rise.
(7) For all Clocks: t_R and t_F = 100 ns (50 ns for military- and industrial-temperature-range versions).
(8) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
(9) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(10) For EP910 and EP910T devices: capacitance measured at 25° C; sample-tested only; Clock-pin capacitance for dedicated Clock inputs only; pin 21 (high-voltage pin during programming) has a maximum capacitance of 60 pF. Values for EP910I devices are evaluated during initial characterization and design modifications.
(11) When the Turbo Bit is not set (non-turbo mode), an EP910I device will enter standby mode if no logic transitions occur for 75 ns after the last transition.
(12) Measured with a device programmed as a 24-bit counter.

AC Operating Conditions: EP910 *Notes (1), (2)*

			EP910-30 EP910T-30		EP910-35		EP910-40		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	*Note (3)*	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		30		35		40	30	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		33		38		43	30	ns
t_{PZX}	Input to output enable	C1 = 35 pF		30		35		40	30	ns
t_{PXZ}	Input to output disable	C1 = 5 pF, *Note (4)*		30		35		40	30	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		33		38		43	30	ns
t_{IO}	I/O input pad and buffer delay			3		3		3	0	ns
f_{MAX}	Maximum frequency	*Note (5)*	41.7		37.0		32.3		0	MHz
t_{SU}	Global clock input setup time		24		27		31		30	ns
t_{H}	Global clock input hold time		0		0		0		0	ns
t_{CH}	Global clock high time		12		13		15		0	ns
t_{CL}	Global clock low time		12		13		15		0	ns
t_{CO1}	Global clock to output delay			18		21		24	0	ns
t_{CNT}	Global clock minimum clock period			30		35		40	0	ns
f_{CNT}	Global clock internal maximum frequency	*Note (6)*	33.3		28.6		25.0		0	MHz
t_{ASU}	Array clock input setup time		10		10		10		30	ns
t_{AH}	Array clock input hold time		15		15		15		0	ns
t_{ACH}	Array clock high time		15		16		17		0	ns
t_{ACL}	Array clock low time		15		16		17		0	ns
t_{ACO1}	Array clock to output delay			33		38		43	30	ns
t_{ACNT}	Array clock minimum clock period			30		35		40	0	ns
f_{ACNT}	Array clock internal maximum frequency	*Note (6)*	33.3		28.6		25.0		0	MHz

Notes to tables:

(1) Operating conditions: $V_{CC} = 5\ V \pm 5\%$, $T_A = 0°C$ to $70°C$ for commercial use.
$V_{CC} = 5\ V \pm 10\%$, $T_A = -40°C$ to $85°C$ for industrial use.

(2) See *Application Brief 100 (Understanding Classic, MAX 5000 & MAX 7000 Timing)* for additional internal timing parameters.

(3) See "Turbo Bit" on page 336 of this data sheet. EP910T devices have no non-turbo mode.

(4) Sample-tested only for an output change of 500 mV.

(5) The f_{MAX} values represent the highest frequency for pipelined data.

(6) Measured with a device programmed as a 24-bit counter. I_{CC} measured at $0°C$.

AC Operating Conditions: EP910I *Notes (1), (2)*

		EP910I-12		EP910I-15		EP910I-25		Non-Turbo Adder	
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	*Note (3)*	**Unit**
t_{PD1}	Input to non-registered output, *Note (4)*		12		15		25	40	ns
t_{PZX}	Input to output enable, *Note (5)*		15		18		28	40	ns
t_{PXZ}	Input to output disable, *Note (5)*		15		18		28	40	ns
t_{CLR}	Asynchronous output clear time		15		18		28	40	ns
f_{MAX}	Global clock maximum frequency	100		83.3		50		0	MHz
t_{SU}	Global clock input setup time	8		11		16		40	ns
t_{H}	Global clock input hold time	0		0		0		0	ns
t_{CH}	Global clock high time	5		6		10		0	ns
t_{CL}	Global clock low time	5		6		10		0	ns
t_{CO}	Global clock to output delay, *Note (6)*		8		9		14	0	ns
t_{CNT}	Global clock minimum clock period		13		15		25	40	ns
f_{CNT}	Global clock internal maximum frequency, *Note (6)*	76.9		66.6		40		0	MHz
t_{ASU}	Array clock input setup time	3		4		8		40	ns
t_{AH}	Array clock input hold time	6		7		8			ns
t_{ACH}	Array clock high time	6		7.5		12.5			ns
t_{ACL}	Array clock low time	6		7.5		12.5			ns
t_{ACO1}	Array clock to output delay, *Note (6)*		16		18		28	40	ns
t_{ACNT}	Array clock minimum clock period		13		15		25	40	ns
f_{ACNT}	Array clock internal maximum frequency, *Note (6)*	76.9		66.6		40			MHz

Notes to tables:

(1) Operating conditions: $V_{CC} = 5\ V \pm 5\%$, $T_A = 0°C$ to $70°C$ for commercial use.
$V_{CC} = 5\ V \pm 10\%$, $T_A = -40°C$ to $85°C$ for industrial use.

(2) See *Application Brief 100 (Understanding Classic, MAX 5000 & MAX 7000 Timing)* for additional internal timing parameters.

(3) If the device is inactive for more than 75 ns while operated in non-turbo mode, increase time by amount shown. See "Turbo Bit" on page 336 of this data sheet.

(4) Measured with eight outputs switching.

(5) The t_{PZX} and t_{PXZ} parameters are measured at ± 0.5 V from steady-state voltage as driven by specified output load.

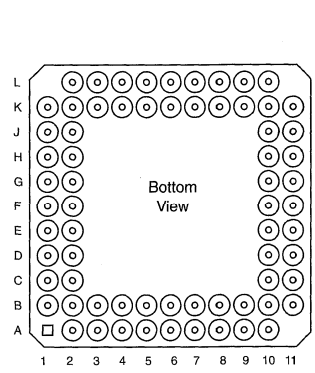
(6) Measured with device programmed as a 24-bit counter.

Features

- High-performance, 48-macrocell Classic EPLD
  - Combinatorial speeds with t_{PD} as low as 20 ns
  - Counter frequencies of up to 50 MHz
  - Pipelined data rates of up to 62.5 MHz
- Programmable I/O architecture with up to 64 inputs or 48 outputs
- The following devices are pin-, function-, and programming file-compatible: EP1810, EP1810T, and EP1810 MIL-STD-883-compliant
- Programmable Clock option for independent clocking of all registers
- Macrocells individually programmable as D, T, JK, or SR flipflops, or for combinatorial operation
- Available in 68-pin windowed ceramic and one-time-programmable (OTP) plastic packages (see Figure 15):
  - Pin-grid array package (ceramic PGA only)
  - J-lead chip carrier (JLCC and PLCC)

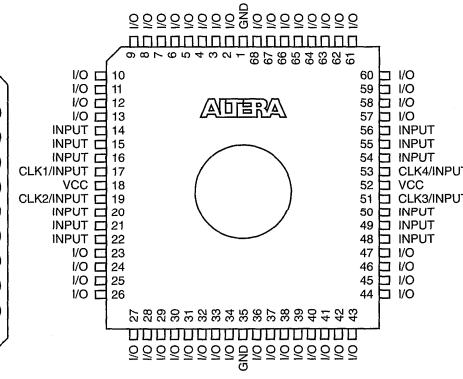
Figure 15. EP1810 Package Pin-Out Diagrams

Package outlines not drawn to scale. See Table 5 in this data sheet for PGA package pin-out information. Windows in ceramic packages only.



68-Pin PGA

EP1810
EP1810 MIL-STD-883-Compliant



68-Pin J-Lead

EP1810
EP1810T

8 Classic

Table 4 summarizes EP1810 device features.

Table 4. EP1810 Device Features

Feature	EP1810	EP1810T	EP1810 MIL-STD-883-Compliant
t_{PD}	20 ns	20 ns	45 ns
Counter frequency	50 MHz	50 MHz	22.2 MHz
Pipeline data rates	62.5 MHz	62.5 MHz	33.3 MHz
Packages	68-pin PGA 68-pin JLCC 68-pin PLCC	68-pin PLCC	68-pin PGA

General Description

The Altera EP1810 EPLD offers LSI density, TTL-equivalent speed, and low power consumption. The EP1810 has 48 macrocells, 16 dedicated input pins, and 48 I/O pins (see Figure 16). The EP1810 is divided into four quadrants, each containing 12 macrocells. Of the twelve macrocells in each quadrant, 8 have quadrant feedback and are "local" macrocells (see "Feedback Selection" on page 340 of this data sheet for more information). The remaining 4 macrocells in the quadrant are "global" macrocells. Both local and global macrocells can access signals from the global bus, which consists of the true and complement forms of the dedicated inputs and the true and complement forms of the feedbacks from the global macrocells.

The EP1810 also has four dedicated inputs (one in each quadrant) that can be used as quadrant Clock inputs. If the dedicated input is used as a Clock pin, the input feeds the Clock input of all registers in that particular quadrant.

Figure 16. EP1810 Block Diagram

Numbers in parentheses are for J-lead packages. Numbers without parentheses are for PGA packages.

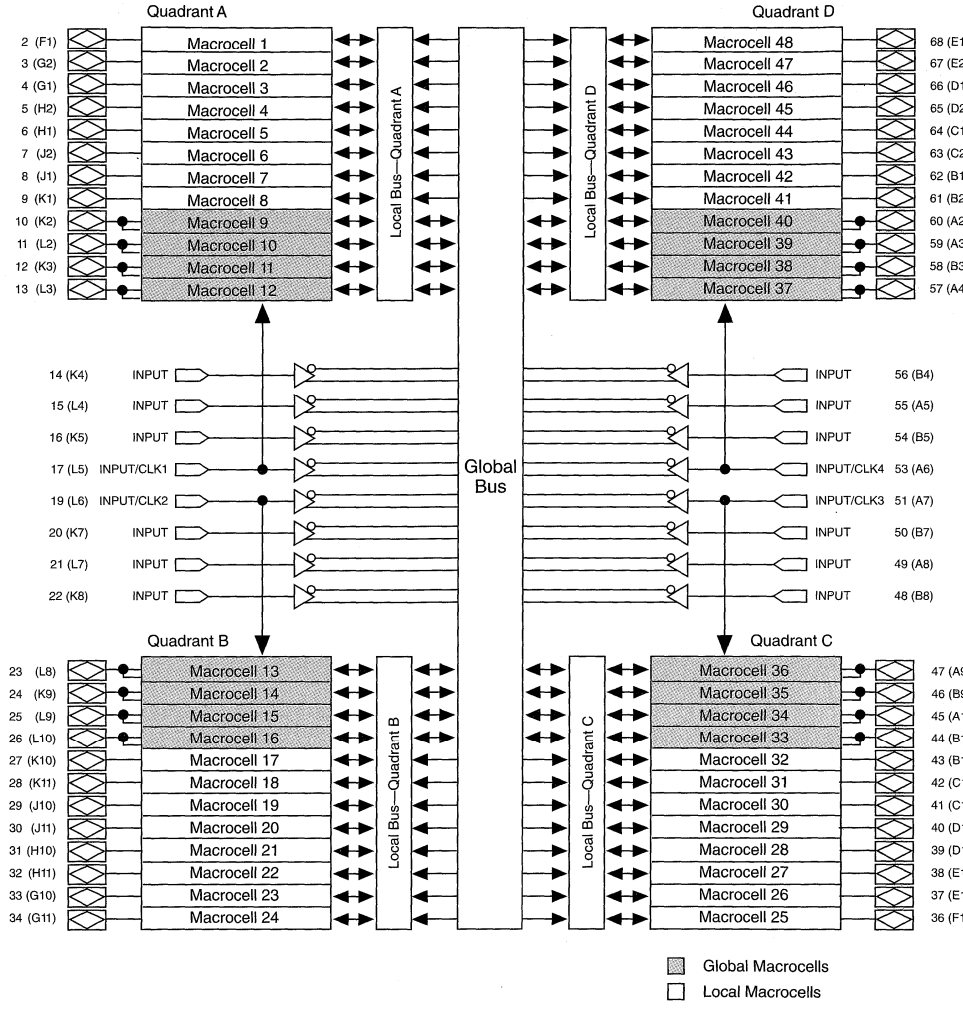


Figure 17 shows the typical supply current (I_{CC}) versus frequency for the EP1810 EPLDs.

Figure 17. EP1810 I_{CC} vs. Frequency

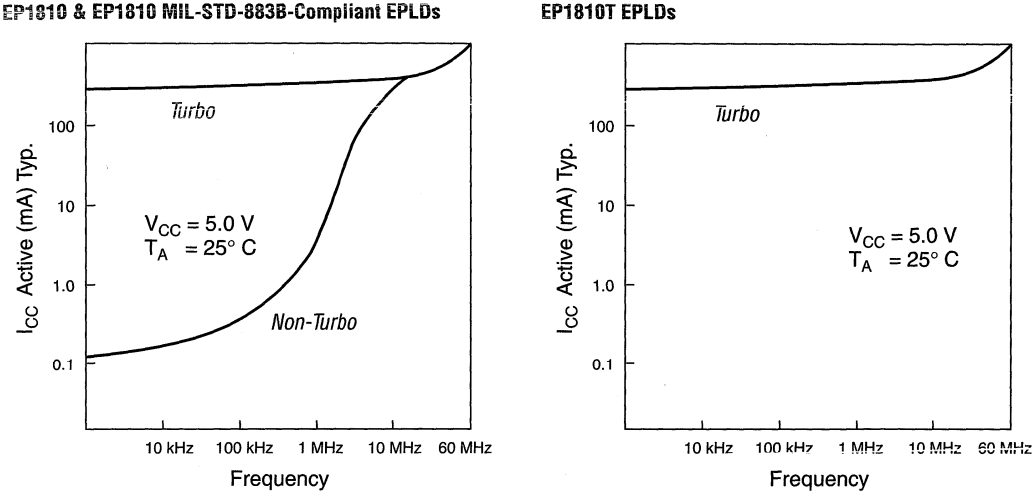
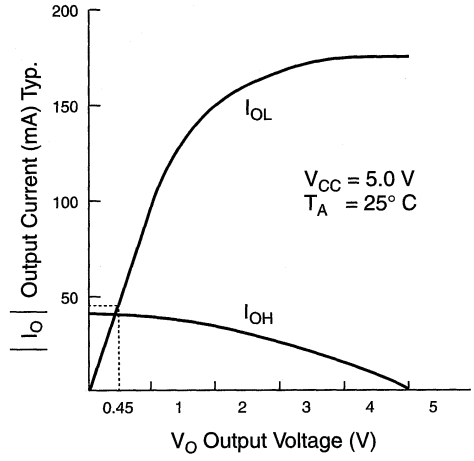


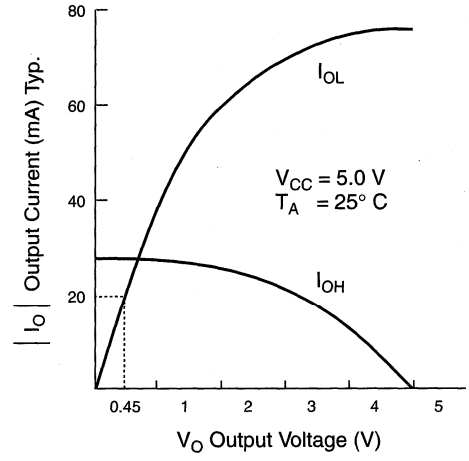
Figure 18 shows the output drive characteristics of EP1810 I/O pins.

Figure 18. EP1810 Output Drive Characteristics

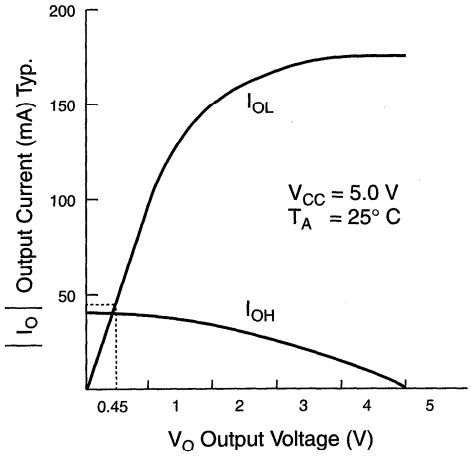
EP1810-20 & EP1810-25 EPLDs
(Including MIL-STD-883-Compliant Versions)



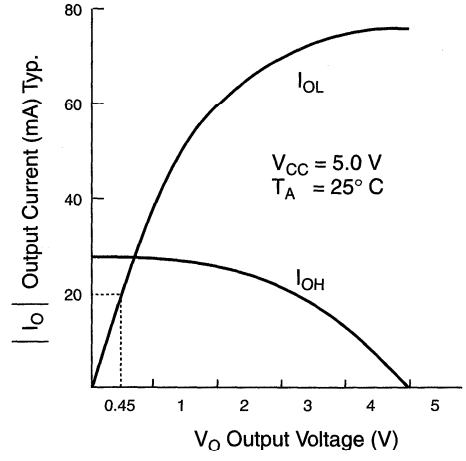
EP1810-35 & EP1810-45 EPLDs
(Including MIL-STD-883-Compliant Versions)



EP1810-20T & EP1810-25T EPLDs



EP1810-35T EPLDs



Absolute Maximum Ratings *Notes (1), (2)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND, *Notes (2), (3)*	–2.0 (–0.5)	7.0	V
V_I	DC input voltage		–2.0 (–0.5)	7.0	V
I_{MAX}	DC V_{CC} or GND current		–300 (–400)	300 (400)	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1,500 (2,000)	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65 (–55)	135 (125)	° C
T_J	Junction temperature	Under bias		(150)	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	*Notes (2), (4)*	4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time	*Note (5)*		50	ns
t_F	Input fall time	*Note (5)*		50	ns

DC Operating Conditions *Notes (2), (6), (7)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC, *Note (8)*	2.4			V
V_{OH}	High-level CMOS output voltage	I_{OH} = –2 mA DC, *Note (8)*	3.84			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC, *Note (8)*			0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	–10		10	µA
I_{OZ}	Tri-state output leakage current	V_O = V_{CC} or GND	–10		10	µA

Capacitance *Note (9)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20	pF
C_{IO}	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF
C_{CLK}	Clock pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		25	pF

I_{CC} Supply Current *Notes (2), (6), (7)*

				EP1810			EP1810T			EP1810 MIL-STD-883-Compliant			
Symbol	Parameter	Conditions	Speed Grade	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{CC1}	V_{CC} supply current (non-turbo, standby)	V_I = V_{CC} or GND, I/O = 0, *Notes (10), (11)*	-20, -25		50	150						900	µA
			-35, -45		35	150							µA
I_{CC2}	V_{CC} supply current (non-turbo, active)	V_I = V_{CC} or GND, no load, f = 1.0 MHz, *Notes (2), (10), (11), (12)*	-20, -25		20	40						40	mA
			-35, -45		10	30 (40)							mA
I_{CC3}	V_{CC} supply current (turbo, active)	V_I = V_{CC} or GND, no load, f = 1.0 MHz, *Notes (2), (10), (12)*	-20, -25		180	225 (250)		180	250			240	mA
			-35, -45		100	180 (240)		120	215				mA

Notes to tables:

(1) See *Operating Requirements for Altera Devices* in this data book.
(2) Numbers in parentheses are for military- and industrial-temperature-range versions.
(3) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no-load conditions. For EP1810-20T and EP1810-25T devices: maximum V_{PP} is 14.0 V.
(4) Maximum V_{CC} rise time is 50 ms.
(5) For EP1810 Clocks: t_R and t_F = 100 ns (50 ns for military and industrial temperature versions). For EP1810-20T and EP1810-25T Clocks: t_R and t_F = 20 ns.
(6) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(7) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C for military use.
(8) Tested at 25° C and 125° C only.
(9) Capacitance measured at 25° C. Sample-tested only. Clock-pin capacitance for dedicated Clock inputs only. Pin 19 has a maximum capacitance of 160 pF.
(10) Measured with a device programmed as four 12-bit counters. I_{CC} measured at 0° C.
(11) Tested at 25° C only.
(12) Tested with non-output loading using a data pattern specified by Altera. Data path is correlated to four 12-bit counters.

AC Operating Conditions: EP1810-20 & EP1810-25 *Note (1)*

External Timing Parameters			EP1810-20 EP1810-20T		EP1810-25 EP1810-25T		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	*Note (2)*	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		20		25	25	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		22		28	25	ns
t_{SU}	Global clock setup time		13		17		25	ns
t_{H}	Global clock hold time		0		0		0	ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		15		18	0	ns
t_{CH}	Global clock high time		8		10		0	ns
t_{CL}	Global clock low time		8		10		0	ns
t_{ASU}	Array clock setup time		8		10		25	ns
t_{AH}	Array clock hold time		8		10		0	ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		20		25	25	ns
t_{CNT}	Minimum global clock period			20		25	0	ns
f_{CNT}	Maximum internal frequency	*Note (3)*	50		40		0	MHz
f_{MAX}	Maximum clock frequency	*Note (4)*	62.5		50		0	MHz

Internal Timing Parameters			EP1810-20 EP1810-20T		EP1810-25 EP1810-25T		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	*Note (2)*	**Unit**
t_{IN}	Input pad and buffer delay			5		7	0	ns
t_{IO}	I/O input pad and buffer delay			2		3	0	ns
t_{LAD}	Logic array delay			9		12	25	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		6		6	0	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		6		6	0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF, *Note (4)*		6		6	0	ns
t_{SU}	Register setup time		8		10		0	ns
t_{H}	Register hold time		8		10		0	ns
t_{IC}	Array clock delay			9		12	25	ns
t_{ICS}	Global clock delay			4		5	0	ns
t_{FD}	Feedback delay			3		3	–25	ns
t_{CLR}	Register clear time			9		12	25	ns

AC Operating Conditions: EP1810-35 & EP1810-45 *Note (1)*

External Timing Parameters			EP1810-35 EP1810-35T		EP1810-45		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	*Note (2)*	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		35		45	30	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		40		50	30	ns
t_{SU}	Global clock setup time		25		30		30	ns
t_{H}	Global clock hold time		0		0		0	ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		20		25	0	ns
t_{CH}	Global clock high time		12		15		0	ns
t_{CL}	Global clock low time		12		15		0	ns
t_{ASU}	Array clock setup time		10		11		30	ns
t_{AH}	Array clock hold time		15		18		0	ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		35		45	30	ns
t_{CNT}	Minimum global clock period			35		45	0	ns
f_{CNT}	Maximum internal frequency	*Note (3)*	28.6		22.2		0	MHz
f_{MAX}	Maximum clock frequency	*Note (5)*	40		33.3		0	MHz

Internal Timing Parameters			EP1810-35 EP1810-35T		EP1810-45		Non-Turbo Adder	
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	*Note (2)*	**Unit**
t_{IN}	Input pad and buffer delay			7		6	0	ns
t_{IO}	I/O input pad and buffer delay			5		5	0	ns
t_{LAD}	Logic array delay			19		28	30	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		9		11	0	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		9		11	0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF, *Note (5)*		9		11	0	ns
t_{SU}	Register setup time		10		10		0	ns
t_{H}	Register hold time		15		18		0	ns
t_{IC}	Array clock delay			19		28	30	ns
t_{ICS}	Global clock delay			4		8	0	ns
t_{FD}	Feedback delay			6		7	–30	ns
t_{CLR}	Register clear time			24		32	30	ns

Notes to tables:

(1) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5 V ± 10%, T_C = –55° C to 125° C for military use.

(2) See "Turbo Bit" on page 336 of this data sheet.

(3) Measured with a device programmed as four 12-bit counters. I_{CC} measured at 0° C.

(4) Sample-tested only for an output change of 500 mV.

(5) The f_{MAX} values represent the highest frequency for pipelined data.

AC Operating Conditions: EP1810 MIL-STD-883-Compliant *Note (1)*

External Timing Parameters					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF, *Notes (2), (3)*		45	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF, *Notes (2), (3)*		55	ns
t_{SU}	Global clock setup time	*Notes (2), (3)*	30		ns
t_{H}	Global clock hold time	*Note (4)*	0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF, *Note (3)*		25	ns
t_{CH}	Global clock high time		15		ns
t_{CL}	Global clock low time		15		ns
t_{ASU}	Array clock setup time	*Notes (2), (3)*	13		ns
t_{AH}	Array clock hold time	*Notes (2), (3)*	18		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF, *Notes (2), (3)*		50	ns
t_{CNT}	Minimum global clock period	*Note (3)*		45	ns
f_{CNT}	Maximum internal frequency	*Note (5)*	22.2		MHz
f_{MAX}	Maximum clock frequency	*Notes (2), (3), (6), (7)*	33.3		MHz
t_{PZX}	Input to output enable	*Notes (2), (3)*		45	ns
t_{PXZ}	Input to output disable	C1 = 5 pF, *Notes (2), (3), (8), (9)*		45	ns

Notes:

(1) Screening and characterization of AC delay parameters are conducted at 10 MHz or less. Operating conditions: $V_{CC} = 5\ V \pm 10\%$, $T_C = -55°\ C$ to $125°\ C$.

(2) All array-dependent delays are specified for an XOR pattern. This pattern includes two product terms and two pure inputs; all other product terms in the macrocell are held low by one EPROM pull-down. Other patterns may result in longer delays. Delays for patterns involving only one product term (such as t_{PXZ}) are specified for an XOR-like pattern in which only one pure input switches at a time.

(3) When the Turbo Bit is not set (non-turbo mode), a non-turbo adder of 30 ns maximum (40 ns for t_{ASU}) is applied. Parameters cannot be tested in non-turbo mode, but are guaranteed to the limits specified. Devices operating in non-turbo mode require one input or I/O transition to guarantee that the device will enter the correct power-up state.

(4) Tested with non-output loading using a data pattern specified by Altera. Data path is correlated to four 12-bit counters.

(5) Not tested directly, but guaranteed by testing t_{CNT} or t_{ACNT}.

(6) The f_{MAX} values represent the highest frequency for pipelined data.

(7) Not tested directly, but derived from t_{SU}.

(8) May not be tested, but is guaranteed to the limits specified in the table under "Absolute Maximum Ratings."

(9) Sample tested only for an output change of 500 mV.

Pin-Out Information

Table 5 provides pin-out information for EP1810 devices in the PGA package.

Table 5. EP1810 PGA Pin-Outs

Pin	Function	Pin	Function	Pin	Function	Pin	Function
A2	I/O	B9	I/O	F10	GND	K4	INPUT
A3	I/O	B10	I/O	F11	I/O	K5	INPUT
A4	I/O	B11	I/O	G1	I/O	K6	VCC
A5	INPUT	C1	I/O	G2	I/O	K7	INPUT
A6	CLK4/INPUT	C2	I/O	G10	I/O	K8	INPUT
A7	CLK3/INPUT	C10	I/O	G11	I/O	K9	I/O
A8	INPUT	C11	I/O	H1	I/O	K10	I/O
A9	I/O	D1	I/O	H2	I/O	K11	I/O
A10	I/O	D2	I/O	H10	I/O	L2	I/O
B1	I/O	D10	I/O	H11	I/O	L3	I/O
B2	I/O	D11	I/O	J1	I/O	L4	INPUT
B3	I/O	E1	I/O	J2	I/O	L5	CLK1/INPUT
B4	INPUT	E2	I/O	J10	I/O	L6	CLK2/INPUT
B5	INPUT	E10	I/O	J11	I/O	L7	INPUT
B6	VCC	E11	I/O	K1	I/O	L8	I/O
B7	INPUT	F1	I/O	K2	I/O	L9	I/O
B8	INPUT	F2	GND	K3	I/O	L10	I/O

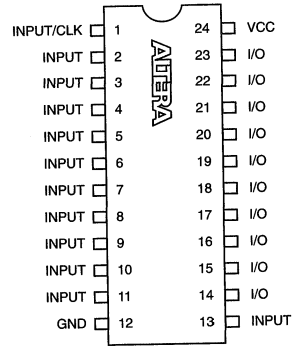
Notes:

Features

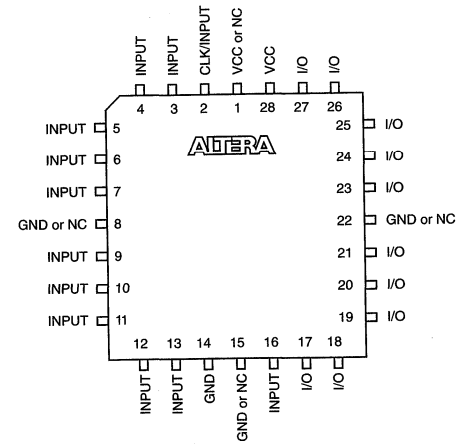
- High-performance, 10-macrocell Classic EPLD
  - Combinatorial speeds with t_{PD} as low as 7.5 ns
  - Counter frequencies of up to 111.1 MHz
  - Pipelined data rates of up to 109.8 MHz
- 1.0-micron CMOS technology with EPROM configuration elements
- Programmable I/O architecture with 12 dedicated inputs and 10 I/O pins
- Up to 16 product terms per macrocell, with selectable output polarity and separate Output Enable
- Global asynchronous Reset and synchronous Preset product terms
- Industry-standard 22V10 architecture
- Enhanced version with superset Clock and feedback features (EP22V10E)
- Available in one-time-programmable (OTP) plastic packages (see Figure 19)
  - 24-pin plastic dual in-line package (PDIP)
  - 28-pin plastic J-lead chip carrier (PLCC)

Figure 19. EP22V10 Package Outlines

Package outlines not drawn to scale.



24-Pin DIP
EP22V10
EP22V10E



28-Pin J-Lead
EP22V10
EP22V10E

Table 6 summarizes EP22V10 features.

Table 6. EP22V10 Device Features

Feature	EP22V10	EP22V10E
t_{PD}	7.5 ns	10 ns
Counter frequency	111.1 MHz	95.2 MHz
Pipeline data rates	109.8 MHz	100 MHz
Packages	24-pin PDIP 28-pin PLCC	24-pin CerDIP 24-pin PDIP 28-pin PLCC

General Description

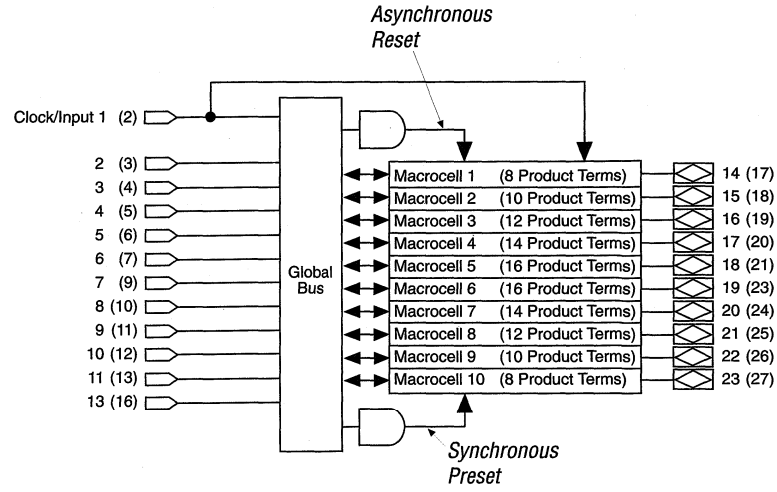
Altera's EP22V10 devices are high-performance, high-integration, general-purpose EPLDs that use 1.0-micron CMOS technology with EPROM configuration elements. These devices accommodate logic functions with up to 22 inputs and 10 I/O macrocells, including an average of 12 input product terms and a separate product term for Output Enable. The EP22V10 provides a high-speed, low-cost, low-power upgrade from PAL and GAL devices. Altera's EP22V10 devices are pin- and JEDEC file-compatible with industry-standard 22V10s. The EP22V10E offers an enhanced macrocell, including an inverted Clock option and an additional feedback path.

Functional Description

The EP22V10 is an optimized device featuring 10 macrocells, 12 dedicated input pins, and 10 I/O pins. Each I/O pin is associated with a macrocell (see Figure 20); all inputs and feedback signals, and their complements, are available to product terms. The product terms form a global bus that feeds each macrocell. Depending on its position, each macrocell can use from 8 to 16 product terms.

Figure 20. EP22V10 Block Diagram

Numbers in parentheses are for PLCC packages.



The EP22V10 architecture includes the following elements:

- Macrocells
- Register Reset and Preset
- Programmable Output Enable
- Power-on characteristics

Macrocells

Each EP22V10 macrocell can be programmed to function as an input, or as a combinatorial or registered output. Each combinatorial or registered output can be active-high or active-low.

EP22V10

The EP22V10 macrocell, shown in Figure 21, offers registered or combinatorial logic with active-high or active-low outputs. In EP22V10 devices, the output type determines the feedback type (if feedback is used); registered output dictates registered feedback, and combinatorial output dictates pin feedback. Because outputs may be programmed as either active-high or active-low on a macrocell-by-macrocell basis, the polarity of the output pin associated with the macrocell register is independent of the register itself.

Figure 21. EP22V10 Macrocell Architecture

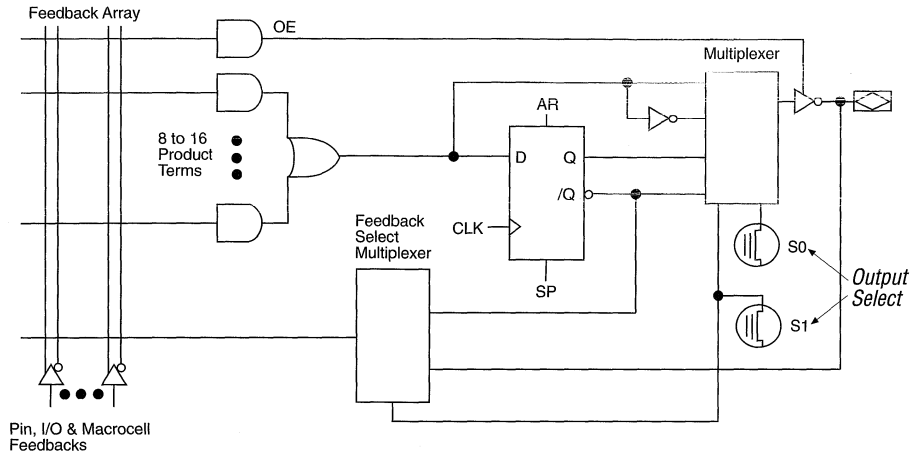


Table 7 lists the output configurations for EP22V10 device.

Table 7. EP22V10 Macrocell Configurations

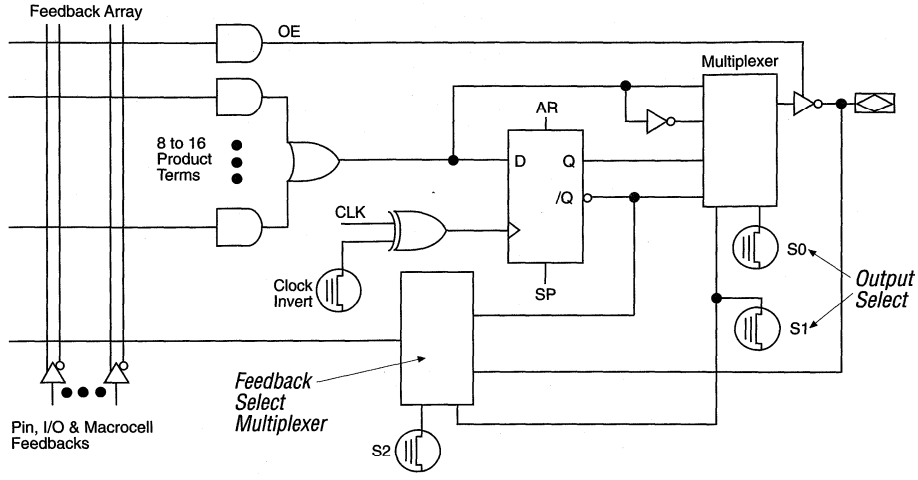
S1	S0	Output/Polarity	Feedback
0	0	Registered/active low	Registered
0	0	Registered/active high	Registered
1	0	Combinatorial/active low	Pin
1	1	Combinatorial/active high	Pin

Pin 1 can supply the Clock input (CLK) for the macrocell registers or be used as a generic input. The Output Enable (OE) for each macrocell is controlled by an independent, asynchronous product term in the array.

EP22V10E

The EP22V10E macrocell has an enhanced Clock and improved feedback selection. See Figure 22. In this macrocell, the Clock can be inverted using the attached XOR gate, allowing the macrocell flipflop to latch at the falling edge—rather than the rising edge—of the CLK input.

Figure 22. EP22V10E Macrocell Architecture



To further enhance the macrocell, an S2 switch has been added to the feedback select multiplexer. See Table 8 for feedback output configurations.

Table 8. EP22V10E Macrocell Configurations

S2	S1	S0	Output/Polarity	Feedback
0	0	0	Registered/active low	Registered
0	0	1	Registered/active high	Registered
0	1	0	Combinatorial/active low	Pin
0	1	1	Combinatorial/active high	Pin
1	0	0	Registered/active low	Pin
1	0	1	Registered/active high	Pin
1	1	0	Combinatorial/active low	Registered
1	1	1	Combinatorial/active high	Registered

All combinations of output and feedback are supported by the EP22V10E. A combinatorial signal can drive the macrocell, while a registered version of that signal is fed back into the device.

Register Reset & Preset

All EP22V10 macrocell registers can be preset or reset using global Preset and Reset product terms. The register Preset is synchronous and must meet the specified Clock setup time; the register Reset is asynchronous and has no Clock setup requirement. Output polarity is selected separately.

The global Preset signal is determined by a single product term originating from the feedback array. When the signal is asserted, the next Clock transition that triggers a macrocell register will set the register's Q outputs to a logic high. If post-register inversion is used (active-low output), the macrocell's pin will be set to a logic low.

Programmable Output Enable

Each macrocell's Output Enable can place the output in a high-impedance state (tri-state). This output buffer is controlled by a single asynchronous product term per macrocell.

Power-On Characteristics

All EP22V10 device inputs and outputs respond a maximum of 1 µs after V_{CC} power-up (V_{CC} = 4.75 V) or after a power-down/power-up sequence. Macrocells programmed as registers are set to a logic low; output polarity is selected separately.

JEDEC File & Pin Compatibility

EP22V10 devices are 100% pin-, function-, and JEDEC File-compatible with industry-standard 22V10 devices. JEDEC Files developed for standard 22V10 architectures can be used to program EP22V10 and EP22V10E devices. EP22V10E devices maintain JEDEC File compatibility if none of the device's superset features are used.

EP22V10 devices in 28-pin PLCC packages offer additional VCC and GND pins (1, 8, 15, and 22). Industry-standard 22V10 designs leave these pins as No Connects (NC).

Figure 23 shows the typical supply current (I_{CC}) versus frequency for EP22V10 devices.

Figure 23. EP22V10 I_{CC} vs. Frequency

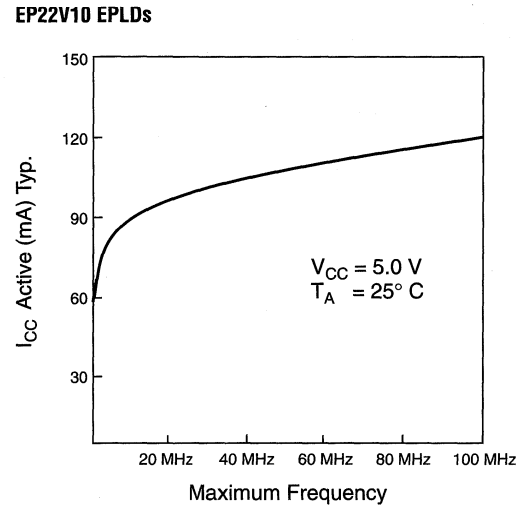
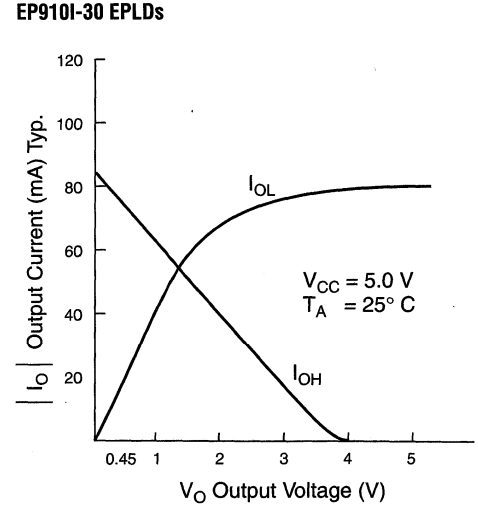


Figure 24 shows the output drive characteristics of EP22V10 I/O pins.

Figure 24. EP22V10 Output Drive Characteristics



Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	*Note (2)*	–2.0	7.0	V
V_I	DC input voltage	*Notes (2), (3)*	–0.5	V_{CC} + 0.5	V
T_{STG}	Storage temperature		–65	150	° C
T_{AMB}	Ambient temperature	*Note (4)*	–10	85	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	5.0-V operation	4.75	5.25	V
V_{IN}	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
t_R	Input rise time			5	ns
t_F	Input fall time			5	ns

DC Operating Conditions *Note (5)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage	*Note (2)*	2.0	V_{CC} + 0.3	V
V_{IL}	Low-level input voltage	*Note (2)*	–0.3	0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4.0 mA DC, V_{CC} = Min.	2.4		V
V_{OH}	High-level CMOS output voltage	I_{OH} = –100 µA, V_{CC} = Min.	V_{CC} – 0.3		V
V_{OL}	Low-level output voltage	I_{OL} = 16 mA DC, V_{CC} = Min.		0.45	V
I_I	Input leakage current	V_{CC} = Max., GND < V_{IN} < V_{CC}		10	µA
I_{OZ}	Tri-state output leakage current	V_{CC} = Max., GND < V_{OUT} < V_{CC}		10	µA
I_{SC}	Output short-circuit current	V_{CC} = Max., V_{OUT} = 0.5 V, *Note (7)*		120	mA

Capacitance

			EP22V10 EP22V10E		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		8	pF
C_{OUT}	I/O capacitance	V_{OUT} = 0 V, f = 1.0 MHz		8	pF
C_{CLK}	Clock pin capacitance, *Note (6)*	V_{IN} = 0 V, f = 1.0 MHz		17 (10)	pF

I_{CC} Supply Current *Note (8)*

			EP22V10 EP22V10E			
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
I_{CC3}	V_{CC} supply current	V_{CC} = Max., V_{IN} = V_{CC} or GND, no load, f_{IN} = 15 MHz, *Note (9)*		90	130	mA

Notes to tables:

(1) See *Operating Requirements for Altera Devices* in this data book.
(2) Voltage with respect to ground; all over- and undershoots due to system or tester noise are included.
(3) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods less than 20 ns under no load conditions.
(4) Under bias. Extended temperature versions are also available.
(5) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
(6) Value in parentheses is for EP22V10-7 device only.
(7) Test 1 output at a time; test duration should not exceed 1 second.
(8) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.
(9) Measured with device programmed as a 10-bit counter.

Combinatorial Mode AC Operating Conditions: EP22V10 & EP22V10E *Note (1)*

			EP22V10-7		EP22V10-10 EP22V10E-10		EP22V10-15 EP22V10E-15		EP22V10-25		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
t_{PD1}	Input to non-registered output, *Note (2)*	C1 = 50 pF		7.5		10		15		25	ns
t_{PD2}	I/O to non-registered output, *Note (2)*	C1 = 50 pF		7.5		10		15		25	ns
t_{PZX}	Input or I/O to output enable	C1 = 50 pF		9		10		15		25	ns
t_{PXZ}	Input or I/O to output disable	C1 = 5 pF		9		10		15		25	ns
t_{PCLR}	Input or I/O to asynchronous reset			10		15		20		20	ns

Register Mode Synchronous Clock AC Operating Conditions: EP22V10 & EP22V10E *Note (1)*

		EP22V10-7		EP22V10-10 EP22V10E-10		EP22V10-15 EP22V10E-15		EP22V10-25		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
f_{CNT1}	Maximum counter frequency, external feedback, *Note (3)*	111.1		95.2		64.5		35.7		MHz
f_{CNT2}	Maximum counter frequency, internal feedback, *Note (3)*	111.1		100		83.3		40		MHz
f_{MAX}	Maximum frequency (pipelined), no feedback	109.8		100		83.3		40		MHz
t_{SU}	Input or I/O setup time to global clock	3		3.5		7.5		14		ns
t_{SP}	Input or I/O setup time to synchronous preset	4.5		4.5		7.5		10.5		ns
t_{H}	Input or I/O hold time from global clock	0		0		0		0		ns
t_{CO1}	Global clock to output delay		6		7		8		14	ns
t_{CO2}	Global clock to output valid fed through combinatorial macrocell		13		16		18		30	ns
t_{CNT}	Minimum global clock period		13		10		12		25	ns
t_{CL}	Clock low time	4		4		5		10		ns
t_{CH}	Clock high time	4		4		5		10		ns
t_{CP}	Clock period	9.1		10		12		25		ns
t_{ARW}	Asynchronous reset pulse duration	4		4		5		5		ns
t_{ARR}	Asynchronous reset to global clock recovery time	7		7		9		10		ns

Notes to tables:

(1) Operating conditions: $V_{CC} = 5\ V \pm 5\%$, $T_A = 0°\ C$ to $70°\ C$ for commercial use.
$V_{CC} = 5\ V \pm 10\%$, $T_A = -40°\ C$ to $85°\ C$ for industrial use.

(2) Measured with all outputs switching.

(3) Measured with device configured as a 10-bit counter.

Configuration EPROM

Contents

March 1995

Configuration EPROM for FLEX 8000 Devices

Configuration EPROM
for FLEX 8000 Devices

March 1995, ver. 3 — Data Sheet

Features

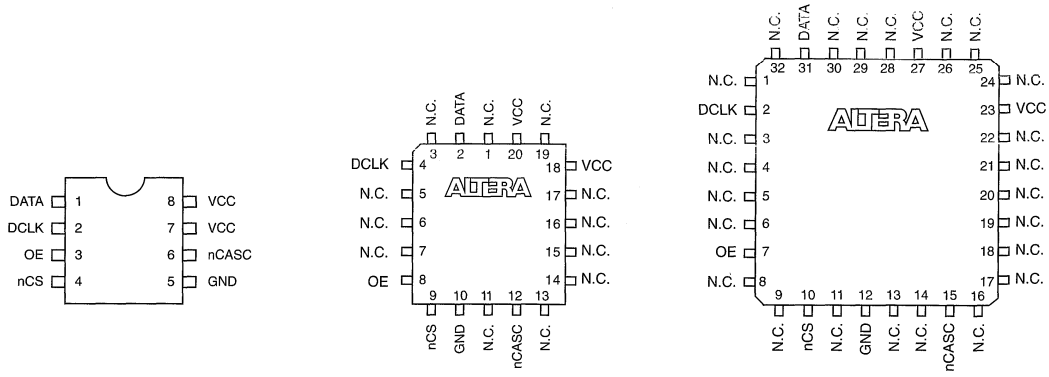
- Serial EPROM family designed to configure FLEX 8000 devices
- Simple 4-wire interface to FLEX 8000 devices for ease of use
- Low current during configuration (15 mA) and near-zero standby current (100 µA)
- Software design support with Altera's MAX+PLUS II development system for 486- and Pentium-based PCs, and Sun SPARCstation, HP 9000 Series 700, and IBM RISC System/6000 workstations
- Programming support with Altera's Master Programming Unit (MPU) and programming hardware from other manufacturers, including Data I/O
- Available in compact, one-time programmable (OTP) ceramic and plastic packages (see Figure 1):
  - 8-pin CerDIP
  - 8-pin PDIP
  - 20-pin PLCC
  - 32-pin TQFP

Functional Description

In SRAM-based devices, configuration data must be reloaded each time the system initializes, or whenever new configuration data is desired. Altera's serial Configuration EPROMs store configuration data for SRAM-based Altera FLEX 8000 devices.

Figure 1. Configuration EPROM Package Pin-Out Diagrams

Package outlines not drawn to scale.



8-Pin DIP

EPC1064
EPC1064V
EPC1213

20-Pin J-Lead

EPC1064
EPC1064V
EPC1213

32-Pin TQFP

EPC1064
EPC1064V

The EPC1064 and EPC1064V are 65,536 × 1 bit devices, and the EPC1213 is a 212,992 × 1 bit device. Table 1 shows the Configuration EPROM that is appropriate for each FLEX 8000 device.

Table 1. Typical Applications for Altera Configuration EPROMs

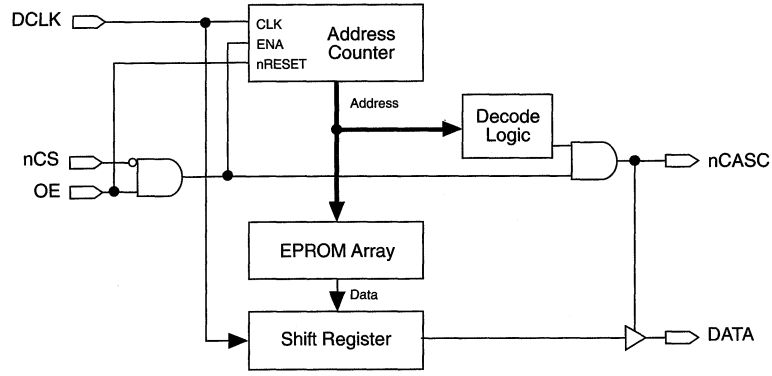
FLEX 8000 Device	Configuration EPROM
EPF8282, EPF8282A	EPC1064
EPF8282V, EPF8282AV	EPC1064V
EPF8452, EPF8452A	EPC1064
EPF8636A	EPC1213
EPF8820, EPF8820A	EPC1213
EPF81188, EPF81188A	EPC1213
EPF81500, EPF81500A	EPC1213, *Note (1)*

Note:
(1) The EPF81500 and EPF81500A require two EPC1213 devices for configuration.

Figure 2 shows a block diagram of the Configuration EPROM. Configuration data is stored in the EPROM array and clocked out serially by the DCLK input. The Output Enable (OE), Chip-Select (nCS), and Clock (DCLK) pins supply the control signals for the address counter and the output tri-state buffer. The device presents the configuration data as a serial bitstream on the DATA pin. This data is routed into the FLEX 8000 device via the DATA0 input pin. The nCASC pin provides handshaking between multiple Configuration EPROMs, so that a set of devices can be linked together to serially configure a large FLEX 8000 device or multiple FLEX 8000 devices.

Go to the *FLEX 8000 Programmable Logic Device Family Data Sheet* in this data book for more information on FLEX 8000 device architecture. Go to *Application Note 33 (Configuring FLEX 8000 Devices)* and *Application Note 38 (Configuring Multiple FLEX 8000 Devices)* in the ***FLEX 8000 Handbook*** for more information on FLEX 8000 device configuration.

Figure 2. Configuration EPROM Functional Block Diagram



The control signals for Configuration EPROMs (DCLK, nCS, and OE) interface directly to the FLEX 8000 device control signals. A FLEX 8000 device can control the entire configuration process and retrieve the configuration data from the Configuration EPROM without an external intelligent controller. The FLEX 8000 device can be set to configure automatically at system power-up by connecting nCONFIG to VCC.

The OE and nCS pins work together to control the tri-state buffer on the DATA output pin, and to enable the address counter in the Configuration EPROM. When OE is driven low, the device resets the address counter and tri-states the DATA pin. When the OE pin is driven high again, the device is controlled by the nCS pin. If nCS is held high after the OE reset pulse, the counter is disabled, and the DATA output pin is tri-stated. When nCS is driven low, the counter is enabled and the DATA output pin is enabled. The nCS pin can then be held either high or low to control the output and counter. When OE is driven low again, the address counter is reset and the DATA output pin is tri-stated regardless of the state of nCS.

When the Configuration EPROM has driven out all of its data and nCASC is driven low, it will tri-state the DATA pin to avoid contention with other Configuration EPROMs. Upon power-up, the address counter is automatically reset. Table 2 describes the pin functions of Altera Configuration EPROMs.

Table 2. Configuration EPROM Pin Functions

Pin Name	Pin Number			Pin Type	Description
	8-Pin PDIP	20-Pin PLCC	32-Pin TQFP		
DATA	1	2	31	Output	Serial data output.
DCLK	2	4	2	Input	Clock input. Rising edges on DCLK increment the internal address counter and cause the next bit of data to be presented on DATA. The counter is incremented only if the OE input is held high and the nCS input is held low.
OE	3	8	7	Input	Output Enable (active high) and Reset (active low). A low logic level resets the address counter. A high logic level enables DATA and permits the address counter to count.
nCS	4	9	10	Input	Chip-select input (active low). A low input allows DCLK to increment the address counter and enables DATA.
nCASC	6	12	15	Output	Cascade-select output (active low). This output goes low when the address counter has reached its maximum value. nCASC is usually connected to the nCS input of the next Configuration EPROM in a daisy-chain, so the next DCLK clocks data out of the next Configuration EPROM.
GND	5	10	12	Ground	A 0.2-µF decoupling capacitor must be placed between the VCC and GND pins.
VCC	7, 8	18, 20	23, 27	Power	Power pin.

Device Configuration

The active serial (AS) and multi-device sequential active serial (MD-SAS) configuration schemes use a Configuration EPROM (e.g., EPC1213) as a data source for a FLEX 8000 device.

For complete information on configuring FLEX 8000 devices, go to the *FLEX 8000 Programmable Logic Device Family Data Sheet* in this data book and *Application Note 33 (Configuring FLEX 8000 Devices)*, and *Application Note 38 (Configuring Multiple FLEX 8000 Devices)* in the ***FLEX 8000 Handbook***.

MAX+PLUS II Support

The MAX+PLUS II development system provides programming support for Altera Configuration EPROMs. The MAX+PLUS II software automatically generates a Programmer Object File (**.pof**) for every Configuration EPROM in a project. In a multi-device project, MAX+PLUS II can combine the programming files for multiple FLEX 8000 devices into one or more Configuration EPROMs. MAX+PLUS II selects the appropriate Configuration EPROM to most efficiently store the data for each FLEX 8000 device.

The POF includes a preamble, cyclic redundancy check (CRC), and synchronization data that allow it to be used in a serial bitstream. The POF is programmed into the Configuration EPROM with MAX+PLUS II and a Configuration EPROM programming adapter. A number of other programming hardware manufacturers, including Data I/O, support programming of Configuration EPROMs. See *Altera Programming Hardware* and *Programming Hardware Manufacturers* in this data book.

Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND, *Note (2)*	–2.0	7.0	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			20	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			100	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage for 5.0-V device		4.75	5.25	V
	Supply voltage for 3.3-V device		3.0	3.6	V
V_I	Input voltage	With respect to GND, *Note (2)*	0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			20	ns
t_F	Input fall time			20	ns

DC Operating Conditions *Notes (3), (4)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage		2.0	V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
V_{OH}	5.0-V device high-level TTL output voltage	I_{OH} = –4 mA DC	2.4		V
	3.3-V device high-level TTL output voltage	I_{OH} = –0.1 mA DC	V_{CC} – 0.2		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC		0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	–10	10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CC} or GND	–10	10	µA

Supply Current

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC0}	V_{CC} supply current (standby)			100		µA
I_{CC1}	V_{CC} supply current (during configuration)	DCLK = 6 MHz		10		mA

Capacitance *Note (5)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF

Timing Parameters

			EPC1064V		EPC1064 EPC1213		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Unit
t_{OEZX}	OE high to DATA output enabled			75		50	ns
t_{CSZX}	nCS low to DATA output enabled			75		50	ns
t_{CSXZ}	nCS high to DATA output disabled			75		50	ns
t_{CSS}	nCS low setup time to first DCLK rising edge		150		100		ns
t_{CSH}	nCS low hold time after DCLK rising edge		0		0		ns
t_{DSU}	Data setup time before rising edge on DCLK, *Note (6)*		75		50		ns
t_{DH}	Data hold time after rising edge on DCLK, *Note (6)*		0		0		ns
t_{CO}	DCLK to DATA out delay, *Note (7)*			100		75	ns
t_{CK}	Clock period		240		160		ns
f_{CK}	Clock frequency			4		6	MHz
t_{CL}	DCLK low time		120		80		ns
t_{CH}	DCLK high time		120		80		ns
t_{XZ}	OE low or nCS high to DATA output disabled			75		50	ns
t_{OEW}	OE pulse width to guarantee counter reset		150		100		ns
t_{CASC}	Last DCLK + 1 to nCASC low delay			90		60	ns
t_{CKXZ}	Last DCLK + 1 to DATA tri-state delay			75		50	ns
t_{CEOUT}	nCS high to nCASC high delay			150		100	ns

Notes to tables:

(1) See *Operating Requirements for Altera Devices* in this data book.

(2) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.

(3) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.

(4) Operating conditions: V_{CC} = 5.0 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5.0 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5.0 V ± 10%, T_A = –55° C to 125° C for military use.

(5) Capacitance is sample-tested only.

(6) This parameter applies to the FLEX 8000 device.

(7) Eight Clock cycles are required after the t_{CSS} setup time has been met to clock out the first eight bits. These bits are all high and are used to synchronize the configuration process. The ninth Clock cycle presents the first configuration data bit.

Notes:

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Military Products


ALTERA
FLEX®
EPF81188GM883B
ALTERA
FLEX®
EPF8820WM883B
ALTERA
MAX®
EPM7256EWM883B
ALTERA
MAX®
EPM7192EGM883B

Military Products

March 1995, ver. 4 — Data Sheet

Introduction

Altera's military devices are manufactured with advanced CMOS technology to provide an optimum combination of reliability, speed, density, and low power consumption. Altera offers military devices that meet military-temperature-range, MIL-STD-883, and DESC requirements. These military devices use the same wafer fabrication processes as Altera's commercial devices. This data sheet discusses product availability and MIL-STD-883 compliance.

Product Availability

Table 1 provides information on military-temperature-range, MIL-STD-883-qualified, and DESC devices. For detailed device information, refer to the appropriate data sheets in this data book or to DESC Standard Microcircuit Drawings (SMDs). For more information on Altera's military products, contact Altera Marketing at (408) 894-7104.

Table 1. Altera Military-Temperature-Range, MIL-STD-883-Compliant & DESC Devices

Device	MIL-STD-883-Compliant	Package	Speed (ns)	DESC Order Number
EP600I	✓	CerDIP	t_{PD1} = 55	5962-8686401LA
EP610	✓	CerDIP	t_{PD1} = 35	5962-8947601LA
EP910		CerDIP	t_{PD1} = 40	
EP910		JLCC	t_{PD1} = 40	
EP1800I	✓	PGA	t_{PD1} = 90	5962-8854901XA
EP1810	✓	PGA	t_{PD1} = 45	5962-8946901YC
EP1810		JLCC	t_{PD1} = 45	
EPM5032	✓	CerDIP	t_{PD1} = 25	5962-9061102XA
EPM5032		JLCC	t_{PD1} = 25	
EPM5064		JLCC	t_{PD1} = 35	
EPM5128	✓	PGA	t_{PD1} = 20	5962-8946804XC
EPM5128	✓	PGA	t_{PD1} = 30	
EPM5128	✓	PGA	t_{PD1} = 35	5962-8946801XC
EPM5128		JLCC	t_{PD1} = 30	
EPM5128		JLCC	t_{PD1} = 35	
EPM5130	✓	PGA	t_{PD1} = 30	5962-9314402MZC
EPM5130	✓	PGA	t_{PD1} = 35	5962-9314401MZC
EPM5130		JLCC	t_{PD1} = 35	
EPM5130	✓	CQFP	t_{PD1} = 30	5962-9314402MXA
EPM5130	✓	CQFP	t_{PD1} = 35	5962-9314401MXA
EPM5192	✓	PGA	t_{PD1} = 30	5962-9206202MYC
EPM5192	✓	PGA	t_{PD1} = 35	5962-9206201MYC
EPM7192E	✓	PGA	t_{PD1} = 15	5962-9316802MXC
EPM7192E	✓	PGA	t_{PD1} = 20	5962-9316801MXC
EPM7256E	✓	PGA	t_{PD1} = 15	5962-9324702MXC
EPM7256E	✓	PGA	t_{PD1} = 20	5962-9324701MXC
EPM7256E	✓	CQFP	t_{PD1} = 15	5962-9324702MYA
EPM7256E	✓	CQFP	t_{PD1} = 20	5962-9324701MYA
EPF8820A	Consult factory	PGA	t_{DRR} = 25.0	Consult factory
EPF8820A	Consult factory	CQFP	t_{DRR} = 25.0	Consult factory
EPF8820	✓	PGA	t_{DRR} = 38.3	5962-9463401MXC
EPF8820	✓	CQFP	t_{DRR} = 38.3	5962-9463401MYA
EPF81188A	Consult factory	PGA	t_{DRR} = 25.0	Consult factory
EPF81188	✓	PGA	t_{DRR} = 38.3	5962-9473301MXC
EPC1213	✓	CerDIP	–	5962-9474501MPA

MIL-STD-883 Qualification Flow

MIL-STD-883-compliant device specifications are provided in DESC Standard Microcircuit Drawings (SMDs). When DESC SMDs are not available, Source Control Drawings (SCDs) are generated for Altera's commercial devices that are or will be qualified for MIL-STD-883. SCDs are also used for document control. An SCD should be based on a Military Product Drawing (MPD) provided by Altera. When an MPD is not available, contact Altera Marketing for current data.

Altera MPDs contain information on the scope, reference documents, MIL-STD-883 requirements, quality assurance provisions, and delivery requirements for devices. Characteristics of device screening—such as burn-in testing, AC/DC electrical properties, timing waveforms, and package dimensions—are also detailed in MPDs. These specifications may differ from those for Altera's commercially rated devices. Altera does not approve an SCD until the described MPD requirements are met. Figure 1 shows the process for generating an SCD for Altera's military products.

Figure 1. Source Control Drawing (SCD) Generation Process

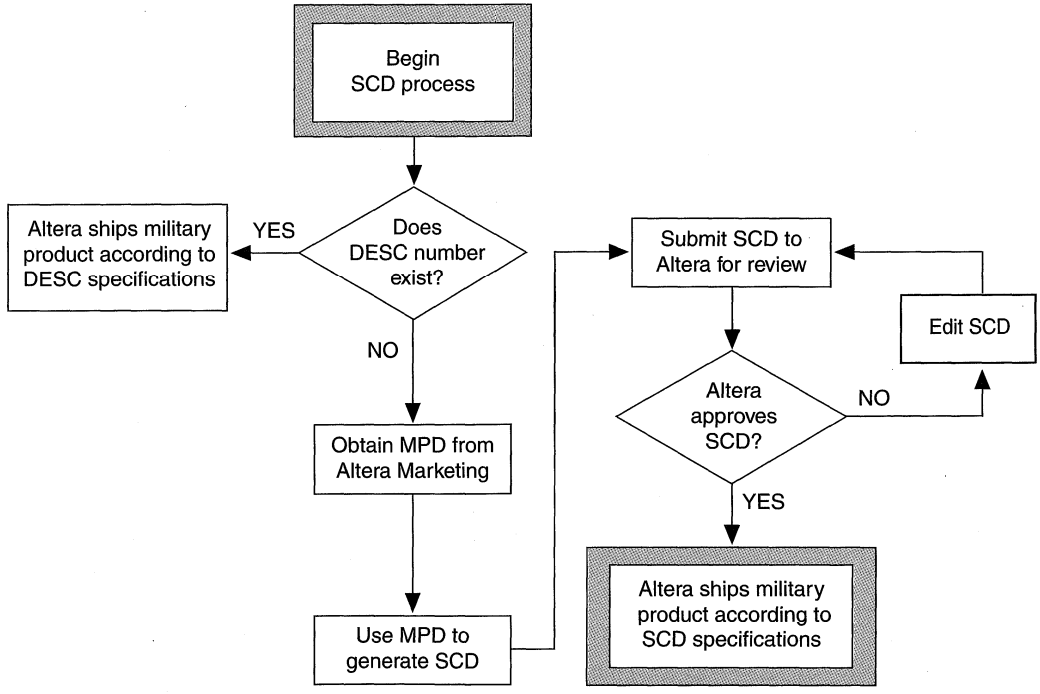
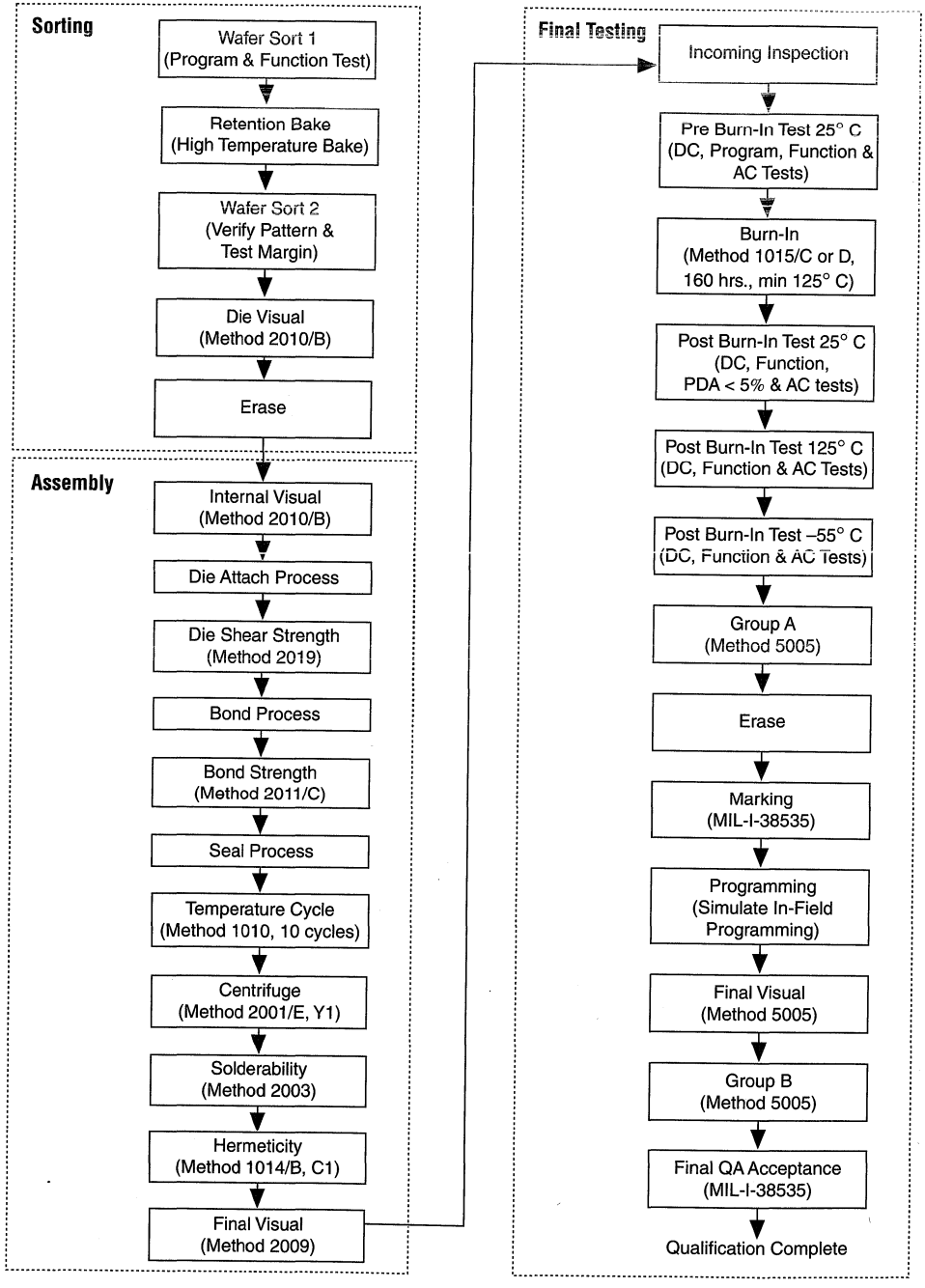


Figure 2 shows the process for MIL-STD-883-compliant Altera devices.

Figure 2. MIL-STD-883 Qualification Flow



March 1995

Mask-Programmed Logic Devices


ALTERA
MPF81500AMC304
ALTERA
MPF81188AMC240
ALTERA
MPM9560MC304

MPLDs

Mask-Programmed Logic Devices

March 1995, ver. 3 Data Sheet

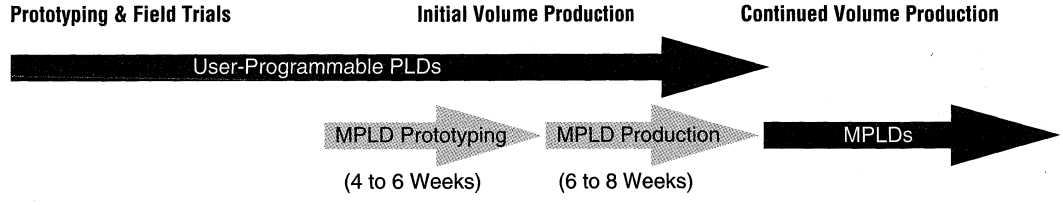
Features

- Masked versions of Altera programmable logic devices (PLDs)
- Reduced cost for high-volume production
- Available for all Altera devices
- Pin-, function-, and timing-compatible with original device
- Conversion process handled by Altera
- Fast turn-around to shorten time-to-market
- Low power consumption

General Description

Altera Mask-Programmed Logic Devices (MPLDs) provide a masked alternative to PLDs. By using a generic CMOS process and removing all programmable cells, Altera passes considerable savings on to customers who anticipate high-volume production. In addition, Altera handles the PLD-to-MPLD conversion so that no customer redesign effort is required. The combination of Altera PLDs and MPLDs provides the best of both worlds: the fast time-to-market of programmable devices, and the low cost of MPLDs. See Figure 1.

Figure 1. High-Volume Production Flow with Altera PLDs & MPLDs



MPLD Compatibility

Each Altera MPLD is pin-, function-, and timing-compatible with the original PLD. This compatibility ensures that the MPLD can replace the original Altera device, while providing lower cost and maintaining the production flow. In addition, the MPLD typically consumes less power than the equivalent programmable device, depending on the design and operating conditions.

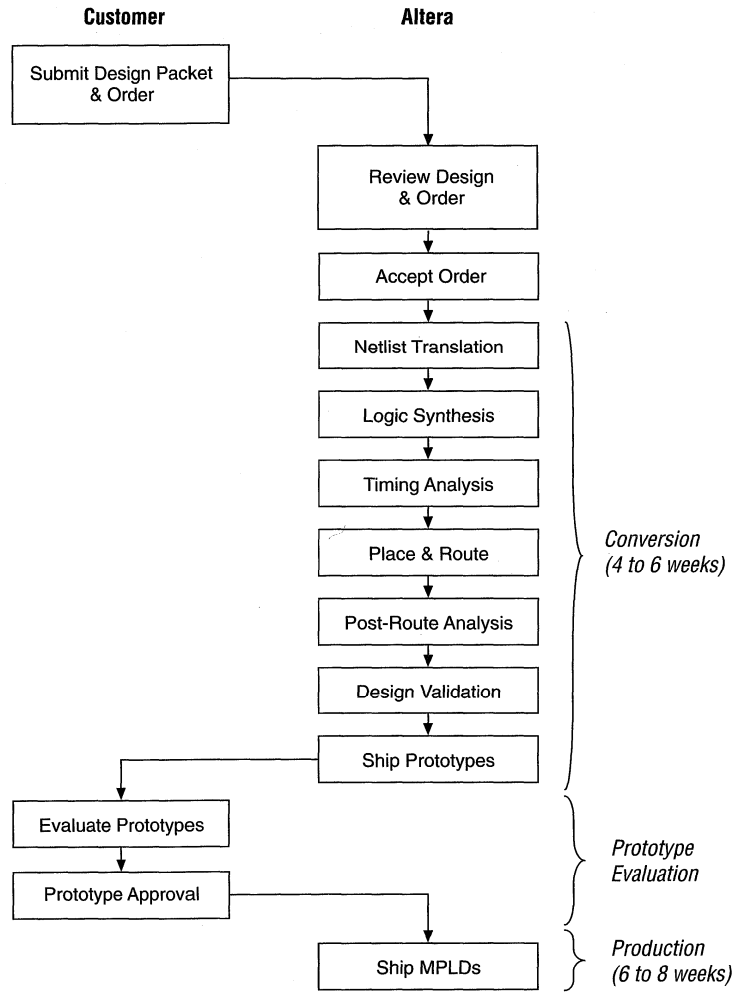
Pin compatibility guarantees that both the pin-out and DC specifications of the MPLD match those of the original device. Altera ensures functional compatibility by mapping the logic within the PLD (e.g., product terms, programmable flipflops, etc.) directly to specially designed elements within the MPLD. Altera's proprietary logic synthesis program uses netlist files generated by MAX+PLUS II software to describe the final synthesis, placement, and routing of the original design. The conversion process accounts for all architecture-specific features—such as wide fan-in product terms, carry chains, and cascade chains—commonly found in programmable logic applications.

Quick, Seamless Conversion

One of the principal objectives of Altera's MPLD conversion program is to minimize the design engineer's time and resource investment in the conversion. The engineer simply submits design files created with MAX+PLUS II software and Altera delivers MPLDs within weeks of the design sign-off.

The MPLD conversion flow chart (see Figure 2) shows how easily a programmable Altera device can be converted into an MPLD.

Figure 2. MPLD Conversion Flow



Go to the *MPLD Conversion Information & Order Forms* workbook, which can be obtained from an Altera sales representative, for the instructions and forms necessary to initiate the PLD-to-MPLD conversion.

The design conversion includes netlist translation, logic synthesis, testability insertion, timing analysis, place-and-route, post-route timing analysis, design validation, and the prototype manufacturing. The entire conversion process, from order acceptance to prototype delivery, takes 4 to 6 weeks. Production quantities are delivered 6 to 8 weeks after the customer returns the *Prototype Approval Form* included in the ***MPLD Conversion Information & Order Forms*** workbook.

Conclusion

The two most important design goals for engineers today are reducing time-to-market and minimizing system cost. Together, Altera PLDs and MPLDs provide a solution that addresses these concerns, allowing a company to take a product to market quickly, lower the end-product cost, and eliminate the risks associated with ASIC design conversions.

Device Operation

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Appication Brief 119: High-Speed Board Designs

Application Brief 100: Understanding Classic, MAX 5000 & MAX 7000 Timing

Application Brief 143: Understanding FLEX 8000 Timing

Application Brief 144: Understanding MAX 9000 Timing

Operating Requirements
for Altera Devices

March 1995, ver. 6 Data Sheet

Introduction

Altera devices combine unique programmable logic architectures with advanced CMOS processes to provide exceptional performance and reliability. To maintain the highest possible performance and reliability of Altera devices, system designers must consider the following operating requirements:

- Operating conditions
- Pin voltage levels
- Output loading
- Power-supply management
- Thermal analysis
- Thermal management
- Device erasure

Operating Conditions

Altera devices are rated according to a set of defined parameters, which must be considered when a device is implemented in a system. These parameters are provided in each device data sheet and include absolute maximum ratings, recommended operating conditions, and DC and AC operating conditions.

Absolute Maximum Ratings

Absolute maximum ratings define the limits of the conditions that a particular Altera device can withstand. These values are based on experiments conducted with Altera devices, as well as on theoretical modeling of breakdown and damage mechanisms. These ratings are stress ratings only. Functional operation of devices at these conditions or at conditions beyond those indicated in the "Recommended Operating Conditions" tables in the device data sheets in this data book is not implied. For example, I_{OUT} is the absolute current capacity, not the drive capability of an output pin. The output source and sink currents are given as I_{OH} and I_{OL} in the "DC Operating Conditions" section of each device data sheet.

Operating an Altera device at conditions listed in the "Absolute Maximum Ratings" table in a device data sheet for extended periods of time may impair device reliability. Operating the device at conditions that exceed these ratings may cause permanent damage to the device.

Recommended Operating Conditions

The functional operation limits for an Altera device, given in the "Recommended Operating Conditions" table in a device data sheet, specify limits under which all AC and DC parameters are guaranteed. These parameters may be expressed differently in other rating sections. For example, the V_{CC} range specified in the "Recommended Operating Conditions" table is the voltage range over which the AC and DC operating conditions are guaranteed, while the V_{CC} range specified in the "Absolute Maximum Ratings" table is the power-supply level beyond which the device may be permanently damaged.

DC Operating Conditions

The steady-state voltage and current values expected from an Altera device are provided in the "DC Operating Conditions" table in a device data sheet. This information includes input voltage sensitivities (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), current drive capability (I_{OH} and I_{OL}), and input and output leakage currents (I_I and I_{OZ}). The values are guaranteed for DC operation under the conditions specified in each device data sheet.

AC Operating Conditions

The external and internal timing parameters for an Altera device are given in the "AC Operating Conditions" table(s) in a device data sheet. These parameters are determined under the conditions specified in the "Recommended Operating Conditions" table. The external timing parameters are guaranteed pin-to-pin delays when the device is operating under these conditions. Internal timing parameters are the delays associated with specific architectural features and can be combined to estimate device performance.

Timing parameters are specified as maximum, minimum, or typical values. A maximum value indicates that the delay will not exceed the specified time. Setup, hold, and pulse width times are expressed as minimum values that the system must provide to ensure reliable device operation.

Pin Voltage Levels

Device pins can be exposed to dangerous voltages during handling or device operation. During handling, pins can be exposed to high-voltage static discharges that cause electrostatic discharge (ESD) damage. During operation, power-supply spikes on the VCC and GND pins or errant logic levels elsewhere in the system can produce logic-level stress with voltages similar to V_{CC} (0 V to 15 V). To minimize these hazards, the user must observe the precautions specified for the following conditions:

- Pin connections
- Latch-up
- Hot-socketing
- Electrostatic discharge

Pin Connections

During project compilation, the MAX+PLUS II software generates a device utilization report, called a Report File (**.rpt**), that provides information on the pin-outs and connectivity of the device(s) used in the project. The Report File includes a pin-out diagram that shows the user signal pins, VCC and GND pins, and reserved pins.

The VCC and GND pins should be tied to the V_{CC} or GND planes, respectively, on the printed circuit board (PCB). Dedicated input pins used in a design and I/O pins configured as inputs should always be driven by an active source. I/O pins configured as bidirectional pins should always be driven whenever the I/O pin is used as an input. Unused dedicated input and I/O pins are marked in the Report File as GND and RESERVED, respectively. Unused dedicated inputs should be tied to the GND plane. Otherwise, these pins may "float" in an indeterminate state, possibly increasing DC current in the device and introducing noise into the system. Since RESERVED I/O pins are driven by active signals representing the buried logic present in the logic cell associated with that particular pin, RESERVED I/O pins should remain unconnected. Tying a RESERVED I/O pin to V_{CC}, GND, or another signal source creates contention that may damage the output driver on the device.

For proper operation, signals on the input and output pins must be in the following range:

$$GND \leq (V_{IN} \textit{ or } V_{OUT}) \leq V_{CC}$$

Latch-Up

Parasitic bipolar transistors, which are present in the fundamental structure of CMOS devices, can create paths for dangerous currents in the device. Typically, the base-emitter and base-collector junctions of these parasitic transistors are not forward-biased, so they are not turned on. Figure 1 shows a cross-section of a CMOS wafer and primary parasitic transistors. To ensure that all junctions remain reverse-biased, the P-type substrate is connected to the most negative voltage available on-chip (GND), and the N-type well structure is connected to the most positive voltage on-chip (V_{CC}).

Figure 1. Parasitic Bipolar Transistors in CMOS Devices

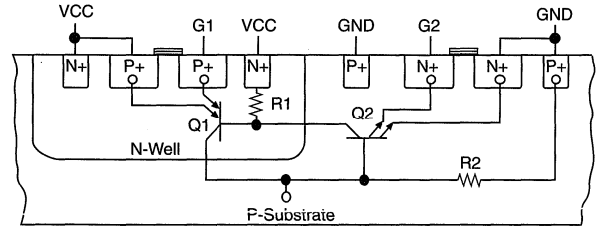


Figure 1 also shows the parasitic resistors that occur in the CMOS structure. Generally, these resistors are of no concern as long as currents do not flow through the structure laterally. However, I-R drops may occur in the structure if any of the associated diodes are turned on. These diodes may be initially turned on by power-supply or I/O pin transients that exceed the limits of GND and V_{CC}. These transients can be induced by signal ringing and other inductive effects in the system.

Catastrophic failure can occur if these parasitic structures begin to conduct, since the effect is regenerative and reinforces itself until potentially destructive currents are produced. This silicon-controlled rectifier (SCR) effect is called "latch-up." As the current flows through the parasitic transistor, the I-R drop through the resistor increases, further forward-biasing the base-emitter junction. The cycle continues until the current is limited by drops in the primary current path. At this point, the current may have reached a level that permanently damages internal circuitry.

Altera devices have been designed to minimize the effects of latch-up that is caused by power-supply and I/O pin transients. Under recommended operating conditions, all devices are guaranteed to withstand input voltage extremes of between GND – 1 V and V_{CC} + 1 V, as well as input currents of 100 mA or less that are forced through the device pins.

To minimize the chances of inducing latch-up during power-up, GND should be applied to the device first, then V_{CC}, and finally the inputs. The power should be removed from the device in the reverse order: first, the inputs are removed, then V_{CC}, and finally GND.

Simultaneous application of inputs and V_{CC} to the device, which may occur as a power supply rises during power up, should be safe as long as V_{CC} meets the maximum rise time. The designer should ensure that the inputs cannot rise faster than the supply at the VCC pin(s).

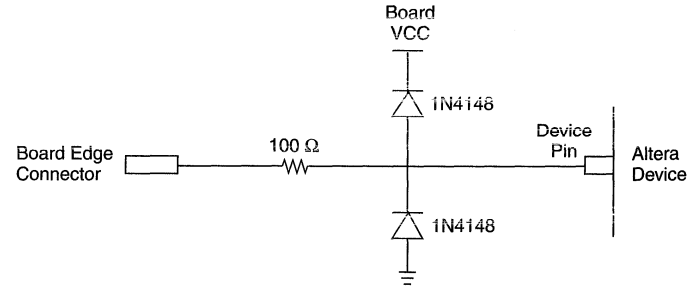
Hot-Socketing

Latch-up frequently occurs when electrical subsystems are plugged into active hardware, i.e., "hot-socketed." When a subsystem is hot-socketed, the logic levels often appear at the subsystem's logic devices before the power supply can provide current to the V_{CC} and GND grid of the subsystem board. This condition may lead to latch-up.

Increasing the length of the V_{CC} and GND connections can reduce the chances of latch-up during hot-socketing. If metal "fingers" are used for the board connection, the V_{CC} and GND fingers at the card edge should be longer than the logic connections. This difference in length causes the power supply to appear at the device before the logic levels, and is usually sufficient to prevent latch-up. Off-the-shelf connectors with longer V_{CC} and GND connections can provide similar results.

Implementing the circuitry shown in Figure 2 also provides protection against latch-up during hot-socketing. The diode structure provides a "clamp" level on the input voltage, preventing it from swinging more than one diode-drop away from a power rail (–0.6 V to V_{CC} + 0.6 V). The series resistor also reduces the possibility of latch-up by restricting the current to the device input and clamp diodes. This circuitry provides the maximum protection against latch-up, but is usually required only if the input on the device is tied directly to the edge connector. Device inputs that are driven by other circuit elements in the subsystem are generally safe from latch-up, since these elements provide a natural delay before the logic levels are established.

Figure 2. Hot-Socket Protection



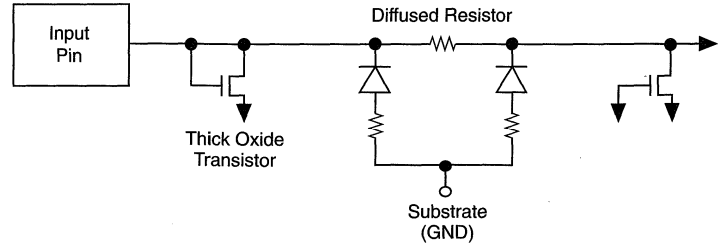
Electrostatic Discharge

Electrostatic discharge (ESD) resulting from improper device handling can cause device failure that may not manifest itself for a long period of time. Although ESD damage may result in immediate device failure, it more frequently affects the long-term reliability of the device.

Device handling during the programming cycle increases exposure to potential static-induced failure. During normal activity, the human body can generate voltages of up to tens of kilovolts (kV). Wearing ground straps during device handling and grounding all surfaces that come in contact with components reduces the likelihood of damage. Synthetic materials used in clothing can store large amounts of static electricity and may also cause ESD.

Altera devices include special structures that reduce the effects of ESD at the pins. Figure 3 shows a typical input structure for an Altera device. Diode structures and specialized field-effect transistors shunt harmful voltages to ground before destructive currents can flow. Most Altera devices can withstand ESD voltages greater than 2 kV, but all devices are guaranteed to withstand ESD voltages greater than 1 kV.

Figure 3. Altera Device Input Protection Structure



Output Loading

Output loading is typically resistive and/or capacitive. During development, the designer should ensure that the target device can supply both the current and speed necessary for the loads.

Resistive Loading

Resistive loading exists whenever a device output sinks or sources a current in a steady state. Examples of resistive loading include devices with TTL inputs, terminated buses, and discrete bipolar transistors.

Output current capabilities (I_{OH} and I_{OL}), which are functions of output voltages (V_{OH} and V_{OL}), are given in the data sheet for each device. In a DC condition, output current capabilities determine the maximum resistivity of a load while still maintaining the necessary output voltage. If the system requires higher currents, such as those necessary to drive an LED or a relay, a high-current buffer or a discrete current switch must be used.

Short-circuit conditions—where I_{OH} and I_{OL} exceed the absolute maximum rating (I_{OUT})—can permanently damage the device.

Capacitive Loading

The "AC Operating Conditions" table in a device data sheet specifies an output capacitance condition (C1) for parameters relating to external performance. For most Altera devices, C1 is 35 pF for active signals and 5 pF for high-impedance parameters.

Device packages and board-level trace capacitance contribute the majority of loading capacitance. (An insignificant amount of the total capacitance on output buffers is attributable to the gate capacitance of CMOS device inputs.) The specified 35-pF load condition is a representative value for most CMOS circuits. For applications in which a device drives a higher capacitance, performance decreases as the capacitive load increases.

Device sockets are a source of both capacitive and inductive loading. Once a system is finalized for production, sockets should be removed if possible, and the devices should be mounted directly onto the PCB. Direct board mounting reduces both the capacitive load and noise from socket contacts.

To ensure the highest circuit performance, the capacitance on device outputs should be minimized. Since wiring traces on the PCB, device input pins, and device packaging all contribute to the total capacitance, the following guidelines should be observed:

- Board layout should ensure that signals run perpendicular to each other to provide a minimum capacitive coupling effect. Also, signal traces should be kept as short as possible.
- A high-current buffer should be used to speed the signal to all destinations for networks in which a single source drives many loads.

The lack of V_{CC} and GND planes or excessive trace lengths may cause problems with radiated coupling of noise into logic signals and transmission-line effects on signal quality. These ringing and noise elements on logic levels can lead to circuit reliability problems. When recommended layout practices cannot be implemented to prevent transmission-line problems, a small series resistance (10 Ω to 30 Ω) can be used to reduce the magnitude of undershoot and overshoot on signal edges. This resistance dampens the ringing that can occur on long board traces and prevents false triggering.

Power-Supply Management

Although Altera devices are designed to minimize noise generation and susceptibility, they—like all CMOS devices—can be sensitive to fluctuations in power supply and input lines. To minimize the effect of these fluctuations, the system designer must pay special attention to:

- V_{CC} and GND planes
- Decoupling capacitors
- V_{CC} rise time
- Current dissipation

V_{CC} & GND Planes

The system designer can minimize power-supply noise or "ground bounce" by providing separate V_{CC} and GND planes for every PCB, thus ensuring a near-infinite current-sink capability, noise protection, and shielding for logic signals on the board. If an entire plane cannot be provided, the widest possible GND and V_{CC} traces should be created throughout the entire board. Logic-width traces should not be used to carry the power supply. Although V_{CC} and GND planes tend to increase the capacitive load of the traces, they significantly reduce system noise, and dramatically increase system reliability.

Decoupling Capacitors

Each VCC and GND pin should be connected directly to the V_{CC} and GND planes in the PCB. Each pair of VCC and GND pins should be decoupled with a 0.2-µF power-supply decoupling capacitor, located as close as possible to the Altera device. For devices with a very large number of VCC and GND pins—i.e., more than 8 pairs of each—it may not be necessary to provide a decoupling capacitor for every pair. Decoupling requirements are based on the amount of logic used in the device, the frequency of operation, and the output switching requirements. As the number of I/Os and the switching frequency increase, more decoupling capacitance is required. The ideal solution is to provide a capacitor for every VCC/GND pair, which will decouple the device for any logic utilization or operating frequency. For less dense or slower designs, a reduction in the number of capacitors may be acceptable. For example, the EPM7192E has 14 VCC/GND pairs. In general, 8 decoupling capacitors are sufficient for most designs. Decoupling capacitors should have a good frequency response, like that of monolithic-ceramic capacitors.

Every PCB should also have a large-capacity, general-purpose, electrolytic capacitor network to stabilize the power supply. A 100-µF capacitor should be placed immediately adjacent to the location where the power-supply lines come into the PCB. If a transformer or regulator is used to change the voltage level, the capacitor should be placed immediately after the final stage that develops the device's V_{CC} supply. This capacitor provides a beneficial leveling effect that supplies extra current when a large number of nodes switch simultaneously in a circuit. However, the larger the power supply capacitor, the longer the time required to bring the maximum V_{CC} to the operating level. The size of the capacitor must not force the V_{CC} rise time to violate the maximum rise time, as discussed in "V_{CC} Rise Time. "

V_{CC} Rise Time

When power is applied to an Altera device, the device initiates a Power-On Reset (POR), typically as V_{CC} approaches 1.5 V to 2.0 V. The POR event occurs only if V_{CC} reaches the recommended operating range within a certain period of time (specified as a maximum V_{CC} rise time). Slower rise times can cause incorrect device initialization and functional failure. The maximum V_{CC} rise times for Altera devices are provided in Table 1.

Table 1. Maximum V_{CC} Rise Time for Altera Devices

Device	Time
EP610, EP910, EP1810	50 ms
EP610I, EP910I	Unlimited (V_{CC} must be monotonic)
EP22V10, EP22V10E	Unlimited (V_{CC} must be monotonic)
MAX 5000 (single-LAB)	10 ms
MAX 5000 (multi-LAB), MAX 5000A	200 ms
FLASHlogic	Unlimited (V_{CC} must be monotonic)
MAX 7000, MAX 7000E, MAX 7000S	Unlimited (V_{CC} must be monotonic)
FLEX 8000	100 ms *Note (1)*
MAX 9000	Unlimited (V_{CC} must be monotonic)

Note:

(1) The V_{CC} rise time for FLEX 8000 devices may exceed 100 ms if the Configuration EPROM or parallel EPROM is powered up before the FLEX 8000 device.

The POR time is the time required after V_{CC} reaches the recommended operating range to clear device registers, configure I/O pins, and release tri-states. Once this initialization is complete, the device is ready to begin logic operation. The POR time does not exceed 50 ms.

Current Dissipation

Every Altera device is designed to consume the least possible amount of power while providing high performance. Since these two design goals can conflict with each other, Altera devices and software tools allow designers to monitor and control the current with built-in device features.

MAX 7000 and MAX 9000 macrocells can be individually configured for high performance or low power during design entry. Turning on the macrocell's Turbo Bit allows the macrocell to function in a high-performance mode at the specified device ratings. If the Turbo Bit is turned off, the macrocell's built-in power-saving mode trades higher performance for lower current consumption.

MAX 7000 and MAX 9000 devices operating in low-power mode consume less current. The supply current (I_{CC}) can be reduced by approximately 50%, depending on the design and operating frequency. The *MAX 7000 Programmable Logic Device Family* and the *MAX 9000 Programmable Logic Device Family* data sheets provide graphs that show the relationship between I_{CC} and frequency. For a device with the Turbo Bit option, the graph provides two curves; one showing I_{CC} versus frequency when all macrocells have their Turbo Bits turned on, the other with all Turbo Bits off. Since most designs use a combination of turbo and non-turbo macrocells, a formula that accounts for this ratio and the frequency of operation is also provided with the graph. The values shown in the graph and formula are measured with no output loads and represent only the current consumed by device operation.

Many Classic devices also have a Turbo Bit option. A Classic device operating in low-power mode enters a standby mode after 100 ns of inactivity (i.e., when no inputs or outputs have changed). An input signal transition "wakes" the device, which then performs normally until the next standby mode period. However, the input signal incurs an additional delay—specified as the non-turbo delay adder in device data sheets—as it wakes and propagates through the device.

Thermal Analysis

A critical element of system reliability is the capacity of electronic devices to safely dissipate the heat generated during operation. The thermal characteristics of a circuit depend on the device and package used, the operating temperature, the operating current, and the system's ability to dissipate heat.

Thermal analysis should be completed early in the design process to help identify potential heat-related problems in the system and prevent the system from exceeding the device's maximum allowed junction temperature. To perform a thermal analysis, the designer must:

1. Estimate power consumption of the application.
2. Calculate the maximum allowed power for the device and package.
3. Compare the estimated and maximum allowed power values.

In most applications, the power dissipated is significantly lower than the maximum allowed. However, this type of analysis should be performed for all projects. Several steps that can correct temperature-related problems are described later in this data sheet.

Estimating Power Consumption

The following formula should be used to estimate the maximum supply current (I_{CC}):

Estimated maximum I_{CC} = no-load I_{CC} + $I_{CCDCOUT}$ + $I_{CCACOUT}$

The no-load I_{CC} can be obtained from the I_{CC} vs. frequency graph provided in the device data sheet. Since this value is "unloaded," it is necessary to add the $I_{CCDCOUT}$ from steady-state outputs and the $I_{CCACOUT}$ current from frequently switching outputs. $I_{CCDCOUT}$ depends on the number of steady-state outputs, the logic levels they drive, and the resistive load on each output, as shown in the following formula:

$$I_{CCDCOUT} = \sum_{n=1}^{d} \frac{V_{On}}{R_n}$$

In this formula, d is the number of DC outputs, V_{On} is the DC output voltage of output n, and R_n is the resistive load driven by output n.

$I_{CCACOUT}$ depends on the capacitive load on each output and the frequency at which each output switches, as shown in the following formula:

$$I_{CCACOUT} = \sum_{n=1}^{a} C_n V_n f_n$$

In this formula, a is the number of AC outputs, C_n is the capacitive load on output n, V_n is the voltage swing of output n, and f_n is the switching frequency of output n.

The estimated maximum I_{CC} is used together with the following formula to estimate the maximum power (P_{EST}):

P_{EST} = estimated maximum $I_{CC} \times V_{CC}$

The actual I_{CC} should be measured after the project is completed to verify P_{EST}.

Calculating Maximum Allowed Power for the Device & Package

The following formulas are used to calculate the maximum allowed power (P_{MAX}) for a device:

$$P_{MAX} = \frac{150°C - T_A}{\theta_{JA}} \quad or \quad P_{MAX} = \frac{150°C - T_C}{\theta_{JC}}$$

The maximum allowable power is dependent on the maximum allowable junction temperature of the silicon, the ambient temperature of operation (T_A), and the package's thermal resistance (θ) when configured in the system. The maximum junction temperature is specified as 150° C. The ambient temperature depends on the application. The worst-case P_{MAX} value is estimated using the formula with θ_{JA}, the junction-to-ambient thermal resistance. θ_{JA} is a measure of the worst-case thermal resistance for a device in still air, with convection cooling only. If forced-air flow and heat-sinking are used to dissipate heat, the designer should use the case temperature (T_C) and the junction-to-case thermal resistance (θ_{JC}) to calculate P_{MAX} for a device. θ_{JC} is a measure of the lowest possible thermal resistance.

Tables 2 through 5 provide θ_{JA} and θ_{JC} values for Altera Classic, MAX 5000, MAX 7000, and FLEX 8000 devices.

Table 2. Thermal Resistance of Classic Devices

Device	Pin Count	Package	θ_{JC} (° C/W)	θ_{JA} (° C/W)
EP330	20	PDIP	19	68
		SOIC	17	88
EP610	24	CerDIP	10	60
EP610T		PDIP	18	55
		SOIC	17	77
	28	JLCC	12	90
		PLCC	13	74
EP610I	24	CerDIP	18	60
		PDIP	22	67
	28	PLCC	16	64
EP910	40	CerDIP	12	40
EP910T		PDIP	23	49
	44	JLCC	5	67
		PLCC	10	58
EP910I	40	CerDIP	17	44
		PDIP	29	51
	44	PLCC	16	55
EP1810	68	JLCC	12	47
EP1810T		PLCC	13	44
		PGA	6	38
EP312	24	CerDIP	16	47
		PDIP	16	52
	28	PLCC	16	56
EP324	40	CerDIP	13	34
		PDIP	15	43
	44	PLCC	15	43
EP22V10	24	CerDIP	19	50
EP22V10E		PDIP	21	66
EP22V10V	28	PLCC	21	65
EP220	20	CerDIP	30	68
		PDIP	25	90
		PLCC	25	90
EP224	24	CerDIP	20	55
		PDIP	22	75
	28	PLCC	22	75

Table 3. Thermal Resistance of MAX 5000 Devices

Device	Pin Count	Package	θ_{JC} (° C/W)	θ_{JA} (° C/W)
EPM5032	28	CerDIP	12	44
		PDIP	19	48
		JLCC	9	69
		PLCC	10	59
		SOIC	*Note (1)*	*Note (1)*
EPM5064	44	JLCC	15	62
		PLCC	9	52
EPM5128	68	JLCC	11	39
		PLCC	12	44
		PGA	2	32
EPM5128A	68	JLCC	11	39
		PLCC	12	44
EPM5130	84	JLCC	*Note (1)*	30
		PLCC	11	35
	100	CQFP	11	50
		PQFP	10	50
		PGA	4	26
EPM5192	84	JLCC	4	30
		PLCC	11	35
		PGA	2	27
EPM5192A	84	JLCC	4	30
		PLCC	11	35
	100	CQFP	11	50
		PQFP	10	50

Note:
(1) Consult factory for more information.

Table 4. Thermal Resistance of MAX 7000 Devices

Device	Pin Count	Package	θJC (° C/W)	θJA (° C/W)
EPM7032	44	PLCC PQFP TQFP	9 *Note (1)* 19	52 63 64
EPM7032V	44	PLCC TQFP	*Note (1)* 19	*Note (1)* 64
EPM7064	44	PLCC TQFP	*Note (1)* *Note (1)*	*Note (1)* *Note (1)*
	68	PLCC	12	44
	84	PLCC	11	35
	100	PQFP	10	50
EPM7096	68	JLCC PLCC	12 12	48 44
	84	JLCC PLCC	*Note (1)* 11	30 55
	100	CQFP PQFP	11 10	50 50
EPM7128E	84	PLCC	11	35
	100	PQFP	*Note (1)*	50
	160	PQFP	7	40
EPM7160E	84	PLCC	11	35
	100	PQFP	10	50
	160	PQFP	7	40
EPM7192E	160	PGA PQFP	7 7	20 40
EPM7256E	192	PGA	6	16
	208	RQFP	2	18

Note:
(1) Consult factory for more information.

Table 5. Thermal Resistance of FLEX 8000 Devices

Device	Pin Count	Package	θ_{JC} (C/W)	θ_{JA} (C/W) Still Air	θ_{JA} (C/W) 100 ft./min.	θ_{JA} (C/W) 200 ft./min.	θ_{JA} (C/W) 400 ft./min.
EPF8282 EPF8282A	84	PLCC	11	35	23	18	14
EPF8282V EPF8282AV	100	TQFP	10	44	38	34	31
EPF8452	84	PLCC	11	35	23	18	14
EPF8452A	160	PQFP	7	40	26	20	16
	160	PGA	6	20	13	10	8
EPF8636A	84	PLCC	11	35	23	18	14
	192	PGA	6	16	11	8	6
	208	RQFP	2	18	12	9	7
EPF8820	160	PQFP	*Note (1)*	*Note (1)*	*Note (1)*	*Note (1)*	*Note (1)*
EPF8820A	192	PGA	6	16	11	8	6
	208	RQFP	2	18	12	9	7
	225	BGA	6	28	19	14	11
EPF81188	208	PQFP	*Note (1)*	*Note (1)*	*Note (1)*	*Note (1)*	*Note (1)*
EPF81188A	232	PGA	2	14	10	7	5
	240	RQFP	2	20	13	10	8
EPF81500	240	PQFP	*Note (1)*	*Note (1)*	*Note (1)*	*Note (1)*	*Note (1)*
EPF81500A	280	PGA	2	14	10	7	5
	304	RQFP	1	20	13	10	8

Note:
(1) Consult factory for more information.

Comparing Maximum Allowed Power & Estimated Power

To avoid reliability problems, the system designer should compare the values calculated for maximum allowed power and estimated power. The estimated power should be the smaller of the two values. If the estimated power exceeds the maximum allowed power, refer to "Thermal Management" in this data sheet for suggestions on how to reduce power requirements for a design.

Thermal Management

The following actions reduce power dissipation, and thus heat build-up, for an application.

- *Use available low-power features of the device.* Classic devices and individual MAX 7000 and MAX 9000 macrocells can be configured for low-power operation, with only a nominal increase in propagation delay, by turning the Turbo Bit off. All macrocells in the MAX 7000 or MAX 9000 device that do not need to run in high-performance mode should be set to low-power mode.
- *Choose a different device package.* A ceramic or higher-pin-count package can be used. Ceramic packages dissipate more heat than plastic packages. Also, packages with higher pin counts can dissipate more heat through the connection to the PCB.
- *Use forced-air cooling and/or heat-sinking.* Forced-air cooling improves the efficiency of convection cooling, reducing the surface temperature of the device. A heat sink connected to a device significantly increases heat dissipation by radiating heat via the metal mass.
- *Slow the operation in portions of the circuit.* I_{CC} is proportional to the frequency of operation. Slowing parts of a circuit lowers the I_{CC} and hence reduces the power. Altera devices provide global or array Clock sources for all registers. Signals that do not require high-speed operation can use a slower array Clock that significantly reduces the system power consumption.
- *Reduce the number of outputs.* DC and AC current is required to support all I/O pins on the device. Reducing the number of I/O pins may reduce the current necessary for the project, and thereby reduce the power.
- *Reduce the amount of circuitry in the device.* Power depends on the amount of internal logic that switches at any given time. Reducing the amount of logic in a device reduces the current in the device. The same effect may be achieved by using a larger device, which also provides increased heat dissipation and maintains a single-device solution.
- *Choose a different device family.* The MAX 7000 family provides more power-saving features than the MAX 5000 family. The Classic family provides power-saving features at low density.

- *Modify the design to reduce power.* Identify areas in the design that can be revised to reduce the power requirements. Common solutions include reducing the number of switching nodes and/or required logic, and removing redundant or unnecessary signals. For assistance in locating less obvious changes, contact Altera Applications at (800) 800-EPLD.

Device Erasure

Altera Classic, MAX 5000, MAX 7000, and MAX 9000 devices use non-volatile, reprogrammable EPROM or EEPROM memory elements to retain the configuration data so that the configuration data does not need to be reloaded when the system powers up. EPROM and EEPROM memory elements have similar programming characteristics, but different erasure mechanisms.

Altera's EPROM-based devices are available in both plastic and ceramic packages. EPROM devices in plastic packages are one-time-programmable (OTP) devices; windowed ceramic packages allow erasure by exposure to UV light. Altera EPROM-based devices begin to erase when exposed to lights with wavelengths shorter than 4,000 Å. Since fluorescent lighting and sunlight fall into this range, an opaque label must be placed over the device window to ensure long-term reliability. To completely erase a device, it must be exposed to UV light with a wavelength of 2,540 Å. Devices should be erased for one hour (2.5 hours for EP22V10 and EP22V10E devices) by an eraser system with a power rating of 12,000 $\mu W/cm^2$. Altera devices may be damaged by long-term exposure to high-intensity UV light.

Altera guarantees that its EPROM-based devices can be programmed and erased at least 25 times, provided that the recommended erasure exposure levels are used. Most devices can be reliably erased and reprogrammed many more times beyond this guaranteed minimum.

All Altera EEPROM- and FLASH-based devices are reprogrammable. EEPROM and FLASH memory elements are electrically erasable and therefore do not have an erasure window. EEPROM- and FLASH-based devices are erased immediately before being programmed, and can be erased and reprogrammed at least 100 times. Most devices can be reliably erased and reprogrammed many more times beyond this guaranteed minimum.

Notes:

Metastability
in Altera Devices

March 1995, ver. 1 Application Note 42

Introduction

The output of an edge-triggered flipflop has two valid states: high and low. To guarantee reliable operation, designs must meet the flipflop's timing requirements. The input to the flipflop must be stable for a minimum time before the Clock edge (register setup time, or t_{SU}) and a minimum time after the Clock edge (register hold time, or t_H). Specific values for t_{SU} and t_H are provided in the device data sheets in this data book, or they can be determined using the MAX+PLUS II Timing Analyzer.

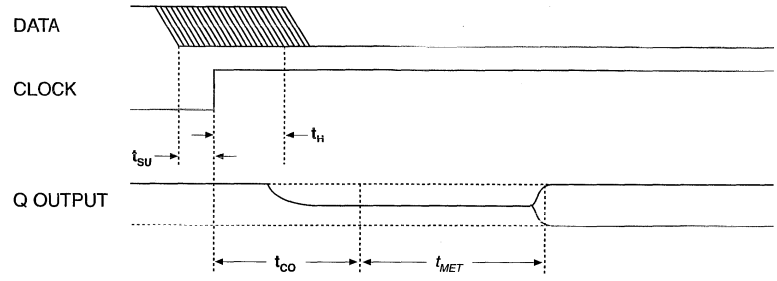
In non-synchronous systems, if the asynchronous input signals violate a flipflop's timing requirements, the output of the flipflop can become metastable. Metastable outputs oscillate or hover between high and low states for a brief period of time, which can cause system failure. Therefore, you must analyze the metastability characteristics of a device to determine the reliability of a non-synchronous design. In synchronous systems, the input signals always meet the flipflop's timing requirements, so metastability does not occur.

This application note describes metastability, how it is quantified, and how to minimize its effect. It also includes metastability data for Altera's MAX 7000, FLEX 8000, and EPX780 and EPX740 FLASHlogic devices that can be used to estimate the mean time between failures (MTBF) of a system that uses an Altera device to synchronize asynchronous data.

Metastability

Violating the setup or hold times of a flipflop can cause its output to become metastable. When a flipflop is in a metastable ("in between") state, the output hovers at a voltage level between high and low, causing the output transition to be delayed beyond the specified Clock-to-output delay (t_{CO}). The additional time beyond t_{CO} that a metastable output takes to resolve to a stable state is called the settling time (t_{MET}). Not every transition that violates the setup or hold times will result in a metastable output. The likelihood that a flipflop will enter a metastable state and the time required to return to a stable state varies depending on the process technology used to manufacture the device and on the ambient conditions. Generally, flipflops quickly return to a stable state. See Figure 1.

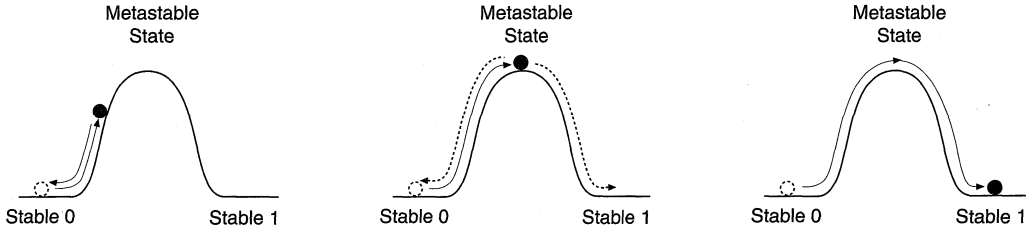
Figure 1. Metastability Timing Parameters



The operation of a register is analogous to a ball rolling over a frictionless hill, as shown in Figure 2. Each side of the hill represents a stable (i.e., high or low) state, and the top of the hill represents the metastable state. When the data input of a flipflop complies with minimum setup (t_{SU}) and hold (t_H) times, the output passes from one stable state to another (i.e., from high to low or low to high) without any additional delay. Analogously, the ball will get over the hill within a specified time if given enough of a push.

However, when the data input of a flipflop violates the setup or hold times, the flipflop is marginally triggered, and the output may not immediately resolve to either of the two stable states within the specified time. This marginal triggering may cause the output to glitch, to remain temporarily at a metastable state between the high and low logic levels, or to take longer to return to a stable state, increasing the delay from the Clock transition to a stable output. See Figure 2.

Figure 2. Effects of Violating t_{SU} & t_H Requirements



Output glitches.

Output temporarily remains at a metastable state and may return to either stable state.

Output passes through a metastable state and incurs an additional delay.

Metastability does not necessarily cause unpredictable system performance. If the wait time is sufficient to allow the flipflop to settle to a stable state, then metastability will not affect the system; the output of the flipflop can temporarily have an undefined value, provided that it returns to a known value before the signal is evaluated. Therefore, allowing an additional time (t_{MET}) for the signal to settle to a known state will prevent the propagation of an undefined value to the rest of the system.

Analyzing Metastability

The MTBF shows quantitatively how metastability affects your design. The MTBF provides an estimate of the mean time between the probabilistic occurrence of two successive metastable events. The MTBF of a synchronizing flipflop can be estimated with the following formula:

$$\text{MTBF} = \left[f_{CLOCK} \times f_{DATA} \times C_1 \times e^{(-C_2 \times t_{MET})} \right]^{-1}$$

The t_{MET} parameter is the additional time required for the flipflop to settle to a stable state. The constants C_1 and C_2 vary according to the process technology used to manufacture the device. Therefore, different devices manufactured with the same technology have similar values for C_1 and C_2.

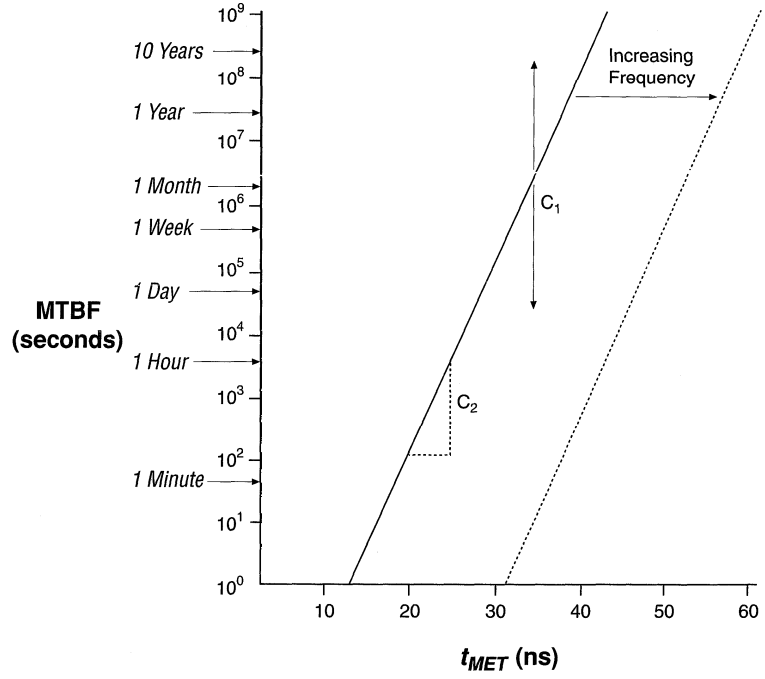
The constants C_1 and C_2 are determined by plotting the natural log of MTBF vs. t_{MET} and performing a linear regression analysis on the data. The slope and the y-intercept of the resulting line determine the values of C_1 and C_2. The formulae for the constants C_1 and C_2 are as follows:

$$C_2 = \frac{\ln(\Delta MTBF)}{\Delta t_{MET}}$$

$$C_1 = \frac{e^{(-C_2 \times t_{MET})}}{MTBF \times f_{CLOCK} \times f_{DATA}}$$

Figure 3 shows the relationship between the MTBF and t_{MET}.

Figure 3. MTBF vs. t_{MET}



The constant C_1 scales the MTBF equation linearly, shifting the entire curve up or down. Therefore, the larger the value of C_1, the higher the MTBF. The constant C_2 affects the slope of the MTBF/t_{MET} curve; therefore, C_2 determines how quickly the flipflop settles to a stable state. For higher C_2 values, the settling time is lower. Increasing the operating frequency will shift the entire curve to the right, lowering the MTBF value.

Once the values for C_1 and C_2 are determined for a particular device, you can use the metastability equation, shown on page 433, to calculate the MTBF of a system with a given settling time (t_{MET}). The t_{MET} delay is the additional time required for the flipflop to resolve, or the difference between the minimum system clock period and the actual clock period. You can also use the metastability equation to determine the t_{MET} delay required for a given MTBF value, as shown below:

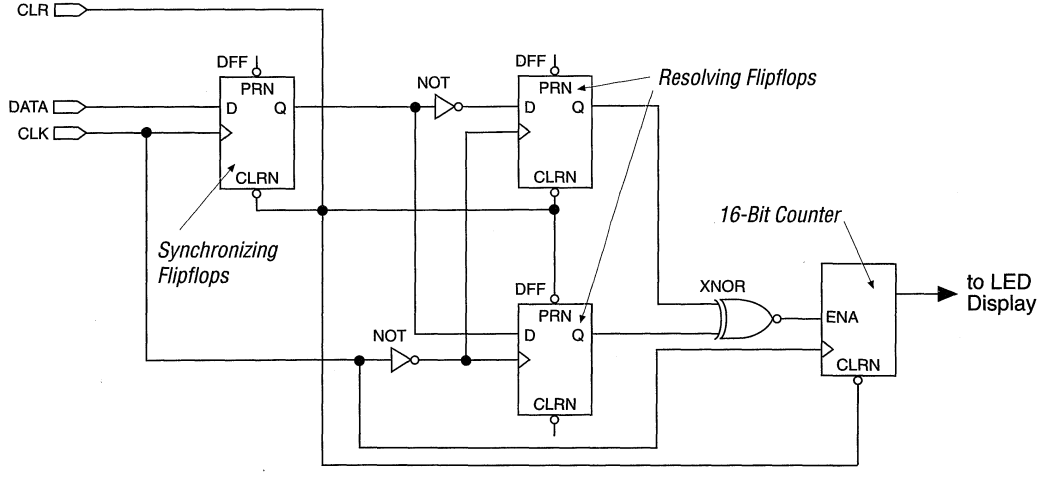
$$t_{MET} = \frac{\ln(\text{MTBF} \times f_{CLOCK} \times f_{DATA} \times C_1)}{C_2}$$

Test Circuitry

Figure 4 shows the test circuit used to determine the metastability characteristics of Altera devices. In this figure, one flipflop has asynchronous Clock and data inputs. The logic that generates the metastable event and the logic that detects it are both located in the device under test (DUT). The output of the synchronizing flipflop is fed directly to one of the resolving flipflops and through an inverter to the other resolving flipflop. The outputs of the resolving flipflops feed an XNOR gate that is at a high logic level when the values of the outputs (the signal and its complement) are the same. If the resolving flipflops detect that the signal and its complement have the same logical value, a metastable event has occurred and the counter is incremented.

Figure 4. Metastability Test Circuit

All logic is part of the device under test (DUT).



Since the resolving flipflops are clocked by the falling edge of the Clock, the required settling time can be controlled by changing the Clock high time (Δt). The settling time t_{MET} can be determined with the equation below. The $\mathbf{t_{ACNT}}$ delay is the minimum delay from the Clock edge to the output of the synchronizing flipflop, plus the delay from the output of the synchronizing flipflop to the input of the resolving flipflops, plus the setup time of the resolving flipflop. The t_{MET} parameter is the minimum time allowed under normal operation of the circuit.

$$t_{MET} = \Delta t - \mathbf{t_{ACNT}}$$

Metastability Characteristics of Altera Devices

Figure 5 shows the metastability characteristics of MAX 7000, FLEX 8000, and EPX780 and EPX740 FLASHlogic devices. For all devices, f_{DATA} is 1 MHz and f_{CLOCK} is 10 MHz.

Figure 5. Metastability Characteristics of Altera Devices

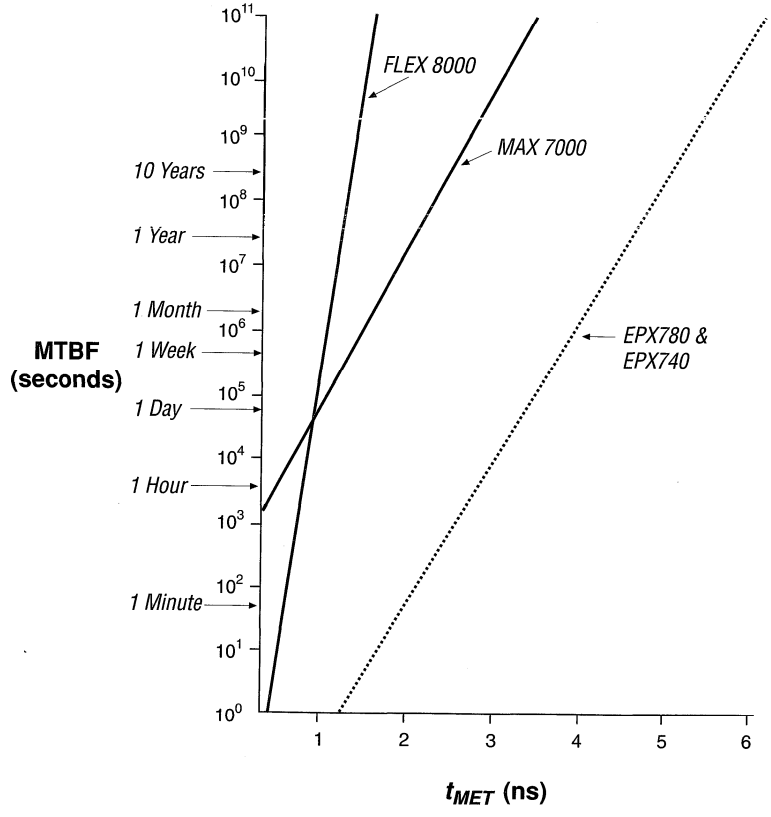


Table 1 summarizes the values of C_1 and C_2 for Altera's MAX 7000, FLEX 8000, and EPX780 and EPX740 FLASHlogic devices.

Table 1. Metastability Equation Constants

Device	C_1	C_2
MAX 7000	2.98×10^{-17}	5.023×10^{9}
FLEX 8000	1.011×10^{-13}	1.268×10^{10}
EPX780 & EPX740	5.30×10^{-11}	5.08×10^{9}

Applying the Metastability Equation

You can use the C_1 and C_2 values listed in Table 1 to calculate the MTBF for a specific settling time, or you can calculate the minimum settling time for a specific MTBF. For example, the equation below calculates the t_{MET} needed to ensure a MTBF of 1 year (approximately 3×10^7 seconds) for an EPF8452 with a data frequency of 2 MHz and a Clock frequency of 10 MHz.

$$t_{MET} = \frac{\ln(3 \times 10^7) + \ln[(10 \times 10^6)(2 \times 10^6)(1.011 \times 10^{-13})]}{1.268\text{E} + 10} = 1.41\text{ns}$$

When calculating the delay for the output of the flipflop to the remaining logic for a MTBF of one year, 1.41 ns should be added to the Clock-to-output delay (t_{CO}) of the flipflop.

Due to the logarithmic relationship between the MTBF and t_{MET}, small changes in t_{MET} dramatically affect the MTBF. If the MTBF required is increased from one year to ten years in the example shown above, the t_{MET} delay is only increased to 1.59 ns.

Figures 6, 7, and 8 show the t_{MET} delay required for MAX 7000 (including MAX 7000E), FLEX 8000, and EPX780 and EPX740 FLASHlogic devices, respectively, when f_{DATA} is one half of f_{CLOCK}. Because the MTBF is inversely proportional to the value ($f_{CLOCK} \times f_{DATA}$), these figures can be used to find the MTBF for many designs. Metastability is probabilistic, and MTBF values are mean values calculated for a limited sample of devices and should only be used to estimate t_{MET} delays.

Figure 6. MAX 7000 (Including MAX 7000E) MTBF Values

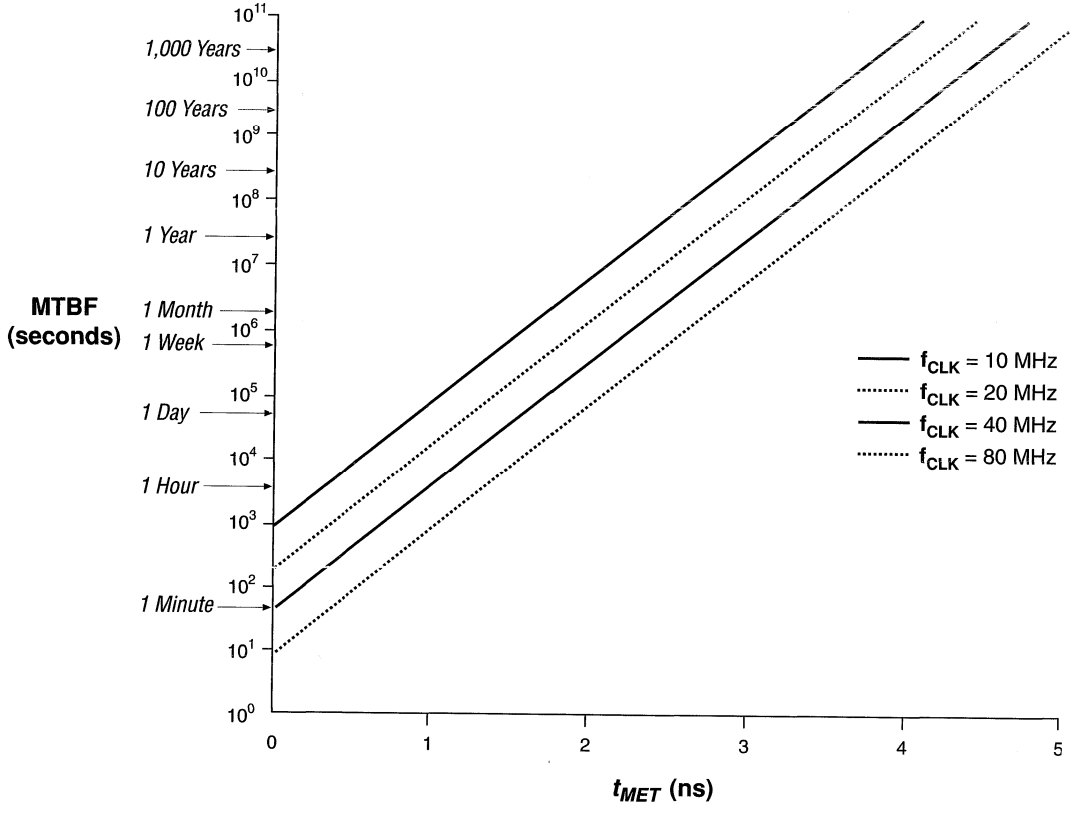


Figure 7. FLEX 8000 MTBF Values

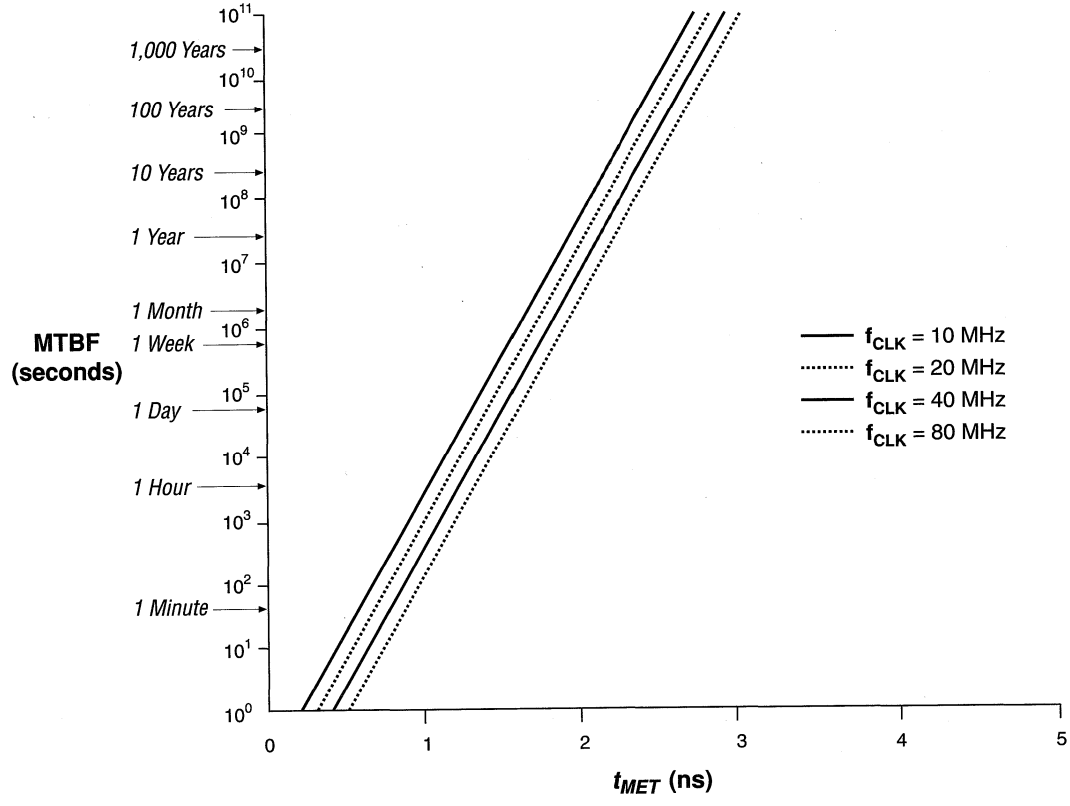
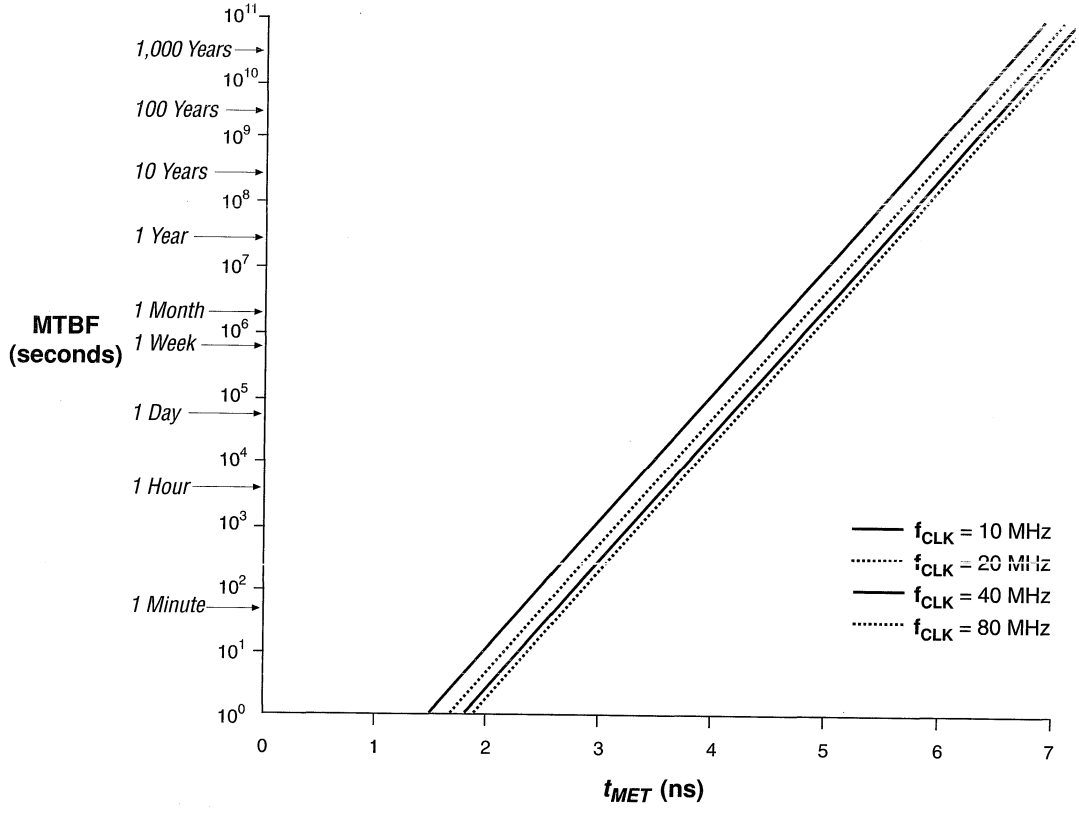


Figure 8. EPX740 & EPX780 MTBF Values

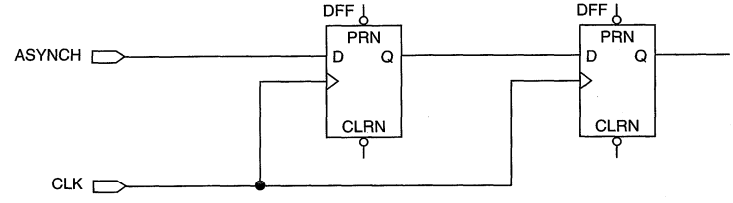


Avoiding Metastability

Several techniques can be used to reduce metastability in a system. If an asynchronous signal is fed to several flipflops, the probability that a metastable event will occur greatly increases because there are more flipflops that could become metastable. In this case, you can avoid metastability by using the output of the synchronizing flipflop throughout the system rather than the asynchronous signal. You can also avoid the negative effects of metastability by adding the t_{MET} calculated for a specific MTBF to the worst-case timing delay calculations, giving the output of the synchronizing flipflops time to settle. Faster devices provide faster t_{CO} and t_{SU} times, which provide additional time for the t_{MET} delay without sacrificing overall system speed.

The most common method of reducing the effects of metastability is to use a multiple-stage synchronizer in which two or more flipflops are cascaded to form a synchronization circuit. See Figure 9. If the synchronizing flipflop produces a metastable output, then the metastable signal may resolve before it is clocked by the second flipflop. This method does not guarantee that the second flipflop will not clock an undefined value, but it doubles the probability that the data will go to a valid state before it reaches the rest of the circuit.

Figure 9. Multiple-Stage Synchronizer



Conclusion

Metastability is a phenomenon that can only affect flipflops that are used to synchronize data from asynchronous systems. The metastability characteristics for a particular device depend on the process technology used to manufacture the device and on ambient conditions. Altera devices have very good metastability characteristics; you only need to add a small t_{MET} delay to the t_{CO} delay to achieve a high MTBF value.

Notes:

High-Speed Board Designs

March 1995, ver. 2 Application Brief 119

Summary

To create a successful high-speed printed circuit board (PCB), you must integrate the device(s), board(s), and other elements into a coherent design. Altera devices typically provide 1-ns to 3-ns edge rates, which contribute to noise generation, signal reflection, cross-talk, and ground bounce. Therefore, your design must filter and evenly distribute power to all devices to reduce noise, terminate signal and transmission lines to diminish signal reflection, minimize cross-talk between parallel traces, and reduce the effects of ground bounce.

Power Filtering & Distribution

You can dramatically reduce system noise by providing clean, evenly distributed power to all boards and devices that is as close as possible to V_{CC}.

Filtering Noise

To diminish the low-frequency (< 1 kHz) noise caused by the power supply, you must filter the noise on the power lines at the point at which the power connects to the PCB, as well as at each device. Altera recommends placing a 100-µF electrolytic capacitor immediately adjacent to the location where the power supply lines enter the PCB. If you use a voltage regulator, place the capacitor immediately after the final stage that provides the V_{CC} signal to the device(s). Capacitors not only filter low-frequency noise from the power supply, but also supply extra current when many outputs switch simultaneously in a circuit.

The components on the PCB add high-frequency noise to the power plane. To filter high-frequency noise at the device, Altera recommends placing 0.02-µF or 0.2-µF decoupling capacitors as close as possible to each V_{CC} and GND pair. See *Operating Requirements for Altera Devices* in this data book for more information on bypass capacitors.

Distributing Power

Power distribution also has an impact on system noise. Power can be distributed throughout the PCB with either a power bus network or power planes.

A power bus network consists of two or more wide, metal traces that carry the V_{CC} and GND to the devices. Usually used on two-layer PCBs, power

buses provide an inexpensive method of supplying power. The trace widths, which should be as wide as possible, are limited by the density of the PCB. Power buses have significant DC resistance; the last component on the bus may receive V_{CC} power that is degraded by as much as 0.5 V. Consequently, Altera recommends using power buses only for applications that do not require equal distribution of V_{CC}.

As an alternative, Altera recommends using power planes to distribute power. Power planes are used on multi-layer PCBs and consist of two or more metal layers that carry V_{CC} and GND to the devices. Because the power plane covers the full area of the PCB, its DC resistance is very low. The power plane maintains V_{CC} and distributes it equally to all devices. The power plane also provides near-infinite current-sink capability, noise protection, and shielding for the logic signals on the PCB.

Signal & Transmission Line Termination

Having established the PCB power network, you must consider the layout of the devices and traces. Fast edge rates contribute to noise, cross-talk, and ground bounce to varying degrees, depending on the PCB construction material.

Each PCB substrate has a different relative dielectric constant (E_r) that measures the effect of an insulator on the capacitance of a pair of conductors as compared to the capacitance of the conductor pair in a vacuum. The type of substrate used determines the length at which the signal traces must be handled as transmission lines. Table 1 lists E_r values for various dielectric materials.

Table 1. Relative Dielectric Constants

Material	E_r
Air	1.0
PTFE/Glass	2.2
Rogers RO 2800	2.9
CE/Goreply	3.0
BT/Goreply	3.3
CE/Glass	3.7
Silicon Dioxide	3.9
BT/Glass	4.0
Polymide/Glass	4.1
FR-4/Glass	4.1
Glass Cloth	6.0
Alumina	9.0

As shown in the following equation, the relative dielectric constant (E_r) of the material determines the velocity (V_P) at which signals may flow. The constant (C) equals 3×10^8 m/s or 30 cm/ns:

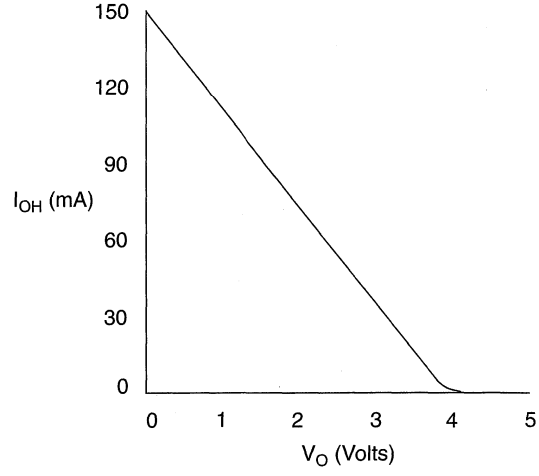
$$V_P = \frac{C}{\sqrt{E_r}}$$

The signal trace must be treated as a transmission line when the two-way propagation delay (PD) of the line exceeds the signal edge rate (t_R). The propagation delay for Classic, FLASHlogic, MAX 5000, MAX 7000, and MAX 9000 devices is the input-to-output (t_{PD}), while the propagation delay for FLEX 8000 devices is either the transfer rate from I/O pin to I/O pin via row, LE, and column (t_1) or the transfer rate from I/O pin to I/O pin via row, LE, and row (t_2). See the following equation:

$$2 \times PD > t_R$$

The rise time of an Altera device is a function of the capacitance that is driven by the device. You can estimate rise time if you know the device's capacitive load. Altera data sheets include a graph that shows output current vs. output voltage. You can derive an equation for rise time as a function of capacitance using the output current vs. output voltage graphs in the device data sheets in this data book. Figure 1 shows the voltage/current relationship graph for the EPM7032.

Figure 1. EPM7032 Voltage/Current Relationship



The relationship between I_{OH} and V_O is roughly linear until the voltage approaches 4 V. The equation for the linear approximation is as follows:

$$I_{OH} = 0.15 - \frac{0.15}{3.8} = 0.15 - 0.0395V$$

Solving the charging capacitor equation for time (t) yields the following equations:

$$\frac{\partial V}{\partial t} = \frac{I_{OH}}{C} \qquad t = \frac{C}{I_{OH}}(\partial V)$$

Substituting the equation above for I_{OH} results in the following equation:

$$\partial t = \frac{C}{0.15 - 0.0395V}(\partial V)$$

Integrating and solving the integral from 0 V to 2.4 V yields the following equation:

$$t = C\frac{-1}{0.0395} \times \ln(0.15 - 0.0395V)\Big|_0^{2.4} = 25.3C$$

You can choose different bounds for the integral if you need to drive a circuit in which V_H is greater than 2.4 V. For instance, if your Altera device is driving a CMOS input, V_H will increase to 4 V, so you can integrate from 0 V to 4 V instead of 2.4 V.

To calculate output delay time, you must first determine the rise time of the specified load. At the 35-pF load, the rise time is as follows:

$$t = (25.3)\ (35 \times 10^{-12})\ \text{sec} = 0.9\text{ns}$$

The propagation delay (PD) is the length (l) of the line divided by the velocity (V_P):

$$PD = \frac{l}{V_P}$$

By solving for length (l) using the equation below, you can calculate the length at which the line must be treated as a transmission line:

$$l > \frac{t_R \times C}{2\sqrt{E_r}}$$

As shown in Table 1, a PCB with glass cloth substrate has an E_r of six. Table 2 lists the maximum line lengths for MAX 5000, MAX 7000, and FLEX 8000 devices using a glass cloth substrate under a 35-pF load.

Table 2. Maximum Line Lengths for Glass Cloth Substrate

Device Family	t_R (ns)	*l* (cm)	*l* (inches)
MAX 5000	2.7	16.52	6.50
MAX 7000	0.9	5.51	2.17
FLEX 8000	1.1	6.73	2.65

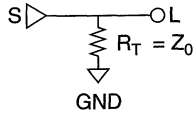
The impedance of the source (Z_S) must equal the impedance of the trace (Z_0) and the load (Z_L). Mismatched impedances cause signals to reflect back and forth and up and down the line, which in turn causes ringing at the load.

The load impedance is typically much higher than the line impedance, which is higher than the source impedance. On an unmatched transmission line, a signal reflects 100% at the load and approximately 80% at the source, bouncing back and forth until it dies out. To reduce signal reflection, you can match the impedance either at the load (Z_L) or at the source (Z_S) to the line impedance (Z_0) by adding an impedance in parallel with the load to reduce its input impedance.

Termination Schemes

Parallel termination diminishes the first reflection by matching the load impedance to the line impedance. Of the four parallel termination circuits described, Altera recommends using either the Thevenin or resistor and capacitor (series-RC) scheme. For the matching to be effective, you must terminate each load, since any impedance mismatch will result in a signal reflection. As an alternative to parallel termination, you can use series termination, which matches the impedance at the signal source.

Simple Parallel Termination



In a simple parallel termination scheme, the terminating resistor (R_T) is equal to the line impedance. The current loading of this termination is highest at a high-output state. You can estimate the current load (I_L) with the following equation. R_{DS} is the pull-up resistance from the I_{OH} curve of the output drive characteristic. R_{TOTAL} is the sum of R_{DS} and R_T.

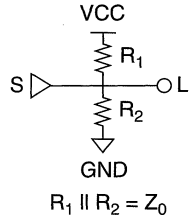
$$I_L = I_{OH} \times \frac{R_{DS}}{R_{TOTAL}}$$

For example, the current load for a 50-Ω parallel termination on a MAX 7000 device at 2.4 V is as follows:

$$I_L = 45mA \times \frac{25\Omega}{75\Omega} = 15mA$$

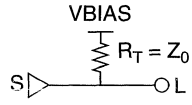
The current load cannot exceed the maximum DC limit per output pin. In this case, the 15-mA current load is less than the maximum DC limit of 25 mA per output pin for MAX 7000 devices.

Thevenin Parallel Termination



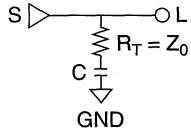
An alternative parallel termination scheme uses a Thevenin voltage divider. The terminating resistor is split between R_1 and R_2, which, when combined, equal the line impedance. Although this scheme reduces the current draw from the source device, it adds current draw from the power supply because the resistors are tied between V_{CC} and GND.

Active Parallel Termination



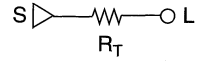
In an active parallel termination scheme, the terminating resistor ($R_T = Z_0$) is tied to a bias voltage (V_{BIAS}). The bias voltage is selected so that the output drivers are capable of drawing current from the high- and low-level signals. However, this scheme requires a separate voltage source that can sink and retain currents to match the output transfer rates.

Series-RC Parallel Termination



In a parallel termination scheme, a resistor and capacitor (series-RC) network is used as the terminating impedance. The terminating resistor (R_T) is equal to Z_0; the capacitor must be greater than 100 pF. The capacitor blocks low-frequency signals while passing high-frequency signals. Therefore, the DC loading effect of R_T does not impact the driver.

Series Termination



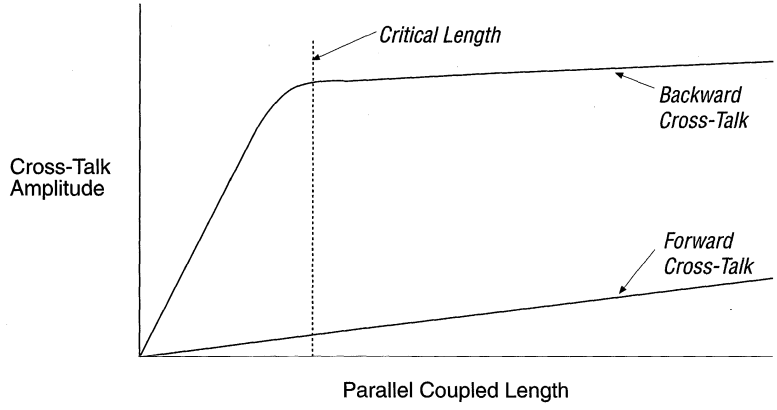
A series termination scheme matches the impedance at the signal source instead of matching the impedance at each load. Because the output impedance of Altera devices is low, you must add a series impedance to match the signal source to the line impedance.

On an unmatched line, the source eventually reduces the reflections; adding the series termination helps attenuate secondary reflections. The source impedance varies from 10 Ω to 18 Ω, and the line impedance varies depending on the distribution of the load. Therefore, you cannot choose a signal resistor value that applies to all conditions. Altera recommends using a 33-Ω series resistor to cover most impedances. This method requires only a single component at the source rather than multiple components at each load, but delays the signal path as it increases the RC time constant.

Cross-Talk

Cross-talk is the unwanted coupling of signals between parallel traces. Two types of cross-talk exist: forward (capacitive) and backward (inductive). Figure 2 illustrates the effect of each type of cross-talk as a function of the parallel length.

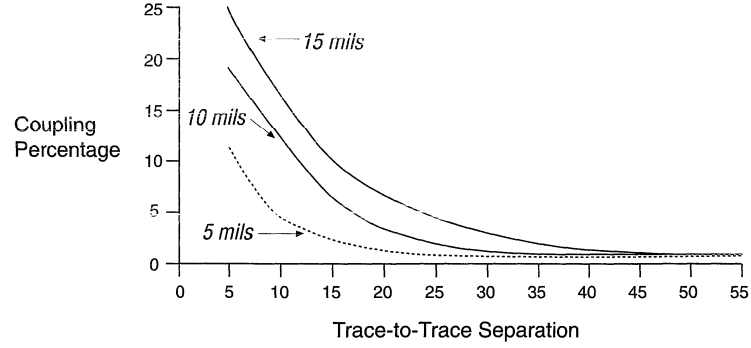
Figure 2. Cross-Talk as a Function of Parallel Length



Backward cross-talk, which has a more dramatic effect than forward cross-talk, occurs when the magnetic field from one trace induces a signal in a neighboring trace. In logic systems, the current flow through a trace is significant when the signals are switching or non-static. The magnetic fields created by switching currents induce the coupling transients.

You can dramatically reduce cross-talk by limiting the trace height to 10 mils above the GND plane. Figure 3 shows the effect of trace height on trace-to-trace coupling.

Figure 3. Effect of Trace Height on Trace-to-Trace Coupling



Ground Bounce

As digital devices become faster, their output switching times decrease. Faster switching times cause higher transient currents in outputs as they discharge load capacitances. These higher currents, which are generated when multiple outputs of a device switch simultaneously from a logic high to a logic low, can cause a board-level phenomenon known as ground bounce.

Many factors contribute to ground bounce. Therefore, no standard test method allows you to predict its magnitude for all possible PCB environments. You can only test the device under a given set of conditions to determine the relative contributions of each condition and of the device itself. Load capacitance, socket inductance, and the number of switching outputs are the predominant factors that influence the magnitude of ground bounce in programmable logic devices.

Design Recommendations

Altera recommends that you take the following steps to reduce ground bounce:

- Limit load capacitance by buffering loads with an external device such as the 74244 IC bus driver or by reducing the number of devices that drive the bus.
- Eliminate sockets whenever possible.
- Reduce the number of outputs that can switch simultaneously and/or distribute them evenly throughout the device.
- Move switching outputs close to a package GND pin.
- Eliminate pull-up resistors, or use pull-down resistors.
- Use multi-layer PCBs that provide separate V_{CC} and GND planes.
- Add 10-Ω to 30-Ω resistors in series to each of the switching outputs to limit the current flow into each of the outputs.
- Turn on the Slow Slew Rate logic option for MAX 9000, FLEX 8000, and MAX 7000E designs.

Go to "Slow Slew Rate" using **Search for Help on** (Help menu) in MAX+PLUS II for more information on this logic option.

These design practices, many of which are described in detail in this application brief, should help you create effective high-speed logic designs that operate over a wide range of PCB conditions.

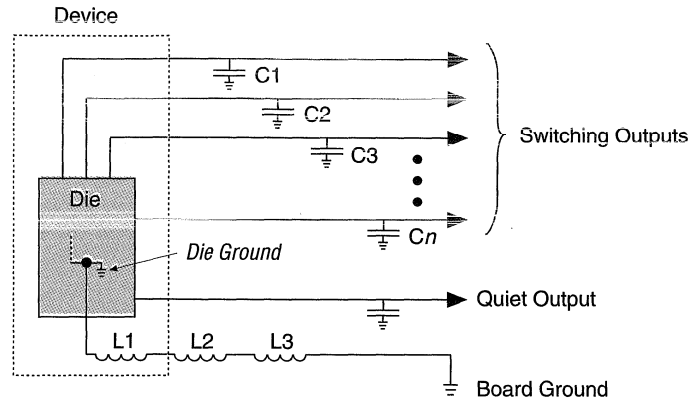
Analyzing Ground Bounce

Figure 4 shows a simple model for analyzing ground bounce. The external components driven by the device appear to that device as capacitive loads (C1 to C*n*). These capacitive loads store a charge that is determined by the following equation:

charge (Q) = [voltage (V) × capacitance (C)]

Thus, the charge increases as the voltage and/or load capacitance increases.

Figure 4. Ground Bounce Model



The environment and ground path of a device have intrinsic inductances (shown in Figure 4 as L1, L2, and L3). L1 is the inductance of the bond wire from the device's die to its package pin, and of the pin itself. L2 is the inductance of the connection mechanism between the device's ground pin and the PCB. This inductance is greatest when the device is connected to the PCB through a socket. L3 is the inductance of the PCB trace between the device and the PCB location where the power supply's reference ground is connected.

Ground bounce occurs when multiple outputs switch from high to low. The transition causes the charge stored in the load capacitances to flow into the device. The sudden rush of current ($\partial i/\partial t$) exits the device through the inductances (L) to board ground, generating a voltage (V) determined by the equation $V = L \times (\partial i/\partial t)$. This voltage difference between board ground and device ground causes the relative ground level for low, or quiet, outputs to temporarily rise, or bounce. Although the rush of current is brief, the magnitude of the bounce can be large enough to trigger other devices on the PCB.

In synchronous designs, ground bounce is less often a problem because synchronous outputs have enough time to settle before the next Clock edge. Also, synchronous circuits are not as likely to be falsely triggered by a voltage spike on a quiet output.

Ground bounce is affected differently by capacitive loading on the switching outputs and quiet outputs.

Switching Outputs

When the capacitive loading on the switching outputs increases, the amount of charge available for instantaneous switching increases, which in turn increases the magnitude of ground bounce. Depending on the device, ground bounce increases with capacitive loading until the loading is approximately 100 pF per device output. At this point, the device output buffers reach their maximum current-carrying capacity and inductive factors become dominant.

One method of reducing the capacitive load, and consequently ground bounce, is to connect the device's switching outputs to a bus driver IC. The outputs of the bus driver IC drive the heavy capacitive loads, reducing the loading on the device, thus minimizing ground bounce for the device's quiet outputs.

Some bus applications use pull-up resistors to create a default high value for the bus. These resistors cause the load capacitances to charge up to the maximum voltage. Consequently, the driving device produces a higher level of ground bounce. Therefore, you should eliminate pull-up resistors in applications in which ground bounce is a concern, or design a bus logic that uses pull-down resistors instead.

The number of switching outputs also affects ground bounce. As the number of switching outputs increases, the total charge stored also increases. The total charge is equal to the sum of the stored charges for each switching output. Therefore, the amount of current that must sink to ground increases as the number of switching outputs increases. Ground bounce can increase by as much as 40 mV to 50 mV for each additional output that is switching.

To counteract these effects, Altera devices provide multiple VCC and GND pin pairs. You can reduce ground bounce by moving switching outputs close to a package GND pin, and by distributing simultaneously switching outputs throughout the device.

Many Altera devices have slew rate options for the output drivers. Setting all or most of the drivers so that the slow slew rate is on slows down the drivers, decreasing $\partial i/\partial t$ and reducing ground bounce.

To further reduce ground bounce, limit the number of outputs that can switch simultaneously in your design. For functions such as counters, you can use Gray coding as an alternative to standard sequential binary coding, since only one bit switches at a time.

In extreme cases, adding resistors (10 Ω to 30 Ω is usually adequate) in series to each of the switching outputs in a high-speed logic device can limit the current flow into each of the outputs, and thus reduce ground bounce to an acceptable level.

Quiet Outputs

An increase in capacitive loading on quiet outputs acts as a low-pass filter and tends to dampen ground bounce. Capacitive loading on a quiet output can reduce ground bounce by as much as 200 to 300 mV. However, an increase in capacitive loading on a quiet output can increase the noise seen on other quiet outputs.

Minimizing Lead Inductance

Socket usage and PCB trace length are two elements of L2, the inductance of the connection mechanism between the device's ground pin and the PCB shown in Figure 4. Sockets can cause ground bounce voltage to increase by as much as 100%. You can often dramatically reduce the ground bounce on the PCB by eliminating sockets. The length of the PCB trace has a much smaller effect on ground bounce than sockets. For PCBs with a ground plane, the voltage drop across the inductance (L3) of the PCB trace between the device and the PCB location where other devices in the system reference ground is negligible, because L3 is significantly less than L2. The inductance in a 3-inch trace increases ground bounce for a quiet output by approximately 100 mV. Nevertheless, trace length should be kept to a minimum. As traces become longer, transmission line effects may cause other noise problems.

You can also reduce ground bounce due to PCB trace inductance by using multi-layer PCBs that provide separate V_{CC} and GND planes. Wire-wrapping the V_{CC} and GND supplies usually increases the amount of ground bounce. To reduce unwanted inductance, you should use low-inductance bypass capacitors between the V_{CC} supply pins and the board GND plane, as close to the package supply pins as possible. A standard decoupling capacitor (0.02 mF to 0.2 mF) used in parallel with a high-frequency decoupling capacitor (470 pF is a standard value) gives the best results.

References

Knack, Kella. *Debunking High-Speed PCB Design Myths.* ASIC & EDA, Los Altos: James C. Uhl, July 1993.

Understanding Classic, MAX 5000 & MAX 7000 Timing

March 1995, ver. 3 Application Brief 100

Introduction

Altera devices provide device performance that is consistent from simulation to application. Before programming a device, you can determine the worst-case timing delays for any design. You can calculate propagation delays either with the MAX+PLUS II Timing Analyzer or with the timing models given in this application brief and the timing parameters listed in individual device data sheets. Both methods yield the same results.

This application brief defines device internal delay parameters and AC timing characteristics, and illustrates the timing models for the Classic, MAX 5000, and MAX 7000 device families. For information on FLEX 8000 or MAX 9000 timing, refer to *Application Brief 143 (Understanding FLEX 8000 Timing)* or *Application Brief 144 (Understanding MAX 9000 Timing)* in this data book.

Familiarity with device architecture and characteristics is assumed. Refer to specific device or device family data sheets in this data book for complete descriptions of the architectures.

Internal Device Delay Parameters

Within a device, timing delays contributed by individual architectural elements are called microparameters. Microparameters cannot be measured explicitly. The following list defines microparameters for Classic, MAX 5000, and MAX 7000 devices. The device data sheets for MAX 5000 and MAX 7000 devices in this data book give the values for these microparameters; microparameters for Classic devices are listed in this application brief.

t_{IN} Input pad and buffer delay. In Classic and MAX 5000 devices, it is the time required for a dedicated input pin to drive the true and complement data input signal into the logic array(s). In MAX 7000 devices, it is the time required for a dedicated input pin to drive the input signal into the Programmable Interconnect Array (PIA) or into the global control array.

t_{IO} I/O input pad and buffer delay. This delay applies to I/O pins used as inputs. In Classic devices, it is the delay added to t_{IN}. In MAX 5000 devices with a single Logic Array Block (LAB), it is the delay from the I/O pin to the logic arrays. In MAX 7000 and multi-LAB MAX 5000 devices, it is the delay from the I/O pin to the PIA.

t_{PIA} Programmable Interconnect Array delay. The delay incurred by signals that require routing through the PIA. MAX 7000 and multi-LAB MAX 5000 devices only.

t_{SEXP} Shared expander array delay. The delay of a signal through the AND-NOT structure of the shared expander product-term array that is fed back into the logic array. MAX 5000 and MAX 7000 devices only.

t_{PEXP} Parallel expander delay. The additional delay incurred by adding parallel expander product terms to the macrocell product terms. For each group of up to five parallel expanders added to a single function, an additional t_{PEXP} delay is added to the timing path. MAX 7000 devices only.

t_{ICS} Global Clock delay. The delay from the dedicated Clock pin to a register's Clock input. Classic and MAX 5000 devices only.

t_{GLOB} Global control delay. The delay from a dedicated input pin to any global control function in a macrocell or I/O control block. MAX 7000 devices only.

t_{LAC} Logic array control delay. The AND array delay for register control functions such as Preset, Clear, and Output Enable. MAX 5000 and MAX 7000 devices only.

t_{IC} Array Clock delay. The delay through a macrocell's Clock product term to the register's Clock input.

t_{EN} Register Enable delay. The register AND array delay from the PIA to the register Enable input. MAX 7000 devices only.

t_{CLR} Register Clear time. The delay from the assertion of the register's asynchronous Clear input to the time the register output stabilizes at logical low.

t_{PRE} Register Preset time. The delay from the assertion of the register's asynchronous Preset input to the time the register output stabilizes at logical high.

t_{LAD} Logic array delay. The time a logic signal requires to propagate through a macrocell's AND-OR-XOR structure.

t_{RD} Register delay. The delay from the rising edge of the register's Clock to the time the data appears at the register output. MAX 5000 and MAX 7000 devices only.

t_{SU} Register setup time. The time required for a signal to be stable at the register input before the Clock's rising edge to ensure that the register correctly stores the input data.

t_{H} Register hold time. The time required for a signal to be stable at the register input after the register Clock's rising edge to ensure that the register correctly stores the input data.

t_{COMB} Combinatorial buffer delay. The delay from the time when a combinatorial logic signal bypasses the programmable register to the time it becomes available at the macrocell output. MAX 5000 and MAX 7000 devices only.

t_{LATCH} Latch delay. The propagation delay through the programmable register when it is configured as a flow-through latch. MAX 5000 devices only.

t_{FD} Feedback delay. In Classic devices, it is the delay of a macrocell output fed back into the logic array. In single-LAB MAX 5000 devices, it is the delay of a macrocell output fed back into the logic array. In multi-LAB MAX 5000 devices, it is the delay of a macrocell output fed back into the LAB's logic array or to a PIA input.

t_{OD1} Output buffer and pad delay with the Slow Slew Rate logic option turned off and V_{CCIO} = 5.0 V. MAX 7000 devices only.

t_{OD2} Output buffer and pad delay with the Slow Slew Rate logic option turned off and V_{CCIO} = 3.3 V. MAX 7000 devices only.

t_{OD3} Output buffer and pad delay with the Slow Slew Rate logic option turned on. MAX 7000 devices only.

t_{XZ} Output buffer disable delay. The delay required for high impedance to appear at the output pin after the output buffer's Enable control is disabled.

t_{ZX} Output buffer Enable delay. The delay required for the output signal to appear at the output pin after the tri-state buffer's Enable control is enabled.

t_{ZX1} Output buffer Enable delay with the Slow Slew Rate logic option turned off and V_{CCIO} = 5.0 V. The delay required for the output signal to appear at the output pin after the tri-state buffer's Enable control is enabled.

t_{ZX2} Output buffer Enable delay with the Slow Slew Rate logic option turned off and V_{CCIO} = 3.3V. The delay required for the output signal to appear at the output pin after the tri-state buffer's Enable control is enabled.

t_{ZX3} Output buffer Enable delay with the Slow Slew Rate logic option turned on and V_{CCIO} = 5.0 V or 3.3 V. The delay required for the output signal to appear at the output pin after the tri-state buffer's Enable control is enabled.

t_{LPA} Low-power adder. The delay associated with macrocells in low-power operation. In low-power mode, t_{LPA} must be added to the logic array delay (t_{LAD}), the register control delay (t_{LAC}, t_{IC}, t_{ACL}, or t_{EN}), and the shared expander delay (t_{SEXP}) paths. MAX 7000 devices only.

External AC Timing Characteristics

External AC timing characteristics, called macroparameters, represent actual pin-to-pin timing characteristics. Each macroparameter consists of a combination of internal delay elements (i.e., microparameters). The data sheet for each device gives timing macroparameters that characterize the AC operating specifications. These are worst-case values, derived from extensive performance measurements and guaranteed by testing. The following list defines macroparameters for Classic, MAX 5000, and MAX 7000 devices.

t_{PD1} Dedicated input pin to non-registered output delay. The time required for a signal on any dedicated input pin to propagate through the combinatorial logic in a macrocell and appear at an external device output pin.

t_{PD2} I/O pin input to non-registered output delay. The time required for a signal on any I/O pin input to propagate through the combinatorial logic in a macrocell and appear at an external device output pin.

t_{PZX} Tri-state to active output delay. The time required for an input transition to change an external output from a tri-state (high-impedance) logic level to a valid high or low logic level.

t_{PXZ} Active output to tri-state delay. The time required for an input transition to change an external output from a valid high or low logic level to a tri-state (high-impedance) logic level.

t_{CLR} Time to clear register delay. The time required for a low signal to appear at the external output, measured from the input transition.

t_{SU} Global Clock setup time. The time data must be present at the input pin before the global (synchronous) Clock signal is asserted at the Clock pin.

t_{H} Global Clock hold time. The time the data must be present at the input pin after the global Clock signal is asserted at the Clock pin.

t_{CO1} Global Clock to output delay. The time required to obtain a valid output after the global Clock is asserted at the Clock pin.

t_{CNT} Minimum global Clock period. The minimum period maintained by a globally clocked counter.

t_{ASU} Array Clock setup time. The time data must be present at the input pin before an array (asynchronous) Clock signal is asserted at an input pin.

t_{AH} Array Clock hold time. The time data must be present at the input pin after an array Clock signal is asserted at an input pin.

t_{ACO1} Array Clock to output delay. The time required to obtain a valid output after an array Clock signal is asserted at an input pin.

t_{ACNT} Minimum array Clock period. The minimum period maintained by a counter when it is clocked by a signal from the array.

Timing Models

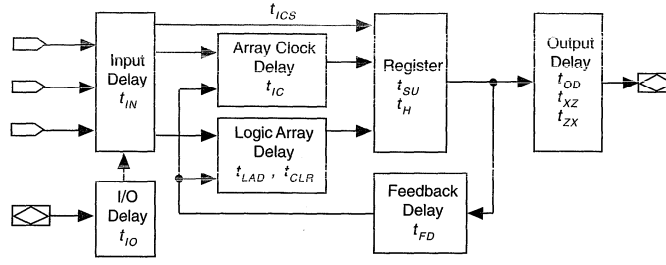
Timing models are simplified block diagrams that illustrate propagation delays through Altera devices. Logic can be implemented on different paths. You can trace the actual paths used in your design by examining the equations listed in the MAX+PLUS II Report File (**.rpt**) for the project. You then add up the appropriate microparameters to calculate the propagation delays through the device.

Classic Devices

The architecture of the EP610, EP610I, EP910, EP910I, and EP1810 Classic devices provides registered and combinatorial capabilities. Registers can be clocked from a global Clock or through an array (product-term) Clock, and can be asynchronously cleared. When the global Clock is used, the Output Enable can be controlled by a product term. Figure 1 shows the timing model for these Classic devices.

Figure 1. EP610, EP610I, EP910, EP910I & EP1810 Device Timing Model

If the register is bypassed, the delay between the logic array and the output buffer is zero.



Tables 1 through 5 show the internal delay parameters for EP610, EP610I, EP910, EP910I, and EP1810 devices.

Table 1. EP610 Internal Timing Parameters (ns)

Parameter	EP610-15	EP610-20	EP610-25	EP610-30	EP610-35
t_{IN}	4	4	8	9	11
t_{IO}	2	2	2	2	2
t_{LAD}	6	11	11	14	15
t_{OD}	5	5	6	7	9
t_{ZX}	5	5	6	7	9
t_{XZ}	5	5	6	7	9
t_{SU}	5	4	11	11	12
t_H	4	7	10	10	10
t_{IC}	6	11	13	16	17
t_{ICS}	2	4	1	1	0
t_{FD}	1	1	3	5	8
t_{CLR}	6	11	13	16	17

Table 2. EP610I Internal Timing Parameters (ns)

Parameter	EP610I-10	EP610I-15	EP610I-25
t_{IN}	1.5	2.0	1.0
t_{IO}	0.0	0.0	0.0
t_{LAD}	5.5	9.0	2.3
t_{OD}	3.0	4.0	1.0
t_{ZX}	8.0	7.0	1.0
t_{XZ}	6.0	7.0	1.0
t_{SU}	3.5	5.0	0.0
t_{H}	3.5	7.0	15.0
t_{IC}	7.5	10.0	18.0
t_{ICS}	2.0	2.0	8.0
t_{FD}	1.0	1.0	2.0
t_{CLR}	8.5	12.0	2.3

Table 3. EP910 Internal Timing Parameters (ns)

Parameter	EP910-30	EP910-35	EP910-40
t_{IN}	9	10	13
t_{IO}	3	3	3
t_{LAD}	14	16	17
t_{OD}	7	9	10
t_{ZX}	7	9	10
t_{XZ}	7	9	10
t_{SU}	12	13	15
t_{H}	12	12	12
t_{IC}	17	19	20
t_{ICS}	2	2	1
t_{FD}	4	6	8
t_{CLR}	17	19	20

Table 4. EP910I Internal Timing Parameters (ns)

Parameter	EP910I-12	EP910I-15	EP910I-25
t_{IN}	1	3	2
t_{IO}	0	0	0
t_{LAD}	8	9	17
t_{OD}	3	3	6
t_{ZX}	6	6	9
t_{XZ}	6	6	9
t_{SU}	4	5	5
t_{H}	4	6	11
t_{IC}	12	10	14
t_{ICS}	4	3	6
t_{FD}	1	1	3
t_{CLR}	11	12	20

Table 5. EP1810 Internal Timing Parameters (ns)

Parameter	EP1810-20	EP1810-25	EP1810-35	EP1810-45
t_{IN}	5	7	7	6
t_{IO}	2	3	5	5
t_{LAD}	9	12	19	28
t_{OD}	6	6	9	11
t_{ZX}	6	6	9	11
t_{XZ}	6	6	9	11
t_{SU}	8	10	10	10
t_{H}	5	7	15	18
t_{IC}	9	12	19	28
t_{ICS}	4	5	4	8
t_{FD}	3	3	6	7
t_{CLR}	9	12	24	32

MAX 5000 Devices

The MAX 5000 architecture supports many functions. The macrocell array provides registered, combinatorial, or flow-through latch operation. The registers can be clocked from a global Clock or through product-term array Clocks, and can be asynchronously preset and cleared. Separate product terms control the Output Enable and logic inversion. The array of shared expander product terms provides additional product terms to implement complex logic.

MAX 5000 devices are divided into single- and multi-LAB devices. Figure 2 shows the timing model for the single-LAB MAX 5000 devices.

Figure 2. Single-LAB MAX 5000 Device Timing Model

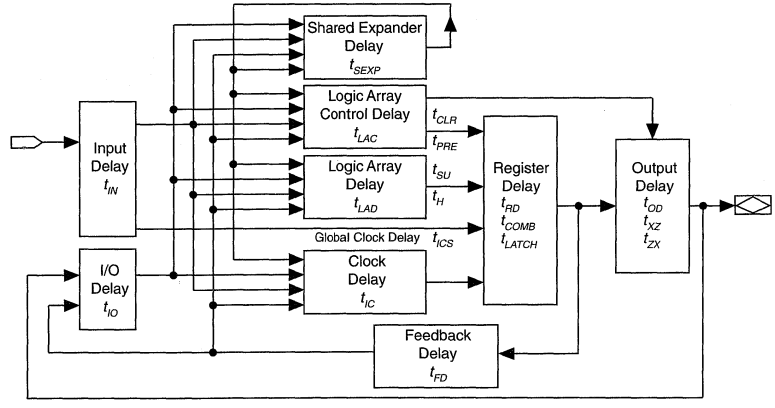
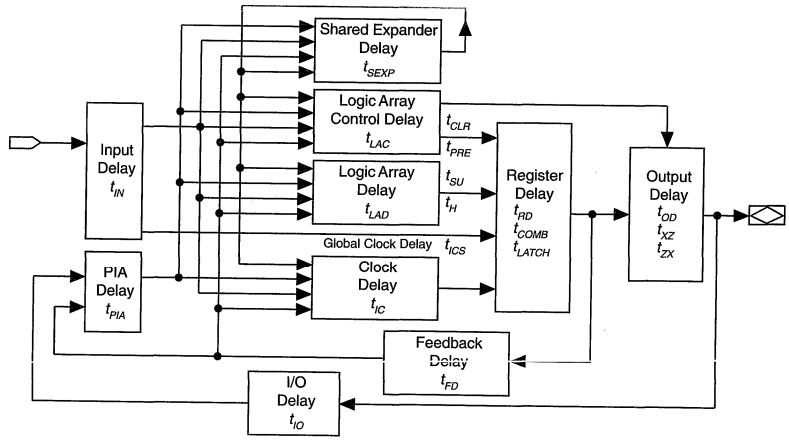


Figure 3 shows the timing model for the multi-LAB MAX 5000 devices: the EPM5064, EPM5064A, EPM5128, EPM5128A, EPM5130, EPM5130A, EPM5192, and EPM5192A devices. In multi-LAB devices, the Programmable Interconnect Array (PIA) routes signals between different LABs. All I/O inputs come into the logic array through the PIA. Signals routed through the PIA incur an additional delay.

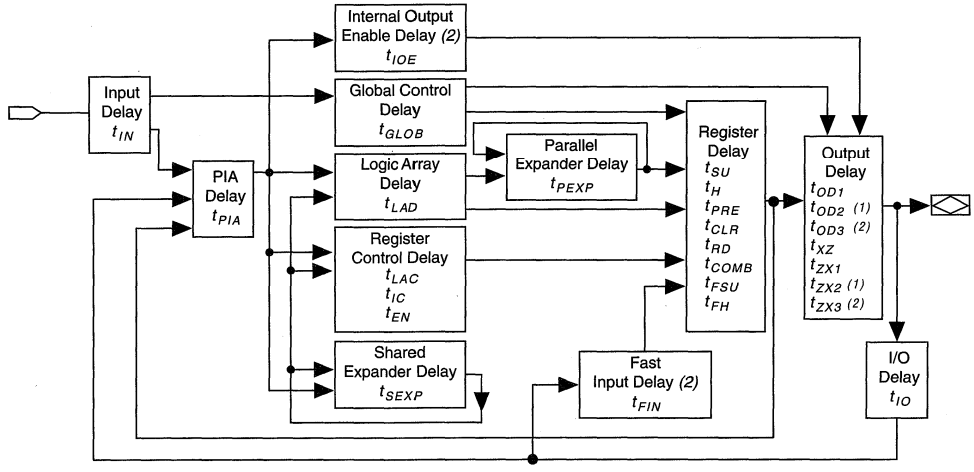
Figure 3. Multi-LAB MAX 5000 Device Timing Model



MAX 7000 Devices

The MAX 7000 architecture differs from the MAX 5000 architecture in several ways. MAX 7000 architecture has globally routed register Clock and Clear and tri-state buffer Output Enable signals. Two types of expander product terms—shared and parallel—can be used to implement complex logic. Each macrocell can be set for low-power operation to reduce power dissipation in the device. Figure 4 shows the timing model for MAX 7000 devices.

Figure 4. MAX 7000 Device Timing Model



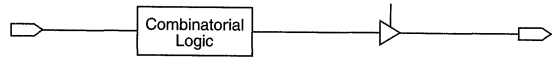
Notes:
(1) Not available in 44-pin devices.
(2) Only available in EPM7128E, EPM7160E, EPM7192E, and EPM7256E devices.

Calculating Timing Delays

You can calculate pin-to-pin timing delays for any device with the appropriate timing model and internal delay parameters. Each AC timing macroparameter is calculated from a combination of internal delays. Figure 5 illustrates the various macroparameters. To calculate the delay for a signal that follows a different path through the device, refer to the timing models shown in Figures 1 through 4 to determine which microparameters to add together.

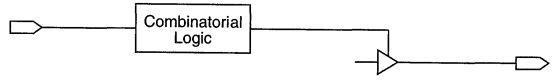
Figure 5. AC Timing Parameters (Part 1 of 3)

Combinatorial Delay

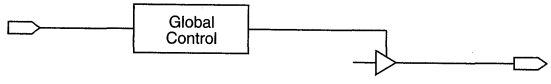


EP610, EP610I, EP910, EP910I, EP1810	$t_{PD1} = t_{IN} + t_{LAD} + t_{OD}$	
	$t_{PD2} = t_{IO} + t_{IN} + t_{LAD} + t_{OD}$	
MAX 5000 (single-LAB)	$t_{PD1} = t_{IN} + t_{LAD} + t_{COMB} + t_{OD}$	
	$t_{PD2} = t_{IO} + t_{LAD} + t_{COMB} + t_{OD}$	
MAX 5000 (multi-LAB)	$t_{PD1} = t_{IN} + t_{LAD} + t_{COMB} + t_{OD}$	
	$t_{PD2} = t_{IO} + t_{PIA} + t_{LAD} + t_{COMB} + t_{OD}$	
MAX 7000	$t_{PD1} = t_{IN} + t_{PIA} + t_{LAD} + t_{COMB} + t_{OD1}$	
	$t_{PD2} = t_{IO} + t_{PIA} + t_{LAD} + t_{COMB} + t_{OD1}$	

Tri-State Enable/Disable Delay



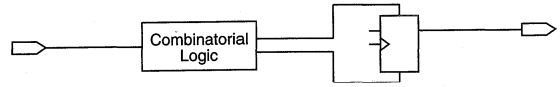
EP610, EP610I, EP910, EP910I, EP1810	$t_{PXZ}, t_{PZX} = t_{IN} + t_{LAD} + (t_{XZ} \text{ or } t_{ZX})$
MAX 5000	$t_{PXZ}, t_{PZX} = t_{IN} + t_{LAC} + (t_{XZ} \text{ or } t_{ZX})$



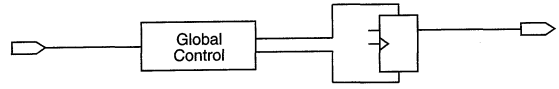
MAX 7000	$t_{PXZ}, t_{PZX} = t_{IN} + t_{GLOB} + (t_{XZ} \text{ or } t_{ZX1})$

Figure 5. AC Timing Parameters (Part 2 of 3)

Register Clear & Preset Time

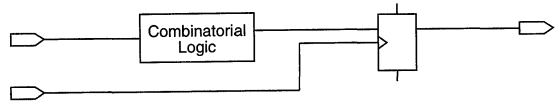


EP610, EP610I, EP910, EP910I, EP1810	t_{CLR}	=	$t_{IN} + t_{CLR} + t_{OD}$
MAX 5000	t_{PRE}, t_{CLR}	=	$t_{IN} + t_{LAC} + (t_{PRE}$ or $t_{CLR}) + t_{OD}$
MAX 7000	t_{PRE}, t_{CLR}	=	$t_{IN} + t_{PIA} + t_{LAC} + (t_{PRE}$ or $t_{CLR}) + t_{OD1}$



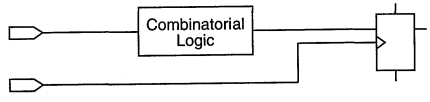
MAX 7000	t_{GCLR}	=	$t_{IN} + t_{GLOB} + t_{CLR} + t_{OD1}$

Setup Time



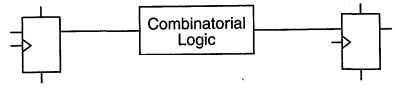
EP610, EP610I, EP910, EP910I, EP1810	t_{SU}	=	$(t_{IN} + t_{LAD}) - (t_{IN} + t_{ICS}) + t_{SU}$
MAX 5000	t_{SU}	=	$(t_{IN} + t_{LAD}) - (t_{IN} + t_{ICS}) + t_{SU}$
MAX 7000	t_{SU}	=	$(t_{IN} + t_{PIA} + t_{LAD}) - (t_{IN} + t_{GLOB}) + t_{SU}$

Hold Time



EP610, EP610I, EP910, EP910I, EP1810	t_{H}	=	$(t_{IN} + t_{ICS}) - (t_{IN} + t_{LAD}) + t_{H}$
MAX 5000	t_{H}	=	$(t_{IN} + t_{ICS}) - (t_{IN} + t_{LAD}) + t_{H}$
MAX 7000	t_{H}	=	$(t_{IN} + t_{GLOB}) - (t_{IN} + t_{PIA} + t_{LAD}) + t_{H}$

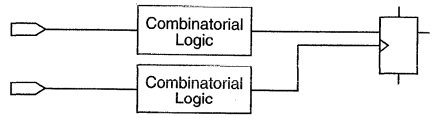
Counter Frequency



EP610, EP610I, EP910, EP910I, EP1810	t_{CNT}	=	$t_{FD} + t_{LAD} + t_{SU}$
MAX 5000	t_{CNT}	=	$t_{RD} + t_{FD} + t_{LAD} + t_{SU}$
MAX 7000	t_{CNT}	=	$t_{RD} + t_{PIA} + t_{LAD} + t_{SU}$

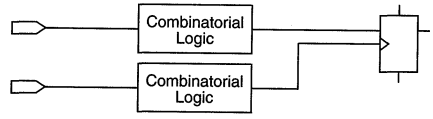
Figure 5. AC Timing Parameters (Part 3 of 3)

Asynchronous Setup Time



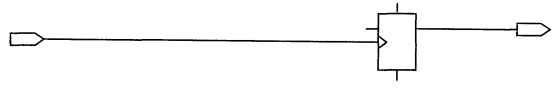
EP610, EP610I, EP910, EP910I, EP1810	t_{ASU}	$= (t_{IN} + t_{LAD}) - (t_{IN} + t_{IC}) + t_{SU}$
MAX 5000	t_{ASU}	$= (t_{IN} + t_{LAD}) - (t_{IN} + t_{IC}) + t_{SU}$
MAX 7000	t_{ASU}	$= (t_{IN} + t_{PIA} + t_{LAD}) - (t_{IN} + t_{PIA} + t_{IC}) + t_{SU}$

Asynchronous Hold Time



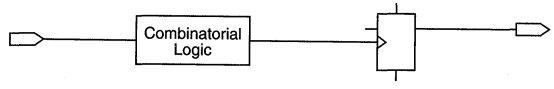
EP610, EP610I, EP910, EP910I, EP1810	t_{AH}	$= (t_{IN} + t_{IC}) - (t_{IN} + t_{LAD}) + t_H$
MAX 5000	t_{AH}	$= (t_{IN} + t_{IC}) - (t_{IN} + t_{LAD}) + t_H$
MAX 7000	t_{AH}	$= (t_{IN} + t_{PIA} + t_{IC}) - (t_{IN} + t_{PIA} + t_{LAD}) + t_H$

Clock-to-Output Delay



EP610, EP610I, EP910, EP910I, EP1810	t_{CO1}	$= t_{IN} + t_{ICS} + t_{OD}$
MAX 5000	t_{CO1}	$= t_{IN} + t_{ICS} + t_{RD} + t_{OD}$
MAX 7000	t_{CO1}	$= t_{IN} + t_{GLOB} + t_{RD} + t_{OD1}$

Array Clock-to-Output Delay



EP610, EP610I, EP910, EP910I, EP1810	t_{ACO1}	$= t_{IN} + t_{IC} + t_{OD}$
MAX 5000	t_{ACO1}	$= t_{IN} + t_{IC} + t_{RD} + t_{OD}$
MAX 7000	t_{ACO1}	$= t_{IN} + t_{PIA} + t_{IC} + t_{RD} + t_{OD1}$

Examples

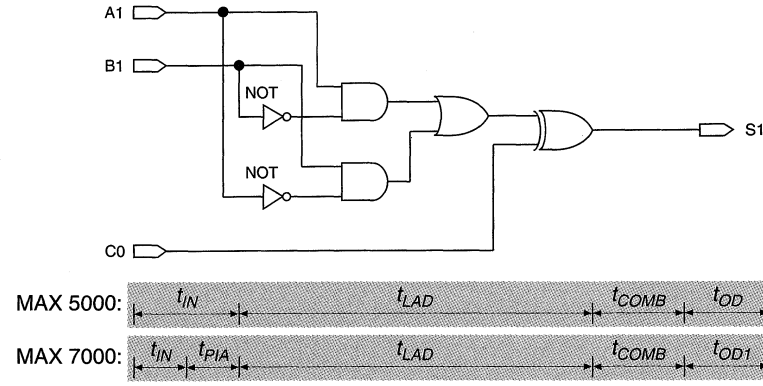
The following examples show how to use microparameters to calculate the delays for real applications.

Example 1: 7483 TTL Macrofunction

You can analyze the timing delays for macrofunctions that have been subjected to minimization and logic synthesis. A MAX+PLUS II Report File (**.rpt**) that includes the optional Equations Section lists the synthesized logic equations. These equations are structured so that you can quickly determine the logic configuration. For example, Figure 6 shows part of a 7483 TTL macrofunction (a 4-bit full adder). The Report File gives the following equations for S1, the least significant bit of the adder:

```
S1      = OUTPUT ( _LC021 , VCC );
_LC021 = LCELL  ( _EQ026 $ C0  );
_EQ026 = B1  & !A1
       # !B1 &  A1;
```

Figure 6. Adder Logic Timing for MAX 5000 & MAX 7000 Architecture



S1 is the output of macrocell 21 (_LC021), which contains combinatorial logic. The combinatorial logic LCELL(_EQ026 $ C0) represents the XOR of the intermediate equation _EQ026 and the carry-in C0. In turn, _EQ026 is logically equivalent to the XOR of inputs B1 and A1. Therefore, the timing delay for S1 in MAX 5000 devices is as follows:

$$t_{IN} + t_{LAD} + t_{COMB} + t_{OD}$$

The timing delay for S1 in MAX 7000 devices is as follows:

$t_{IN} + t_{PIA} + t_{LAD} + t_{COMB} + t_{OD1}$

Example 2: S2 Adder Bit

For complex logic that requires expanders (represented as _X<*number*> in Report Files), the expander array delay, t_{SEXP}, is added to the delay element. The second bit of the 7483 adder macrofunction, S2, requires shared expanders. The equations are:

```
S2      =  _LC019;
_LC019  =  LCELL( _EQ023  $  _EQ024 );
_EQ023  =  _X029  &  _X030  &  _X031;
_X029   =  EXP( !B1  &  !A1 );
_X030   =  EXP( !B1  &  !C0 );
_X031   =  EXP( !A1  &  !C0 );
_EQ024  =  _X032  &  _X033;
_X032   =  EXP( !B2  &  A2  );
_X033   =  EXP(  B2  &  A2  );
```

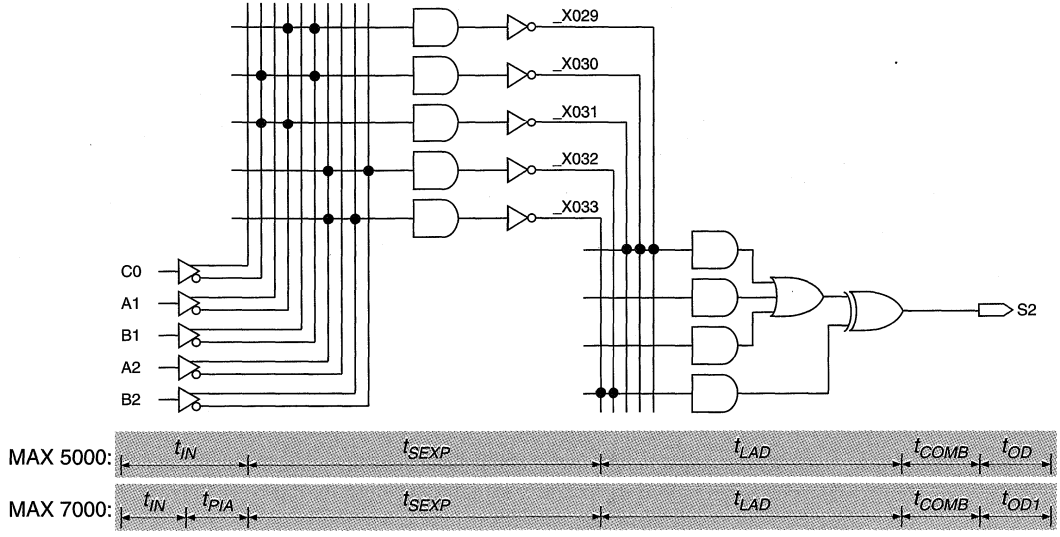
Figure 7 shows how you can map the logic structure onto the MAX 5000 and MAX 7000 architectures with these equations. Therefore, the timing delay for S2 in MAX 5000 devices is as follows:

$t_{IN} + t_{SEXP} + t_{LAD} + t_{COMB} + t_{OD}$

The timing delay for S2 in MAX 7000 devices is as follows:

$t_{IN} + t_{PIA} + t_{SEXP} + t_{LAD} + t_{COMB} + t_{OD1}$

Figure 7. Adder Equations Mapped to MAX 5000 & MAX 7000 Architecture



Example 3: S2 Adder Bit With Parallel Expanders (MAX 7000)

The Compiler implements logic with parallel expanders if the Parallel Expanders logic synthesis option is turned on when a project is compiled for MAX 7000 devices. When parallel expanders are used, no shareable expanders are used, and the timing delay for the S2 bit of the 7483 becomes:

$$t_{IN} + t_{PIA} + t_{LAD} + t_{PEXP} + t_{COMB} + t_{OD1}$$

Example 4: S1 Adder Bit in Low-Power Mode (MAX 7000)

If a macrocell in a MAX 7000 device is set for low-power mode, then you must add the low-power adder delay to the total delay through that macrocell. In Figure 6, the S1 delay thus becomes:

$$t_{IN} + t_{PIA} + t_{LPA} + t_{LAD} + t_{COMB} + t_{OD1}$$

Conclusion

The architectures of Altera devices have fixed internal timing delays that are independent of routing. You can determine the worst-case timing delays for any design before programming a device. Total delay paths (macroparameters) can be expressed as the sums of internal timing delays (microparameters). Timing models illustrate the internal delay paths for devices and show how these microparameters affect each other. You can use MAX+PLUS II development tools to automatically calculate delay paths, or hand-calculate delay paths by adding the microparameters for an appropriate timing model. With this ability to predict worst-case timing delays, you can be confident of a design's in-system timing performance.

Understanding FLEX 8000 Timing

March 1995, ver. 1 Application Brief 143

Introduction

Altera FLEX 8000 devices provide predictable performance that is consistent from simulation to application. Before configuring a device, you can determine worst-case timing delays for any design. You can calculate propagation delays either with the MAX+PLUS II Timing Analyzer, or with the timing models given in this application brief and the timing parameters listed in the *FLEX 8000 Programmable Logic Device Family Data Sheet* in this data book.

☞ For the most precise results, you should use the MAX+PLUS II Timing Analyzer, which accounts for the effects of secondary factors such as placement and fan-out.

This application brief defines device internal delay parameters and AC timing characteristics and shows the timing model for Altera FLEX 8000 devices.

Familiarity with FLEX 8000 architecture and characteristics is assumed. Refer to the *FLEX 8000 Programmable Logic Device Family Data Sheet* in this data book for a complete description of the FLEX 8000 architecture and for specific values for timing parameters.

Internal FLEX 8000 Delay Parameters

Timing delays contributed by individual architectural elements are called internal delay parameters, or microparameters. All microparameters are shown in italics. The following list defines microparameters for FLEX 8000 devices.

t_{IN} I/O input pad and buffer delay. The time required for a signal on an I/O pin used as an input to reach a row or column channel of the FastTrack Interconnect.

t_{DIN_D} Dedicated input data delay. The time required for a signal used as a data input to reach a logic element (LE) from a dedicated input pin. The t_{DIN_D} delay is a function of fan-out and the distance between the source pin and destination LEs. The value shown in the *FLEX 8000 Programmable Logic Device Data Sheet* is the longest delay possible for a pin with a fan-out of four LEs. The value generated by the MAX+PLUS II Timing Analyzer is more accurate because it includes information on the fan-out and

the relative locations of the source pin and destination LEs of the design.

t_{DIN_C} Dedicated input control delay. The delay of a signal coming from a dedicated input pin that is used as an LE register control. These signals include the Clock, Clear, and Preset inputs to the LE register.

t_{DIN_IO} Dedicated input I/O control delay. The delay of a signal from a dedicated input pin that is used as an I/O element (IOE) register control. These signals include the Clock and Clear inputs to the IOE register, in addition to the Output Enable control of the IOE's tri-state buffer.

t_{COL} FastTrack Interconnect column delay. The delay incurred by a signal that requires routing through a column channel in the FastTrack Interconnect.

t_{ROW} FastTrack Interconnect row delay. The delay incurred by a signal that requires routing through a row channel in the FastTrack Interconnect. The t_{ROW} delay is a function of fan-out and the distance between the source and destination LEs. The value shown in the *FLEX 8000 Programmable Logic Device Data Sheet* is the longest delay possible for an LE with a fan-out of four LEs. The value generated by the MAX+PLUS II Timing Analyzer is more accurate because it includes information on the fan-out and the relative locations of the source and destination LEs of the design.

t_{LOCAL} Local interconnect delay. The delay incurred by a signal routed between LEs in the same Logic Array Block (LAB).

$t_{LABCARRY}$ Carry chain delay to the next LAB. The delay incurred by a carry-out signal that carries into the next LAB in the row.

$t_{LABCASC}$ Cascade chain delay to the next LAB. The delay incurred by a cascade-out signal that cascades into the next LAB in the row.

t_{LUT} Look-up table (LUT) delay. The delay incurred by generating an LUT output from a signal from the local LAB interconnect.

t_{RLUT} LUT for LE feedback delay. The time required for the output of an LE to be fed back and used to generate the LUT output in the same LE.

t_{CLUT}	LUT for carry chain delay. The delay incurred by a carry chain signal that is used to generate the LUT output.
t_{CGEN}	Carry-out generation delay. The delay incurred by generating a carry-out signal from a local LAB interconnect signal.
t_{CGENR}	Carry-out generation using LE feedback delay. The delay incurred by generating a carry-out signal from the feedback of the LE.
t_{CICO}	Carry-in, carry-out delay. The delay incurred by generating a carry-out signal that uses the carry-in signal from the previous LE.
t_C	Register control delay. The time required for a signal to be routed to the Clock, Preset, or Clear input of an LE register.
t_{GATE}	Cascade gate delay. The time required for a signal to pass through the cascade-generating AND gate in the LE. This delay is incurred, regardless of whether or not the cascade output is used.
t_{CASC}	Cascade chain delay. The time required for a cascade-out signal to be routed to the next LE in the same LAB. This delay, along with $t_{LABCASC}$, is also used to calculate the delay for a cascade-out signal to be routed to an LE in the next LAB in the row.
t_{CO}	LE Clock-to-output delay. The delay from the rising edge of the LE register's Clock to the time the data appears at the register output.
t_{COMB}	Combinatorial output delay. The time required for a combinatorial signal to bypass the LE register and become the output of the LE.
t_{SU}	LE register setup time. The time that a signal is required to be stable at the LE register input before the register Clock's rising edge to ensure that the register correctly stores the input data.
t_H	LE register hold time. The time that a signal is required to be stable at the LE register input after the register Clock's rising edge to ensure that the register correctly stores the input data.

t_{PRE}	LE register Preset delay. The delay from the assertion of the LE register's asynchronous Preset input to the time the register output stabilizes at a logical high.
t_{CLR}	LE register Clear delay. The delay from the assertion of the LE register's asynchronous Clear input to the time the register output stabilizes at a logical low.
t_{IOD}	Output data delay. The delay incurred by a signal routed from the FastTrack Interconnect to an IOE.
t_{IOC}	IOE control delay. The delay for a signal used to control the I/O register's Clock or Clear input, or for the Output Enable control of the IOE's tri-state buffer.
t_{IOCO}	I/O register Clock-to-output delay. The delay from the rising edge of the I/O register's Clock to the time the data appears at the register output.
t_{IOCOMB}	I/O register bypass delay. The delay for a combinatorial signal to bypass the I/O register.
t_{IOSU}	I/O register setup time. The time required for a signal to be stable at the I/O register input before the register Clock's rising edge to ensure that the register correctly stores the input data.
t_{IOH}	I/O register hold time. The time required for a signal to be stable at the I/O register input after the register Clock's rising edge to ensure that the register correctly stores the input data.
t_{IOCLR}	I/O register Clear delay. The delay from the time the I/O register's asynchronous Clear input is asserted to the time the register output stabilizes at logical low.
t_{OD1}	Output buffer and pad delay with the Slow Slew Rate logic option turned off and V_{CCIO} = 5.0 V.
t_{OD2}	Output buffer and pad delay with the Slow Slew Rate logic option turned off and V_{CCIO} = 3.3 V.
t_{OD3}	Output buffer and pad delay with the Slow Slew Rate logic option turned on.

t_{XZ} Output buffer disable delay. The delay required for high impedance to appear at the output pin after the tri-state buffer's Enable control is disabled.

t_{ZX1} Output buffer Enable delay with the Slow Slew Rate logic option turned off and V_{CCIO} = 5.0 V. The delay required for the output signal to appear at the output pin after the tri-state buffer's Enable control is enabled.

t_{ZX2} Output buffer Enable delay with the Slow Slew Rate logic option turned off and V_{CCIO} = 3.3 V. The delay required for the output signal to appear at the output pin after the tri-state buffer's Enable control is enabled.

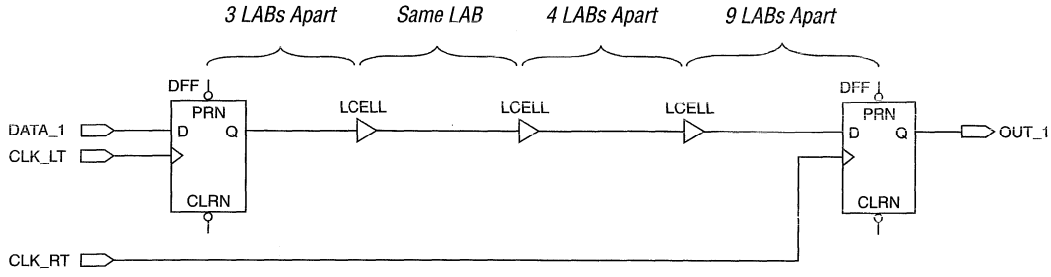
t_{ZX3} Output buffer Enable delay with the Slow Slew Rate logic option turned on and V_{CCIO} = 5.0 V or 3.3 V. The delay required for the output signal to appear at the output pin after the tri-state buffer's Enable control is enabled.

External AC Timing Characteristics

External AC timing characteristics, called macroparameters, represent actual pin-to-pin timing characteristics. Each macroparameter consists of a combination of internal delay elements (microparameters). All macroparameters are shown in bold type. One timing macroparameter, $\mathbf{t_{DRR}}$, characterizes the AC operating specifications. This is a worst-case value, derived from extensive performance measurements and guaranteed by testing. Other macroparameters can be estimated by using the timing model or the equations in "Calculating Timing Delays" later in this application brief.

$\mathbf{t_{DRR}}$ Register-to-register delay. The average time required for the signal from one register to pass through four LEs via three row interconnects and four local interconnects. The test circuit used for this parameter is a register with an output that goes through three LCELL primitives in two different LABs; the last LCELL goes to another register in another LAB. Figure 1 shows this path. The full circuit contains multiple copies of this path, and the registers and LCELL primitives are assigned with the same relationship in each of the paths. That relationship is also described in Figure 1.

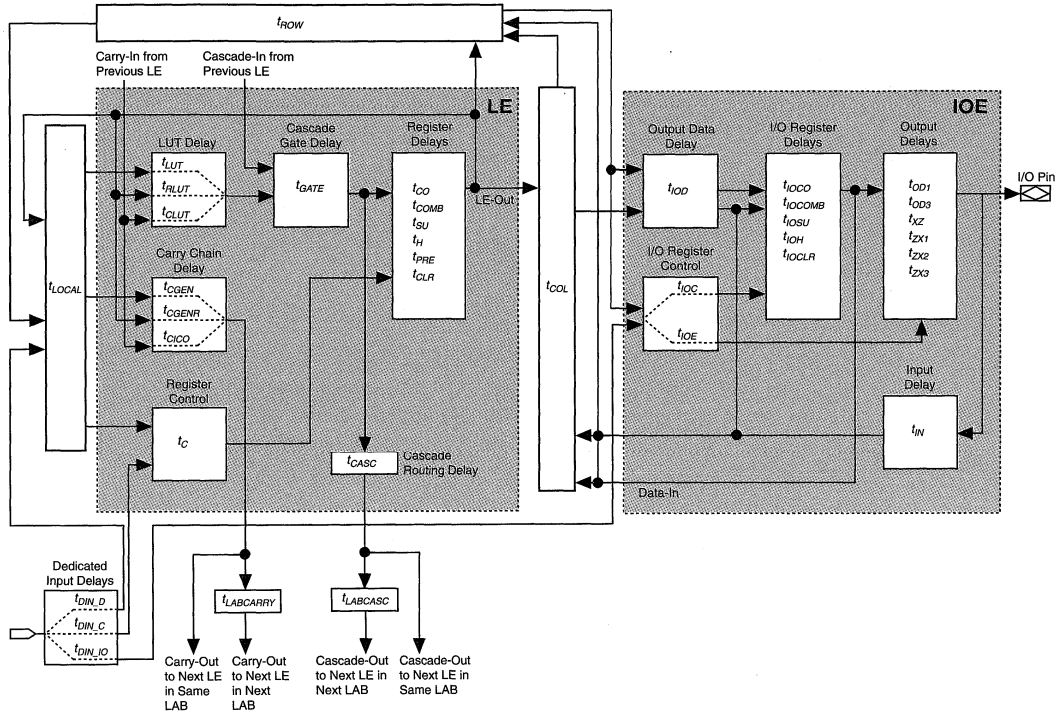
Figure 1. Path for t_{DRR} Circuit for 21-Column Devices



FLEX 8000 Timing Model

Timing models are simplified block diagrams that illustrate propagation delays through Altera devices. Logic can be implemented on different paths. You can trace the actual paths used in your FLEX 8000 device by examining the equations listed in the MAX+PLUS II Report File (**.rpt**) for the project. You can then add up the appropriate microparameters to calculate the approximate propagation delays through the FLEX 8000 device. However, for the most precise delay information, you should use the MAX+PLUS II Timing Analyzer. Figure 2 shows the timing model for FLEX 8000 devices.

Figure 2. FLEX 8000 Timing Model



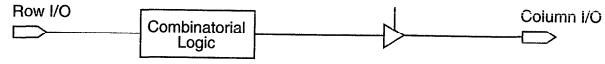
Calculating Timing Delays

You can calculate approximate pin-to-pin timing delays for FLEX 8000 devices with the timing model and the internal delay parameters in the *FLEX 8000 Programmable Logic Device Family Data Sheet* in this data book. Each AC timing macroparameter is calculated from a combination of internal delays. Figure 3 shows the FLEX 8000 family LE macroparameters (shown in bold type). To calculate the delay for a signal that follows a different path through the FLEX 8000 device, refer to the timing model to determine which microparameters (shown in italic type) to add together.

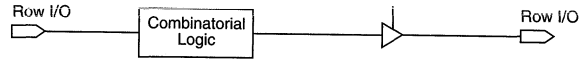
Figure 3. Logic Element AC Timing Parameters (Part 1 of 3)

Combinatorial Delay

t_1



t_2



From I/O Inputs:

$t_1 = t_{IN} + t_{ROW} + t_{LOCAL} + t_{LUT} + t_{GATE} + t_{COMB} + t_{COL} + t_{IOD} + t_{IOCOMB} + t_{OD1}$

$t_2 = t_{IN} + t_{ROW} + t_{LOCAL} + t_{LUT} + t_{GATE} + t_{COMB} + t_{ROW} + t_{IOD} + t_{IOCOMB} + t_{OD1}$

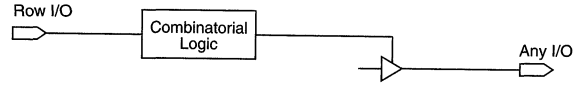
From Dedicated Inputs:

$t_1 = t_{DIN\_D} + t_{LOCAL} + t_{LUT} + t_{GATE} + t_{COMB} + t_{COL} + t_{IOD} + t_{IOCOMB} + t_{OD1}$

$t_2 = t_{DIN\_D} + t_{LOCAL} + t_{LUT} + t_{GATE} + t_{COMB} + t_{ROW} + t_{IOD} + t_{IOCOMB} + t_{OD1}$

Tri-State Enable/Disable Delay

t_{XZ} or t_{ZX}



From Row I/O Inputs:

$t_{XZ}, t_{ZX} = t_{IN} + t_{ROW} + t_{LOCAL} + t_{LUT} + t_{GATE} + t_{COMB} + t_{ROW} + t_{IOC} + (t_{XZ} \text{ or } t_{ZX1})$

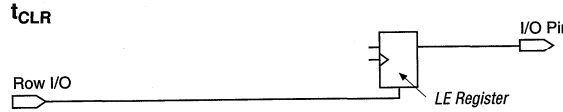
From Dedicated Inputs:

$t_{XZ}, t_{ZX} = t_{DIN\_IO} + t_{IOE} + (t_{XZ} \text{ or } t_{ZX1})$

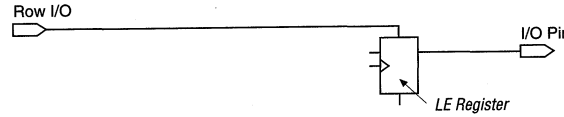
Figure 3. Logic Element AC Timing Parameters (Part 2 of 3)

LE Register Clear & Preset Time

t_{CLR}



t_{PRE}



From I/O Inputs to Row or Column Outputs:

$$t_{CLR} = t_{IN} + t_{ROW} + t_{LOCAL} + t_C + t_{CLR} + (t_{ROW} \text{ or } t_{COL}) + t_{IOD} + t_{IOCOMB} + t_{OD1}$$

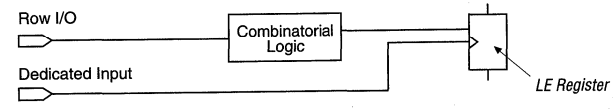
$$t_{PRE} = t_{IN} + t_{ROW} + t_{LOCAL} + t_C + t_{PRE} + (t_{ROW} \text{ or } t_{COL}) + t_{IOD} + t_{IOCOMB} + t_{OD1}$$

From Dedicated Inputs to Row or Column Outputs:

$$t_{CLR} = t_{DIN\_C} + t_C + t_{CLR} + (t_{ROW} \text{ or } t_{COL}) + t_{IOD} + t_{IOCOMB} + t_{OD1}$$

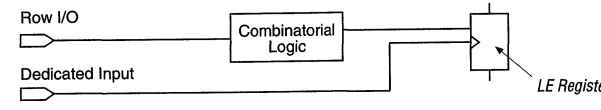
$$t_{PRE} = t_{DIN\_C} + t_C + t_{PRE} + (t_{ROW} \text{ or } t_{COL}) + t_{IOD} + t_{IOCOMB} + t_{OD1}$$

Register Setup Time from a Global Clock & Row I/O Data Input



$$t_{SU} = (t_{IN} + t_{ROW} + t_{LOCAL} + t_{LUT} + t_{GATE}) - (t_{DIN\_C} + t_C) + t_{SU}$$

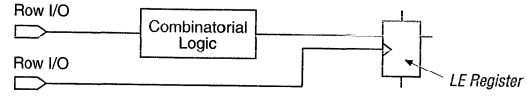
Register Hold Time from a Global Clock & Row I/O Data Input



$$t_H = (t_{DIN\_C} + t_C) - (t_{IN} + t_{ROW} + t_{LOCAL} + t_{LUT} + t_{GATE}) + t_H$$

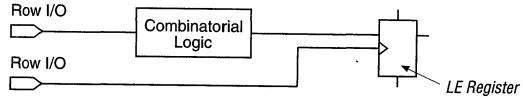
Figure 3. Logic Element AC Timing Parameters (Part 3 of 3)

Asynchronous Setup Time from a Row I/O Clock & Row I/O Data Input



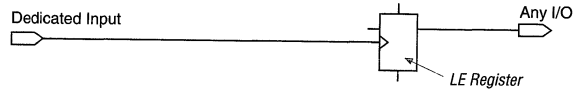
$$t_{ASU} = (t_{IN} + t_{ROW} + t_{LOCAL} + t_{LUT} + t_{GATE}) - (t_{IN} + t_{ROW} + t_{LOCAL} + t_{C}) + t_{SU}$$

Asynchronous Hold Time from a Row I/O Clock & Row I/O Data Input



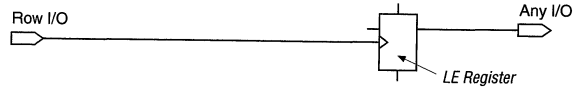
$$t_{AH} = (t_{IN} + t_{ROW} + t_{LOCAL} + t_{C}) - (t_{IN} + t_{ROW} + t_{LOCAL} + t_{LUT} + t_{GATE}) + t_{H}$$

Clock-to-Output Delay from a Global Clock to Any Output



$$t_{CO} = t_{DIN\_C} + t_{C} + t_{CO} + (t_{ROW} \text{ or } t_{COL}) + t_{IOD} + t_{IOCOMB} + t_{OD1}$$

Asynchronous Clock-to-Output Delay from a Row I/O Clock to Any Output



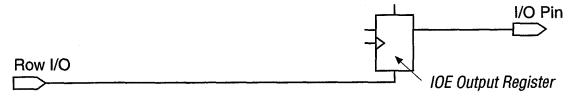
$$t_{ACO} = t_{IN} + t_{ROW} + t_{LOCAL} + t_{C} + t_{CO} + (t_{ROW} \text{ or } t_{COL}) + t_{IOD} + t_{IOCOMB} + t_{OD1}$$

Figure 4 shows the FLEX 8000 family I/O element macroparameters. To calculate the delay for a signal that follows a different path through the FLEX 8000 device, refer to the timing model to determine which microparameters to add together.

Figure 4. I/O Element AC Timing Parameters (Part 1 of 2)

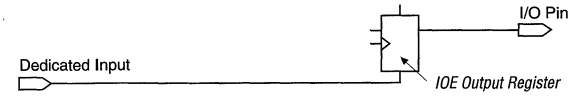
I/O Element Clear Time

From I/O Inputs:



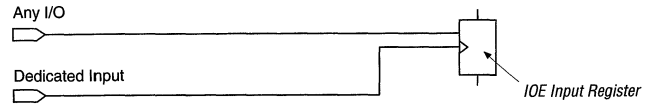
$$t_{CLR} = t_{IN} + t_{ROW} + t_{IOC} + t_{IOCLR} + t_{OD1}$$

From Dedicated Inputs:



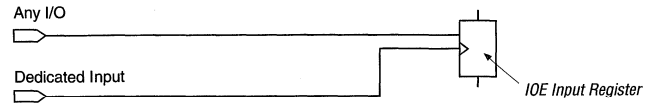
$$t_{CLR} = t_{DIN\_IO} + t_{IOC} + t_{IOCLR} + t_{OD1}$$

Register Setup Time from a Global Clock & Row I/O Data Input



$$t_{SU} = t_{IN} - (t_{DIN\_IO} + t_{IOC}) + t_{IOSU}$$

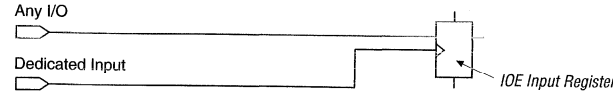
Register Hold Time from a Global Clock & Row I/O Data Input



$$t_{H} = (t_{DIN\_C} + t_{IOC}) - t_{IN} + t_{H}$$

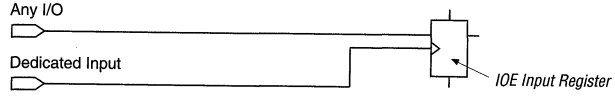
Figure 4. I/O Element AC Timing Parameters (Part 2 of 2)

Asynchronous Setup Time from a Row I/O Clock & Row I/O Data Input



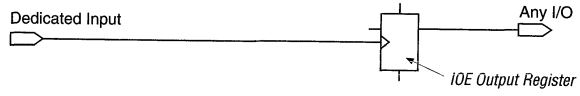
$$t_{ASU} = t_{IN} - (t_{IN} + t_{ROW} + t_{IOC}) + t_{SU}$$

Asynchronous Hold Time from a Row I/O Clock & Row I/O Data Input



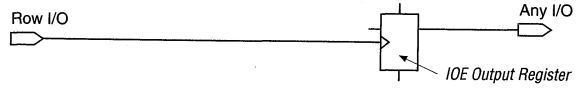
$$t_{AH} = (t_{IN} + t_{ROW} + t_{IOC}) - t_{IN} + t_{H}$$

Clock-to-Output Delay from a Global Clock to Any Output



$$t_{CO} = t_{DIN\_IO} + t_{IOC} + t_{IOCO} + t_{OD1}$$

Asynchronous Clock-to-Output Delay from a Row I/O Clock to Any Output



$$t_{ACO} = t_{IN} + t_{ROW} + t_{IOC} + t_{IOCO} + t_{OD1}$$

Timing Model vs. MAX+PLUS II Timing Analyzer

The MAX+PLUS II Timing Analyzer always provides the most accurate information on the performance of a design. However, hand calculations based on the timing model also provide a good estimate of the design performance. The MAX+PLUS II Timing Analyzer is more accurate because it takes into account three secondary factors that influence the t_{ROW} and t_{DIN_D} parameters:

- Fan-out for each signal in the delay path
- Positions of other loads relative to the source and destination
- Distance between signal source and destination

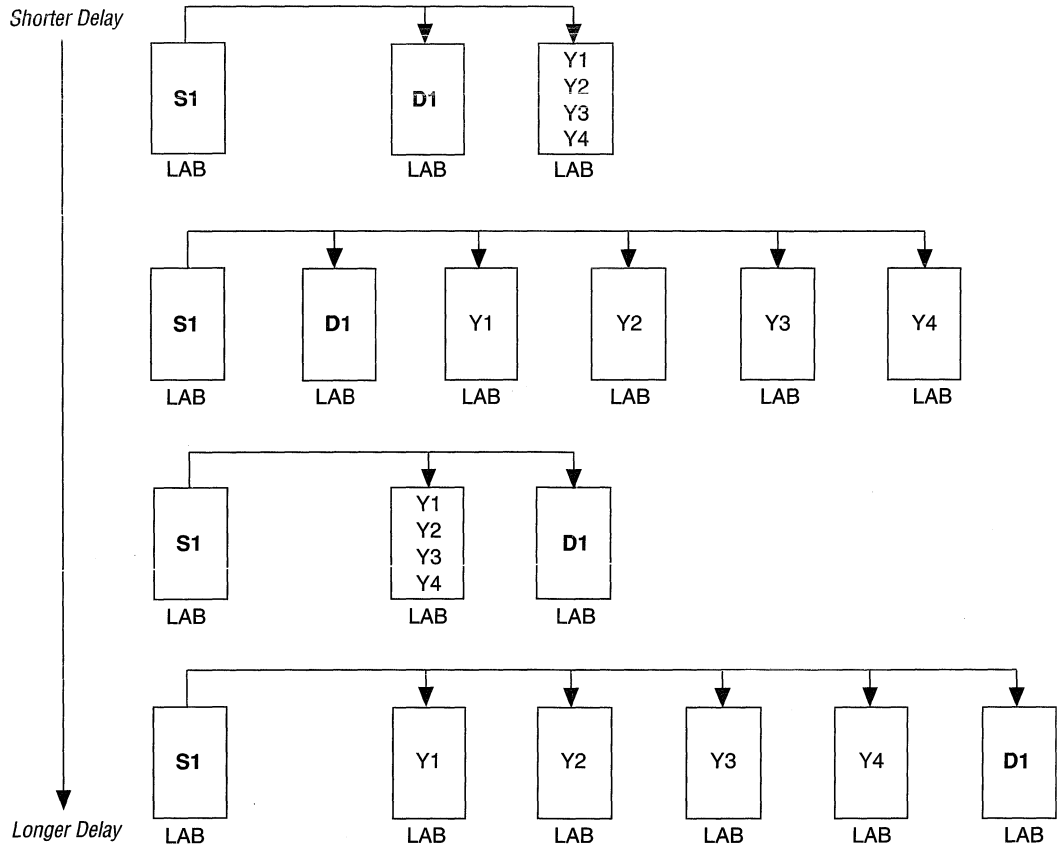
Fan-Out

The more loads a signal has to drive, the longer the delay across t_{ROW} and t_{DIN_D}. This loading is a function of the number of LABs that a signal source has to drive, as well as of the number of LEs in the LAB that use the signal. The number of LABs that a signal drives has a greater effect on the delay than the number of cells in the LAB that use the signal. For example, a signal `S1` feeds destination `D1` and feeds logic elements `Y[4..1]`. If `Y[4..1]` are in different LABs, then `S1` has four loads. If, however, they are all in the same LAB, then `S1` still has four loads, but has a shorter delay. Therefore, the delay from `S1` to `D1` is greater when each signal `Y[4..1]` is in a different LAB.

Load Distribution

The load distribution relative to the source and destination also affects the t_{ROW} and t_{DIN_D} delays. Figure 5 illustrates the change in the t_{ROW} and t_{DIN_D} delays caused by variations in the position of `D1` and the distribution of `Y[1..4]`.

Figure 5. Effect of Relative Position & Load Distribution on t_{ROW}



Distance

The distance between the source and destination LEs also affects the timing of t_{ROW} and t_{DIN_D}. For example, if S1 and D1 are pins on the left and right sides of a device, respectively, then the delay through one LCELL on the same row (i.e., the time required to traverse the length of the device) is the same no matter where the LCELL is placed. If, on the other hand, S1 and D1 are both on the left side, then the delay from S1 to D1 depends on where the LCELL is placed. If the LCELL is on the right side (far from S1 and D1), then the delay is longer than if it is on the left side (close to S1 and D1).

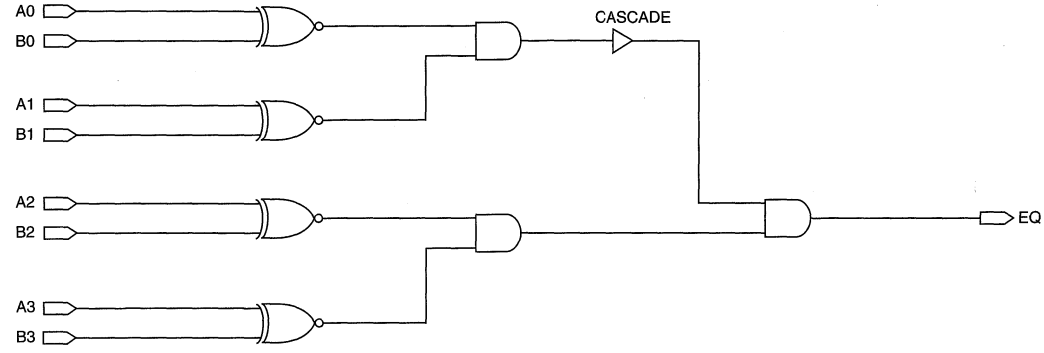
Examples

The following examples show how to use microparameters to estimate the delays for real applications.

Example 1: 4-Bit Equality Comparator with Cascade

You can analyze the timing delays for circuits that have been subjected to minimization and logic synthesis. The synthesized equations can be found in the MAX+PLUS II Report File (**.rpt**) for the project. These equations are structured so that you can quickly determine the logic configuration of any signal. For example, Figure 6 shows a 4-bit equality comparator.

Figure 6. 4-Bit Equality Comparator Circuit



The Report File for this circuit gives the equations for EQ, the output of the comparator:

```
EQ       =  _LC2_B1;
_LC2_B1  =  LCELL( _EQ002C);
_EQ002C  =  _EQ002 & CASCADE( _EQ001C);
_EQ002   =  A2 & A3 & B2 & B3
            # A2 & !A3 & B2 & !B3
            # !A2 & A3 & !B2 & B3
            # !A2 & !A3 & !B2 & !B3;
```

The equation for _EQ001C cascades into the previous equation:

```
% _LC1_B1 =  LCELL( _EQ001C); %
_EQ001C   =  _EQ001;
_EQ001    =  A0 & A1 & B0 & B1
             # A0 & !A1 & B0 & !B1
             # !A0 & A1 & !B0 & B1
             # !A0 & !A1 & !B0 & !B1;
```

The output pin, EQ, is the output of the second LE of a cascade chain. The combinatorial LE, _LC1_B1, implements the comparison of the first two bits. The second two bits are implemented in the LUT of _LC2_B1. The outputs of these two LEs are then cascaded together to form the output of _LC2_B1.

If A2 and EQ are row I/O pins, then the timing delay from A2 to EQ can be estimated by adding the following parameters:

$$t_{IN} + t_{ROW} + t_{LOCAL} + t_{LUT} + t_{GATE} + t_{COMB} + t_{ROW} + t_{IOD} + t_{IOCOMB} + t_{OD1}$$

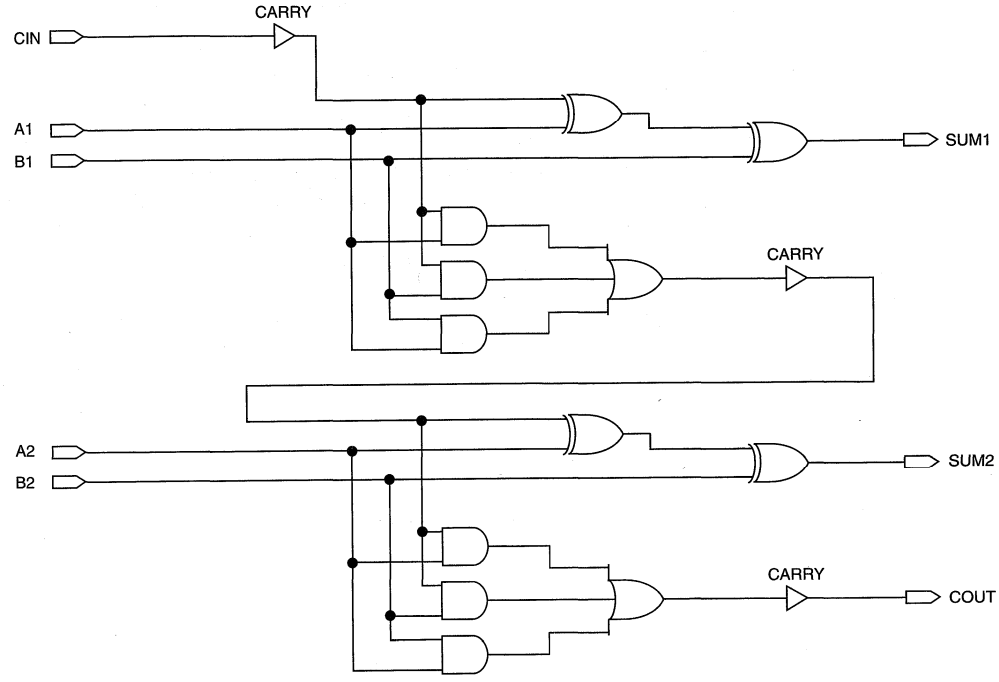
If A0 is a row I/O pin, the timing delay from A0 to EQ can be estimated by adding the following parameters:

$$t_{IN} + t_{ROW} + t_{LOCAL} + t_{LUT} + t_{GATE} + t_{CASC} + t_{GATE} + t_{COMB} + t_{ROW} + t_{IOD} + t_{IOCOMB} + t_{OD1}$$

Example 2: 2-Bit Adder Using Carry Chain

FLEX 8000 devices have specialized resources that implement complex arithmetic functions. For instance, adders and counters require a carry function to determine whether or not to increment the next significant bit. The FLEX 8000 architecture has a built-in carry chain that performs this function. The following example explains how to estimate the delay for a 2-bit adder that uses the carry chain, shown in Figure 7.

Figure 7. 2-Bit Adder Implemented with a Carry Chain



The MAX+PLUS II Report File contains the following equations for the 2-bit adder:

```
COUT            =  _LC4_B1;
SUM1            =  _LC2_B1;
SUM2            =  _LC3_B1;
_LC2_B1         =  LCELL( _EQ001);
_EQ001          =  !A1 & !B1 & _LC1_B1_CARRY
                   # A1 & !B1 & !_LC1_B1_CARRY
                   # A1 & B1 & _LC1_B1_CARRY
                   # !A1 & B1 & !_LC1_B1_CARRY;
_LC2_B1_CARRY   =  CARRY( _EQ002);
_EQ002          =  A1 & B1
                   # A1 & _LC1_B1_CARRY
                   # B1 & _LC1_B1_CARRY;
_LC3_B1         =  LCELL( _EQ003);
_EQ003          =  A2 & B2 & _LC2_B1_CARRY
                   # !A2 & B2 & !_LC2_B1_CARRY
                   # !A2 & !B2 & _LC2_B1_CARRY
                   # A2 & !B2 & !_LC2_B1_CARRY;
```

```
_LC4_B1          =  LCELL( _LC3_B1_CARRY);
_LC3_B1_CARRY    =  CARRY( _EQ004);
_EQ004           =  B2 & _LC2_B1_CARRY
                    # A2 & B2
                    # A2 & _LC2_B1_CARRY;
_LC1_B1_CARRY    =  CARRY( CIN);
```

The CIN input carries into _LC2_B1, and the output of the LE _LC2_B1 is SUM1 and _LC2_B1_CARRY. These signals are then used to generate SUM2 and _LC3_B1_CARRY. The output pin, COUT, must pass through the LCELL _LC4_B1 because a CARRY buffer cannot directly feed a pin.

If CIN to SUM1 are on a row IOE, the pin-to-pin delay between them can be estimated by adding the following parameters:

$t_{IN} + t_{ROW} + t_{LOCAL} + t_{CGEN} + t_{CLUT} + t_{GATE} + t_{COMB} + t_{ROW} + t_{IOD} + t_{IOCOMB} + t_{OD1}$

If CIN to COUT are on a row IOE, the pin-to-pin delay between them can be estimated by adding the following parameters:

$t_{IN} + t_{ROW} + t_{LOCAL} + t_{CGEN} + t_{CICO} + t_{CICO} + t_{CLUT} + t_{GATE} + t_{COMB} + t_{ROW} + t_{IOD} + t_{IOCOMB} + t_{OD1}$

Conclusion

The FLEX 8000 architecture has predictable internal timing delays that can be estimated based on signal synthesis and placement. With the FLEX 8000 timing model and the individual device parameters in the *FLEX 8000 Programmable Logic Device Family Data Sheet*, you can estimate the performance of a design before compilation. For the most accurate timing data, the MAX+PLUS II Timing Analyzer calculates delays based on secondary factors, such as capacitive loading and the distance across the FastTrack Interconnect. These methods enable you to accurately predict your design's in-system timing performance.

Understanding MAX 9000 Timing

March 1995, ver. 1 Application Brief 144

Introduction

Altera MAX 9000 devices provide predictable device performance that is consistent from simulation to application. Before placing a device in a circuit, you can determine the worst-case timing delays for any design. You can calculate propagation delays either with the MAX+PLUS II Timing Analyzer or with the timing models given in this application brief and the timing parameters listed in the *MAX 9000 Programmable Logic Device Family Data Sheet* in this data book.

☞ For the most precise results, you should use the MAX+PLUS II Timing Analyzer, which accounts for the effects of secondary factors such as placement and fan-out.

This application brief defines device internal delay parameters and external AC timing characteristics, and illustrates the timing model for the MAX 9000 family.

Familiarity with MAX 9000 architecture and characteristics is assumed. Refer to the *MAX 9000 Programmable Logic Device Family Data Sheet* in this data book for a complete description of the MAX 9000 architecture and for specific values for the timing parameters listed in this application brief.

Internal MAX 9000 Delay Parameters

Timing delays contributed by individual MAX 9000 architectural elements are called microparameters. Microparameters cannot be measured explicitly. All microparameters are shown in italics. The following list defines the microparameters for the MAX 9000 family.

t_{INCOMB} I/O input pad and buffer delay. This delay applies to I/O pins used as inputs. It is the time required for a signal on an I/O pin to reach a row or column interconnect of the FastTrack Interconnect.

t_{INREG} I/O input pad to I/O register delay. This delay applies to I/O pins used as inputs. It is the time required for a signal on an I/O pin to reach the data input of an I/O register.

t_{DIN_D} Dedicated input data delay. The time required for a signal that originates from a dedicated input pin and is used as a data input to a macrocell to reach a row interconnect on the FastTrack Interconnect.

t_{DIN_CLK}	Dedicated input Clock delay. The delay for a signal that originates from a dedicated input pin and that is used as a macrocell register Clock.
t_{DIN_CLR}	Dedicated input Clear delay. The delay for a signal that originates from a dedicated input pin and that is used as a macrocell register Clear.
t_{DIN_IO}	Dedicated input I/O control delay. The delay for a signal that originates from a dedicated input pin (including the Enable and Clear inputs to the I/O register and the Output Enable control of the I/O cell's tri-state buffer) and is used as an I/O register control.
t_{DIN_IOC}	Dedicated input I/O Clock delay. The delay for a signal that originates from a dedicated input pin and that is used as an I/O register Clock.
t_{COL}	FastTrack Interconnect column delay. The delay incurred by a signal that requires routing through a column interconnect. The t_{COL} delay is a function of fan-out and of the distance between the source and destination macrocells and is a worst-case value for most column signals.
t_{ROW}	FastTrack Interconnect row delay. The delay incurred by a signal that requires routing through a row interconnect. The t_{ROW} delay is a function of fan-out and of the distance between the source and destination macrocells and is a worst-case value for most row signals.
t_{LOCAL}	LAB local array delay. The delay incurred by a signal that is routed from one macrocell to another macrocell in the same Logic Array Block (LAB).
t_{LAD}	Logic array delay. The time required for a logic signal to propagate through a macrocell's AND-OR-XOR structure.
t_{LAC}	Logic array control delay. The AND array delay for register control functions, including the Clear and Preset inputs to the macrocell register.
t_{IC}	Array Clock delay. The delay through a macrocell's Clock product term to the register's Clock input.
t_{EN}	Register Enable delay. The AND array delay for the macrocell register Enable.

t_{SEXP}	Shared expander delay. The delay of a signal through the AND-NOT structure of the shared expander product-term array that is fed back into the local array.
t_{PEXP}	Parallel expander delay. The additional delay incurred by adding parallel expander product terms to the macrocell product terms. For each group of up to five parallel expanders added to a macrocell, an additional t_{PEXP} delay is added to the timing path.
t_{RD}	Macrocell Clock-to-output delay. The delay from the rising edge of the macrocell register's Clock to the time the data appears at the register output.
t_{COMB}	Macrocell combinatorial output delay. The delay required for a signal to bypass the macrocell register and become the macrocell output.
t_{SU}	Macrocell register setup time. The time required for a signal to be stable at the macrocell register input before the register Clock's rising edge to ensure that the register correctly stores the input data.
t_{H}	Macrocell register hold time. The time required for a signal to be stable at the macrocell register input after the register Clock's rising edge to ensure that the register correctly stores the input data.
t_{PRE}	Macrocell register Preset delay. The delay from the assertion of the macrocell register's asynchronous Preset input to the stabilization of the register output at logical high.
t_{CLR}	Macrocell register Clear delay. The delay from the assertion of the macrocell register's Clear input to the stabilization of the register output at logical low.
t_{FTD}	FastTrack Interconnect drive delay. The delay from the time when a signal is available on the macrocell output to the time that signal is driven onto the row or column interconnect.
t_{IODR}	Output data delay for the row. The delay incurred by signals routed from a row to an I/O cell.
t_{IODC}	Output data delay for the column. The delay incurred by signals routed from a column to an I/O cell.

t_{IOC}	I/O cell control delay. The delay for a signal that controls the I/O register's Enable or Clear input, or for the signal that controls the Output Enable of the I/O cell's tri-state buffer.
t_{IORD}	I/O register Clock-to-output delay. The delay from the rising edge of the I/O register's Clock to the time the data appears at the register output.
t_{IOCOMB}	I/O register bypass delay. The delay for a signal to bypass the I/O register.
t_{IOSU}	I/O register setup time. The time required for a signal to be stable at the I/O register input before the register Clock's rising edge to ensure that the register correctly stores the input data.
t_{IOH}	I/O register hold time. The time required for a signal to be stable at the I/O register input after the register Clock's rising edge to ensure that the register correctly stores the input data.
t_{IOCLR}	I/O register Clear delay. The delay from the time when the I/O register's asynchronous Clear input is asserted to the time the register output stabilizes at logical low.
t_{IOFD}	I/O register feedback delay. The delay from the output of the I/O register to the row and column interconnect.
t_{OD1}	Output buffer and pad delay with the Slow Slew Rate logic option turned off and V_{CCIO} = 5.0 V.
t_{OD2}	Output buffer and pad delay with the Slow Slew Rate logic option turned off and V_{CCIO} = 3.3 V.
t_{OD3}	Output buffer and pad delay with the Slow Slew Rate logic option turned on.
t_{XZ}	Output buffer disable delay. The delay required for high impedance to appear at the output pin after the tri-state buffer's Enable control is disabled.
t_{ZX1}	Output buffer Enable delay with the Slow Slew Rate logic option turned off and V_{CCIO} = 5.0 V. The delay required for the output signal to appear at the output pin after the tri-state buffer's Enable control is enabled.

t_{ZX2} Output buffer Enable delay with the Slow Slew Rate logic option turned off and V_{CCIO} = 3.3V. The delay required for the output signal to appear at the output pin after the tri-state buffer's Enable control is enabled.

t_{ZX3} Output buffer Enable delay with the Slow Slew Rate logic option turned on and V_{CCIO} = 5.0 V or 3.3 V. The delay required for the output signal to appear at the output pin after the tri-state buffer's Enable control is enabled.

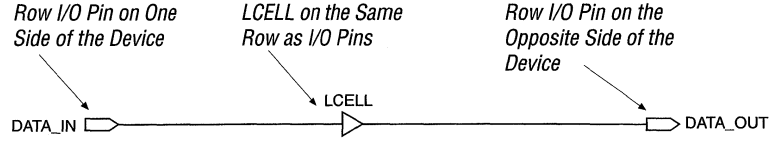
t_{LPA} Low-power adder. The delay associated with macrocells in low-power operation. In low-power mode, t_{LPA} must be added to the LAB local array delay (t_{LOCAL}).

External AC Timing Characteristics

External AC timing characteristics, called macroparameters, represent actual pin-to-pin timing characteristics. Each macroparameter consists of a combination of internal delay elements (microparameters). These macroparameters are worst-case values, derived from extensive performance measurements and guaranteed by testing. All macroparameters are shown in bold. The following list defines macroparameters for the MAX 9000 family.

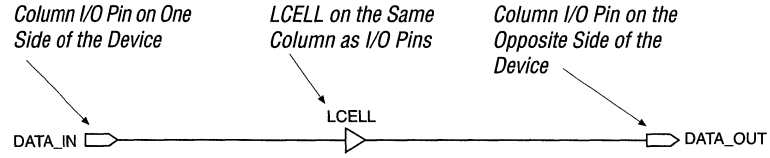
t_{PD1} Row I/O pin to non-registered row pin delay. The time required for a signal on any row input to propagate through the combinatorial logic in a macrocell and appear at a row output pin. The test circuit for this parameter is a row input pin on one side of the device that feeds a row output on the opposite side of the device through an LCELL in that row. See Figure 1.

Figure 1. Test Circuit for t_{PD1}



t_{PD2} Column I/O pin to non-registered column pin delay. The time required for a signal on any column input to propagate through the combinatorial logic in a macrocell and appear at a column output pin. The test circuit for this parameter is a column input pin on one side of the device that feeds a column output on the opposite side of the device through an LCELL in that column. See Figure 2.

Figure 2. Test Circuit for t_{PD2}



t_{FSU} Global Clock setup time for I/O register. The time the input data must be present at the I/O pin before the global (synchronous) Clock signal is asserted at the Clock pin.

t_{FH} Global Clock hold time for I/O register. The time the input data must be present at the I/O pin after the global Clock signal is asserted at the Clock pin.

t_{CO} Global Clock to output delay for macrocell registers. The time required to obtain a valid row output after the global Clock is asserted at the Clock pin.

t_{FCO} Global Clock to output delay for I/O register. The time required to obtain a valid output after the global Clock is asserted at the Clock pin.

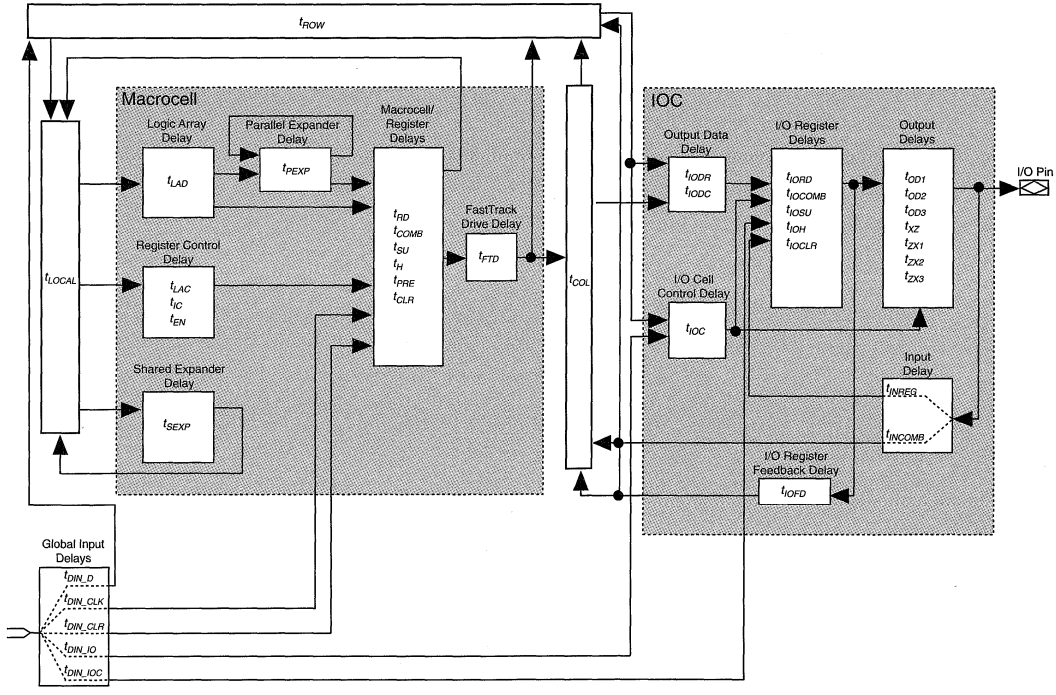
t_{CNT} Minimum global Clock period. The minimum period maintained by a globally clocked 16-bit loadable, enabled, up/down counter.

t_{ACNT} Minimum array Clock period. The minimum period maintained by a 16-bit loadable, enabled, up/down counter when it is clocked by a signal from the array.

MAX 9000 Timing Model

Timing models are simplified block diagrams that illustrate propagation delays through Altera devices. Logic can be implemented in different paths. You can trace the actual paths used in your MAX 9000 device by examining the equations listed in the MAX+PLUS II Report File (**.rpt**) for the project. You can then add up the appropriate microparameters to calculate the approximate propagation delays through the MAX 9000 device. However, the MAX+PLUS II Timing Analyzer provides the most accurate information. The timing model for the MAX 9000 family is shown in Figure 3.

Figure 3. MAX 9000 Timing Model



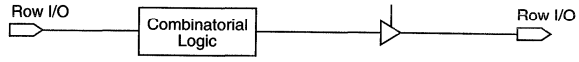
Calculating Timing Delays

You can calculate approximate pin-to-pin timing delays for MAX 9000 devices with the timing model shown in Figure 3 and the internal delay parameters from the *MAX 9000 Programmable Logic Device Family Data Sheet* in this data book. Figure 4 shows the MAX 9000 family macrocell macroparameters (shown in bold type). To calculate the delay for a signal that follows a different path through the MAX 9000 device, refer to the timing model to determine which microparameters (shown in italic type) to add together.

Figure 4. Macrocell AC Timing Parameters (Part 1 of 3)

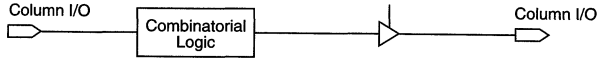
Combinatorial Delay

From Row I/O Inputs to Row I/O Outputs:



$$t_{PD1} = t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{LAD} + t_{COMB} + t_{FTD} + t_{ROW} + t_{IODR} + t_{IOCOMB} + t_{OD1}$$

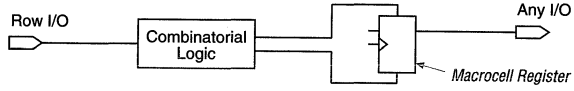
From Column I/O Inputs to Column I/O Outputs:



$$t_{PD2} = t_{INCOMB} + t_{COL} + t_{ROW} + t_{LOCAL} + t_{LAD} + t_{COMB} + t_{FTD} + t_{COL} + t_{IODC} + t_{IOCOMB} + t_{OD1}$$

Macrocell Register Clear & Preset Time

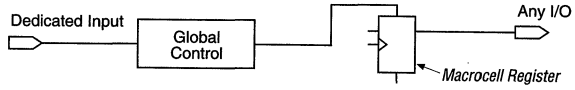
From Row I/O Inputs to Row or Column Outputs:



$$t_{CLR} = t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{LAC} + t_{CLR} + t_{FTD} + (t_{ROW} \text{ or } t_{COL}) + (t_{IODR} \text{ or } t_{IODC}) + t_{IOCOMB} + t_{OD1}$$

$$t_{PRE} = t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{LAC} + t_{PRE} + t_{FTD} + (t_{ROW} \text{ or } t_{COL}) + (t_{IODR} \text{ or } t_{IODC}) + t_{IOCOMB} + t_{OD1}$$

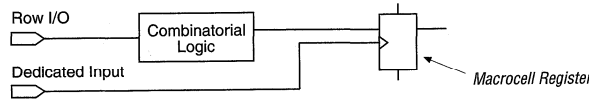
From Dedicated Inputs to Row or Column Outputs:



$$t_{CLR} = t_{DIN\_CLR} + t_{CLR} + t_{FTD} + (t_{ROW} \text{ or } t_{COL}) + (t_{IODR} \text{ or } t_{IODC}) + t_{IOCOMB} + t_{OD1}$$

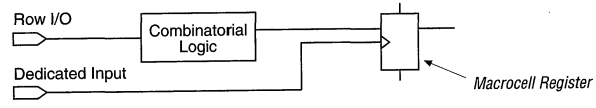
Figure 4. Macrocell AC Timing Parameters (Part 2 of 3)

Register Setup Time from a Global Clock & Row I/O Data Input



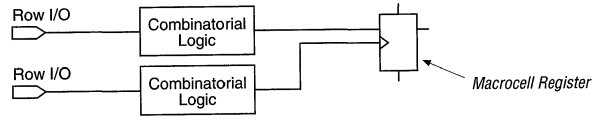
$$t_{SU} = (t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{LAD}) - t_{DIN\_CLK} + t_{SU}$$

Register Hold Time from a Global Clock & Row I/O Data Input



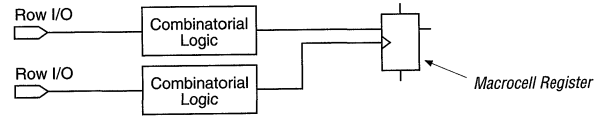
$$t_{H} = t_{DIN\_CLK} - (t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{LAD}) + t_{H}$$

Asynchronous Setup Time from a Row I/O Clock & Row I/O Data Input



$$t_{ASU} = (t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{LAD}) - (t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{IC}) + t_{SU}$$

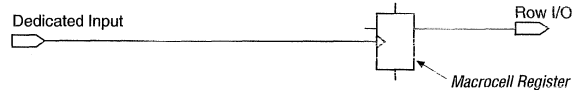
Asynchronous Hold Time from a Row I/O Clock & Row I/O Data Input



$$t_{AH} = (t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{IC}) - (t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{LAD}) + t_{H}$$

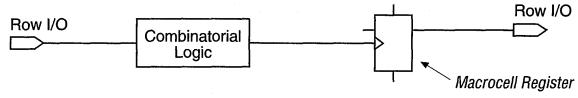
Figure 4. Macrocell AC Timing Parameters (Part 3 of 3)

Clock-to-Output Delay from a Global Clock & Row Output



$$t_{CO} = t_{DIN\_CLK} + t_{RD} + t_{FTD} + t_{ROW} + t_{IODR} + t_{IOCOMB} + t_{OD1}$$

Asynchronous Clock-to-Output Delay from a Row I/O Clock & Row Output



$$t_{ACO} = t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{IC} + t_{RD} + t_{FTD} + t_{ROW} + t_{IODR} + t_{IOCOMB} + t_{OD1}$$

Counter Frequency

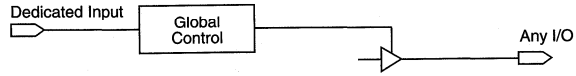
$$t_{CNT} = t_{RD} + t_{LOCAL} + t_{LAD} + t_{SU}$$

Figure 5 shows the MAX 9000 family I/O cell macroparameters. To calculate the delay for a signal that follows a different path through the device, refer to the timing model shown in Figure 3 to determine which microparameters to add together.

Figure 5. I/O Cell AC Timing Parameters (Part 1 of 3)

Tri-State Enable/Disable Delay

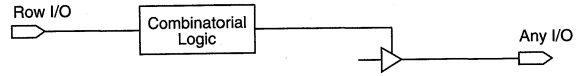
For Global Output Enable:



$t_{XZ} = t_{DIN\_IO} + t_{IOC} + t_{XZ}$

$t_{ZX} = t_{DIN\_IO} + t_{IOC} + t_{ZX1}$

For Row Output Enable:

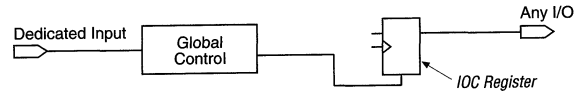


$t_{PXZ} = t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{LAD} + t_{COMB} + t_{FTD} + t_{ROW} + t_{IOC} + t_{XZ}$

$t_{PZX} = t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{LAD} + t_{COMB} + t_{FTD} + t_{ROW} + t_{IOC} + t_{ZX1}$

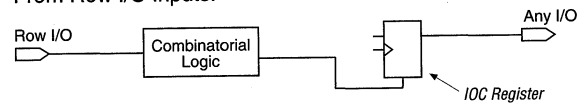
I/O Element Clear Time

From Dedicated Inputs:



$t_{CLR} = t_{DIN\_IO} + t_{IOC} + t_{IOCLR} + t_{OD1}$

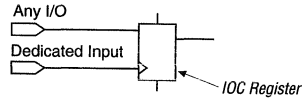
From Row I/O Inputs:



$t_{CLR} = t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{LAD} + t_{COMB} + t_{FTD} + t_{ROW} + t_{IOC} + t_{IOCLR} + t_{OD1}$

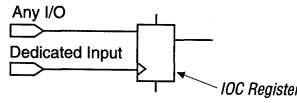
Figure 5. I/O Cell AC Timing Parameters (Part 2 of 3)

Register Setup Time from a Global Clock



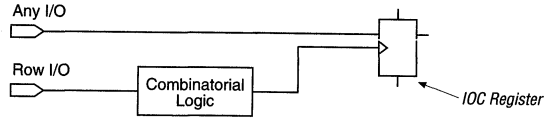
$$t_{FSU} = t_{INREG} - t_{DIN\_IOC} + t_{IOSU}$$

Register Hold Time from a Global Clock



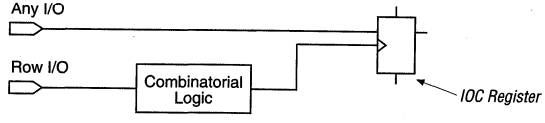
$$t_{FH} = t_{DIN\_IOC} - t_{INREG} + t_{IOH}$$

Asynchronous Setup Time from a Row I/O Clock



$$t_{FASU} = t_{INREG} - (t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{LAD} + t_{COMB} + t_{FTD} + t_{ROW} + t_{IOC}) + t_{IOSU}$$

Asynchronous Hold Time from a Row I/O Clock



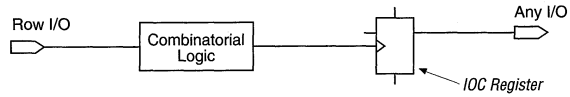
$$t_{FAH} = (t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{LAD} + t_{COMB} + t_{FTD} + t_{ROW} + t_{IOC}) - t_{INREG} + t_{IOH}$$

Figure 5. I/O Cell AC Timing Parameters (Part 3 of 3)

Clock-to-Output Delay from a Global Clock

$t_{FCO} = t_{DIN\_IOC} + t_{IORD} + t_{OD1}$

Asynchronous Clock-to-Output Delay from a Row I/O Clock



$t_{ACO} = t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{LAD} + t_{COMB} + t_{FTD} + t_{ROW} + t_{IOC} + t_{IORD} + t_{OD1}$

Timing Model vs. MAX+PLUS II Timing Analyzer

The MAX+PLUS II Timing Analyzer will always provide the most accurate information on the performance of a design. However, hand calculations based on the timing model also provide a good estimate of the design performance. The MAX+PLUS II Timing Analyzer is more accurate because it takes into account two factors that affect the t_{ROW} and t_{COL} parameters:

- Fan-out for each signal in the delay path
- Distance between signal source and destination

Fan-Out

The more loads a signal has to drive, the longer the delay across t_{ROW} and t_{COL}. For t_{ROW}, this loading is a function of the number of LABs that a signal source has to drive. For t_{COL}, this loading is a function of the number of rows that a signal source has to reach. For example, consider a signal `S1` going to destination `D1` that also goes to macrocells `Y[4..1]`. If `Y[4..1]` are in different LABs, then `S1` has four loads. If, however, they are all in the same LAB, then `S1` has only one load. Therefore, the row interconnect delay from `S1` to `D1` is greater when each macrocell `Y[4..1]` is in a different LAB. The same is true for a column delay. If `Y[4..1]` are in different rows, then the delay will be longer than if they are on the same row.

Distance

The distance between the source and destination also affects the t_{ROW} and t_{COL} parameters. For example, if S1 and D1 are pins on the left and right sides of a device, respectively, then the delay through one LCELL on the same row (i.e., the time required to traverse the length of the device) is the same no matter where the LCELL is placed. If, on the other hand, S1 and D1 are both on the same side, then the delay from S1 to D1 depends on where the LCELL is placed. If the LCELL is on the opposite side from S1 and D1, the delay will be longer than if it is on the same side as S1 and D1. The same is true for the delay incurred by traversing a column.

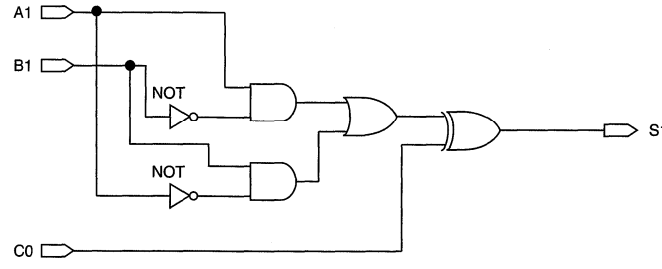
Examples

The following examples show how to use microparameters to estimate the delays for real applications.

Example 1: 7483 TTL Macrofunction

You can analyze the timing delays for circuits that have been subjected to minimization and logic synthesis. The synthesized equations are available in the MAX+PLUS II Report File for the project. These equations are structured so that you can quickly determine the logic configuration of any signal. Figure 6 shows part of a 7483 TTL macrofunction (a 4-bit full adder).

Figure 6. Adder Logic Timing for MAX 9000 Architecture



The Report File for this circuit gives the following equations for S1, the least significant bit of the adder:

```
% S1       = _LC9_B1 %
S1         = LCELL( _EQ002 $ C0);
_EQ002     = !A1 & B1
           # A1 & !B1;
```

S1 is the output of macrocell 9 in LAB B1 (LC9_B1), which contains combinatorial logic. The combinatorial logic LCELL (_EQ002 $ C0) represents the XOR of the intermediate equation _EQ002 and the carry-in C0. In turn, _EQ002 is logically equivalent to the XOR of inputs B1 and A1. Therefore, the timing delay for S1 can be estimated by adding the following parameters:

$t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{LAD} + t_{COMB} + t_{FTD} + t_{ROW} + t_{IODR} + t_{IOCOMB} + t_{OD1}$

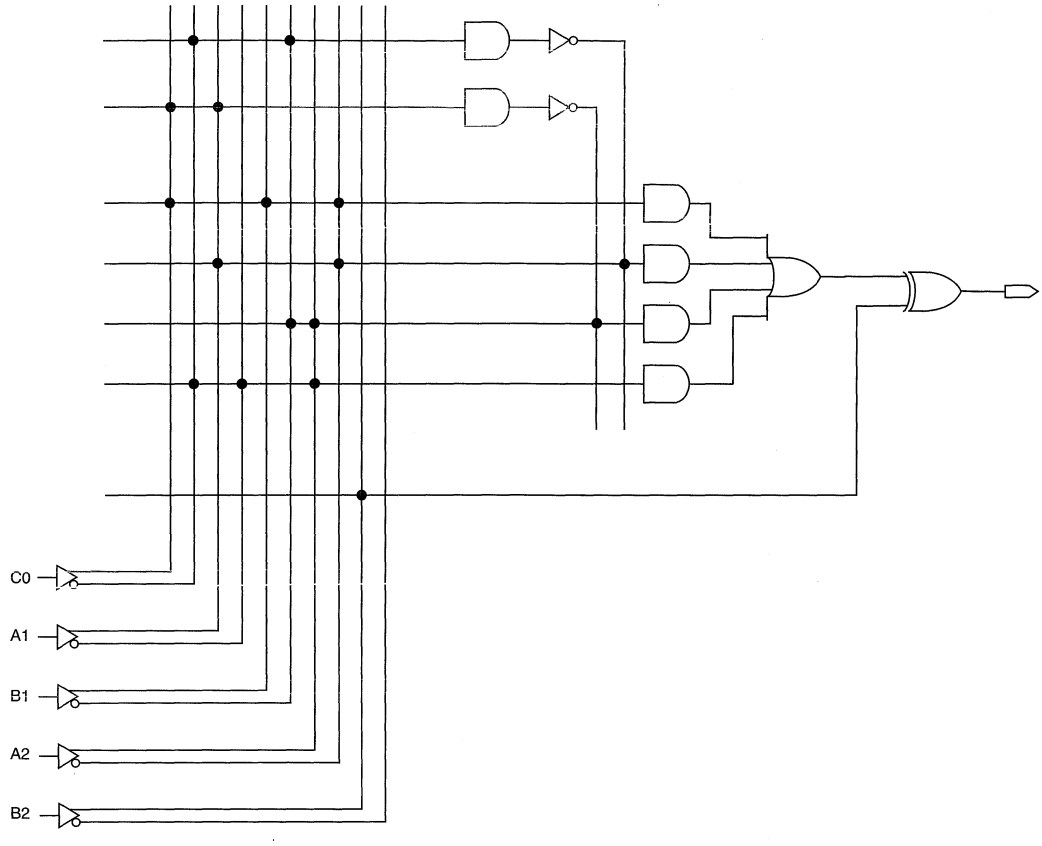
Example 2: S2 Adder Bit

The expander array delay, t_{SEXP}, is added to the delay element for complex logic that requires expanders (represented as _X<*number*> in Report Files). The second bit of the 7483 adder macrofunction, S2, requires shared expanders. The equations are:

```
% S2       = _LC8_B1 %
S2         = LCELL( _EQ003 $ B2);
_EQ003     = !A2 & B1 & C0
           # A1 & !A2 & _X005
           # A2 & !B1 & _X006
           # !A1 & A2 & !C0;
_X005      = EXP(!B1 & !C0);
_X006      = EXP( A1 & C0);
```

Figure 7 shows how you can map the logic structure onto the MAX 9000 architecture with this equation.

Figure 7. Adder Equations Mapped to MAX 9000 Architecture



Therefore, the timing delay for S2 can be estimated by adding the following parameters:

$t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{SEXP} + t_{LOCAL} + t_{LAD} + t_{COMB} + t_{FTD} + t_{ROW} + t_{IODR} + t_{IOCOMB} + t_{OD1}$

Example 3: S2 Adder Bit With Parallel Expanders

The MAX+PLUS II Compiler uses parallel expanders if the Parallel Expanders logic synthesis option is turned on when a project is compiled for MAX 9000 devices. When parallel expanders are used and no sharable expanders are used, the equation for S2 is:

```
% _LC10_B1 borrows parallel expanders from _LC9_B1 %
% S2       = _LC10_B1 %
S2         = LCELL( _EQ003 $ B2);
_EQ003     =  A1 & !A2 & C0
           # A1 & !A2 & B1
           # !A2 & B1 & C0
           # !A1 & A2 & !B1
           # A2 & !B1 & !C0
           # !A1 & A2 & !C0;
```

Therefore, the timing delay for the S2 bit of the 7483 can be estimated by adding the following parameters:

$t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{LAD} + t_{PEXP} + t_{COMB} + t_{FTD} + t_{ROW} + t_{IODR} + t_{IOCOMB} + t_{OD1}$

Example 4: S1 Adder Bit in Low-Power Mode

If a macrocell in a MAX 9000 device is set for low-power mode, you must add the low-power adder delay to the total delay through that macrocell. The estimated S1 delay becomes:

$t_{INCOMB} + t_{ROW} + t_{LOCAL} + t_{LPA} + t_{LAD} + t_{COMB} + t_{FTD} + t_{ROW} + t_{IODR} + t_{IOCOMB} + t_{OD1}$

Conclusion

The MAX 9000 architecture has predictable internal timing delays that can be estimated based on signal synthesis and placement. Using the MAX 9000 timing model shown in Figure 3 and the timing parameters in the *MAX 9000 Programmable Logic Device Data Sheet* in this data book, you can estimate the performance of a design before compilation. However, the MAX+PLUS II Timing Analyzer provides the most accurate information. These methods enable you to accurately predict your design's in-system timing performance.

Notes:

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Introduction

Ideally, a programmable logic design environment satisfies a large variety of design requirements: it should support devices with different architectures, run on multiple platforms, provide an easy-to-use interface, and offer a broad range of features. Moreover, a design environment should give designers the freedom to use the design entry methods and the tools of their choice. The Altera MAX+PLUS II development system is a fully integrated programmable logic design environment that meets all of these requirements.

The MAX+PLUS II design environment offers unmatched flexibility and performance. The rich graphical user interface is complemented by complete and instantly accessible on-line documentation, which makes learning and using MAX+PLUS II quick and easy.

- *Architecture-Independence* The MAX+PLUS II Compiler, the heart of the MAX+PLUS II system, supports Altera's FLEX 10K, MAX 9000, FLEX 8000, MAX 7000, FLASHlogic, MAX 5000, and Classic programmable logic device families, offering the industry's only truly architecture-independent programmable logic design environment. (Support for FLASHlogic devices is planned for the second half of 1995.) The Compiler also provides powerful logic synthesis and minimization to efficiently fit designs with minimal user effort.

- *Multiple Platforms* MAX+PLUS II runs under Microsoft Windows or Windows NT on 486- or Pentium-based PCs, and under X Windows on Sun SPARCstation, HP 9000 Series 700, and IBM RISC System/6000 workstations.

- *Full Integration* Together, MAX+PLUS II design entry, processing, and verification features offer the most fully integrated suite of programmable logic development tools available, allowing faster debugging and shorter development cycles.

- *Modular Tools* Designers can customize their development environment by choosing from a variety of design entry, compilation, verification, and device programming options, all of which are described in this data sheet. Additional features can be added as needed, preserving the initial tools investment. Since MAX+PLUS II

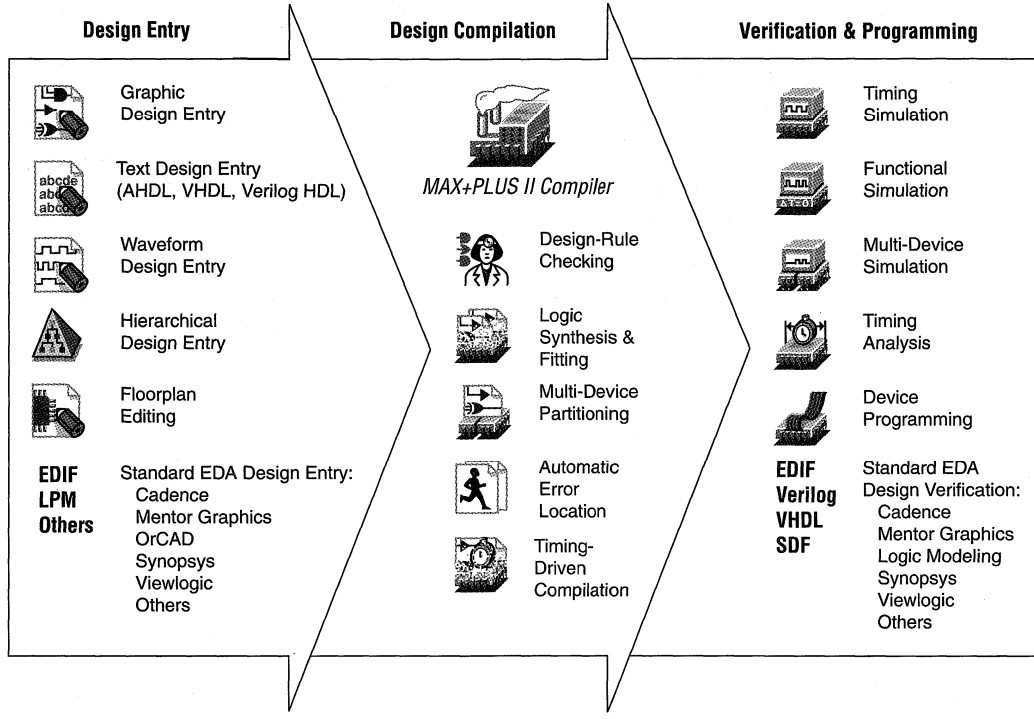
supports multiple device families, designers can add support for new architectures without having to learn new tools.

- *Hardware Description Languages (HDLs)* MAX+PLUS II supports a variety of HDL design entry options, including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL).

- *Open Interfaces* Altera works closely with EDA manufacturers to link MAX+PLUS II with other industry-standard design entry, synthesis, and verification tools. The interfaces to EDA tools comply with EDIF 2 0 0 and 3 0 0, library of parameterized modules (LPM), Verilog HDL, VHDL, and other standards. They allow users to create a logic design with Altera or standard EDA design entry tools, compile the design for an Altera device with the MAX+PLUS II Compiler, and perform device- or board-level simulation with Altera or other EDA verification tools. MAX+PLUS II currently supports interfaces to tools from Synopsys, Viewlogic, Mentor Graphics, Cadence, Exemplar, Data I/O, Intergraph, Minc, OrCAD, and others.

The MAX+PLUS II design process, shown in Figure 1, consists of four phases: design entry, design compilation, design verification, and device programming.

Figure 1. MAX+PLUS II Design Environment



Design Entry

MAX+PLUS II can integrate design files—generated with MAX+PLUS II design entry tools or with a variety of other industry-standard EDA design entry tools—into a single design hierarchy. The extensive integration between MAX+PLUS II applications allows information to flow freely to and from each application. For example, errors identified during compilation, simulation, and timing analysis can be automatically located and highlighted in the original design file or in the Floorplan Editor. If a design (called a "project" in MAX+PLUS II) consists of two or more hierarchical levels, the user can go from one design file directly to any other design file in the hierarchy, regardless of whether it is graphic-, text-, or waveform-based.

Industry-Standard Library Support

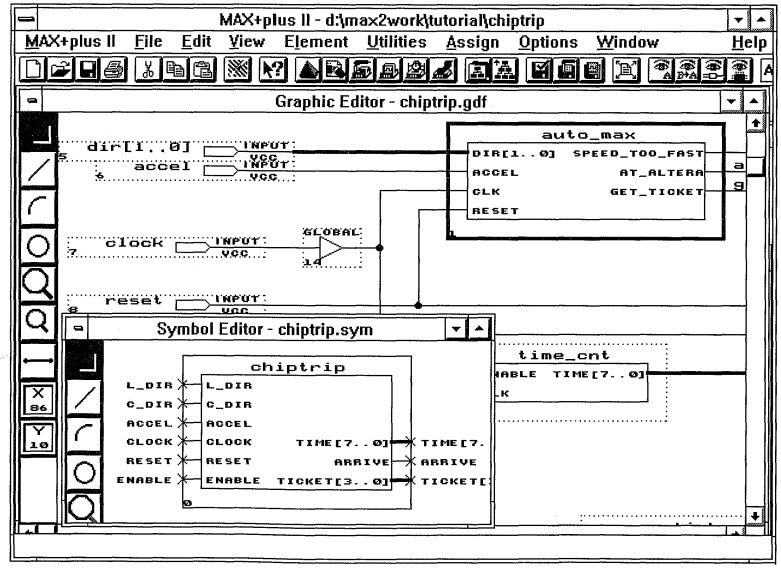
Users can describe their designs with the industry-standard library of parameterized modules (LPM). The LPM standard offers scalable macrofunctions, such as counters, adders, and multiplexers, and preserves high-level design information for optimal implementation. The MAX+PLUS II Compiler automatically generates optimized, architecture-specific implementations of the LPM privitives. LPM primitives can be enteredwith industry-standard design entry tools or in schematic text designs created with MAX+PLUS II.

Schematic Capture & Symbol Editing

The MAX+PLUS II Graphic Editor, shown in Figure 2, makes schematic design entry fast and easy. Drag-and-drop editing allows the user to quickly move one or more objects or an entire area. During a move, a net can be preserved with the rubberbanding feature. The designer can also make a design more compact by connecting primitives with buses to create arrays of symbols. MAX+PLUS II provides symbols for over 300 74-series, LPM, and custom functions.

MAX+PLUS II can create a symbol for any design file automatically. With the Symbol Editor (also shown in Figure 2), the designer can modify a symbol to customize its appearance, or create an entirely new symbol.

Figure 2. MAX+PLUS II Graphic & Symbol Editor



Hardware Description Language (HDL) Entry

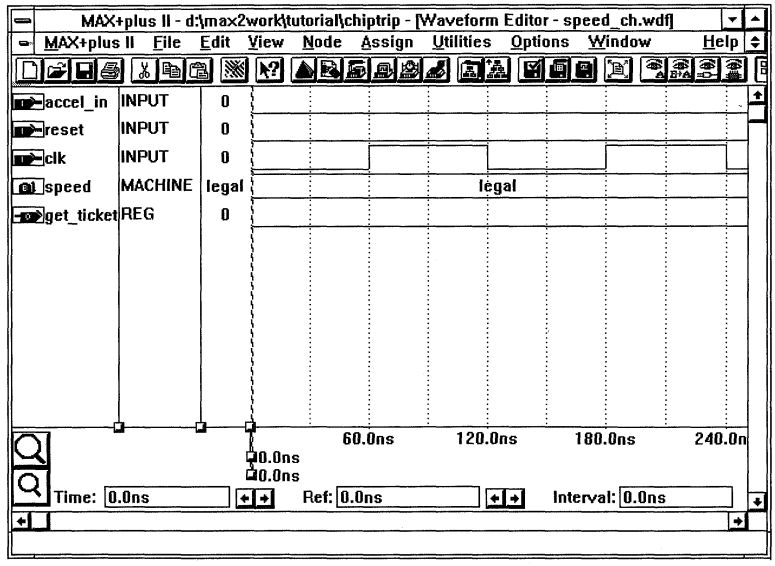
The MAX+PLUS II software contains an integrated Text Editor that is ideal for entering and editing hardware description language (HDL) design files written in VHDL, Verilog HDL, or the Altera Hardware Description Language (AHDL). The MAX+PLUS II Compiler can synthesize logic from any of these languages and map it to any of Altera's device families.

Each of these HDLs can implement state machines, truth tables, conditional logic and Boolean equations; AHDL also supports LPM design entry. Arithmetic operations—including addition, subtraction, and equality and magnitude comparison—are also supported. Together, these features make it easy to implement complex projects in a concise, high-level description.

Waveform Design Entry

The MAX+PLUS II Waveform Editor (shown in Figure 3) is used to create and edit waveform design files, as well as input vectors for simulation and functional testing. The Waveform Editor also functions as a logic analyzer that allows the designer to view simulation results.

Figure 3. MAX+PLUS II Waveform Editor



13 Development Tools

Waveform design entry is best suited for sequential and repeating functions. The Compiler's advanced waveform synthesis algorithms automatically generate logic from user-defined input and output waveforms that represent registered, combinatorial, and state machine logic. The Compiler automatically assigns state bits and state variables for state machines.

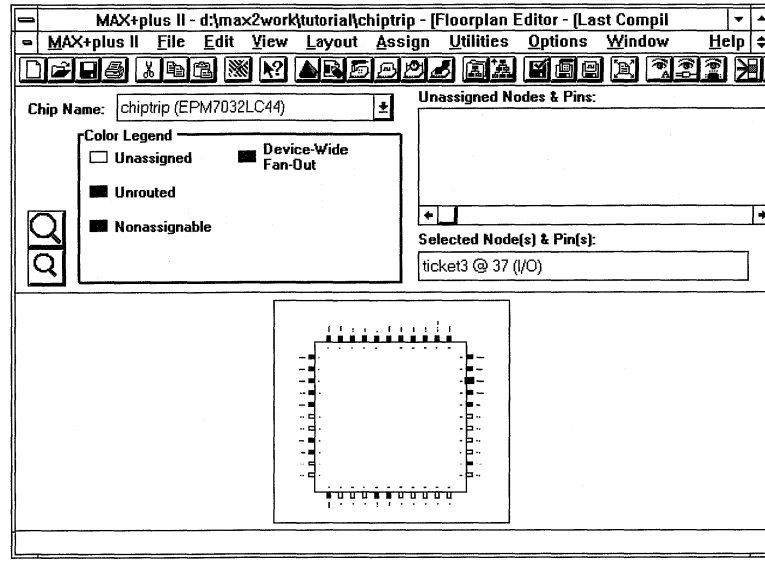
Waveform Editor features allow the designer to copy, cut, paste, repeat, and stretch waveforms; to create design files with internal nodes, flipflops, and state machines; to combine waveforms into groups that display binary, octal, decimal, or hexadecimal values; and to compare two sets of simulation results by superimposing one set of waveforms on another.

Floorplan Editing

The MAX+PLUS II Floorplan Editor (shown in Figure 4) simplifies the process of assigning logic to device pins and logic cells. A graphical image of each device that is used in a project allows easy logic placement. Both high-level and detailed device views are available. The designer can assign pins and logic cells before compiling a design, and can view and modify the results after compilation.

Floorplan Editor features allow the designer to view all assigned and unassigned logic in a device. The Floorplan Editor provides a color-coded view of all logic resources in the device, as well as user assignments, fan-in and fan-out information, and architecture-specific features. Any node or pin can be dragged to a new location. Logic can be assigned to specific pins and logic cells, or to more general regions within a device. Alternatively, these assignments may be made in a text-based Assignment & Configuration File (**.acf**), that can be edited in the MAX+PLUS II Text Editor.

Figure 4. MAX+PLUS II Floorplan Editor



Industry-Standard EDA Design Entry

The MAX+PLUS II Compiler can interface with industry-standard EDA tools that generate EDIF 2 0 0 and 3 0 0 netlist files. The Compiler uses Library Mapping Files (**.lmf**) to map proprietary symbol and pin names from other EDA tools to MAX+PLUS II macrofunction and basic gate library elements. Altera provides LMFs for over 100 74-series and custom macrofunctions for files generated by tools from companies such as Cadence, Mentor Graphics, Minc, OrCAD, and Viewlogic. VHDL and Verilog HDL design support is also available through Cadence, Exemplar, Intergraph, Mentor Graphics, Racal-Redac, Synopsys, and Viewlogic.

For more information on other industry-standard design entry tools, see *EDA Software Support* in this data book.

MAX+PLUS II can also read OrCAD Schematic Files (**.sch**) or Xilinx Netlist Files (**.xnf**) for compilation or integration into designs for Altera devices.

Hierarchical Design Entry

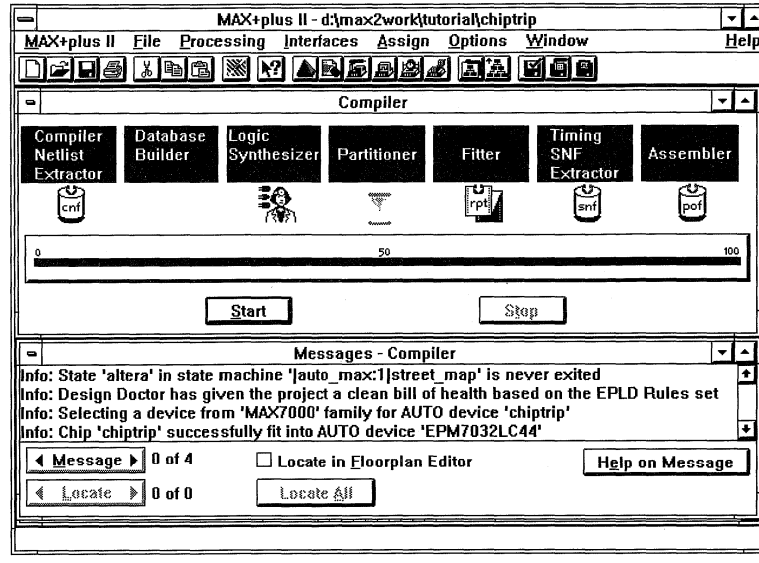
Hierarchical designs can consist of design files created with several different methods, including schematic capture, HDL design entry, waveform design entry, and industry-standard netlist files. MAX+PLUS II supports multiple levels of hierarchy in a single design. This flexibility allows designers to use the design entry method best suited to each portion of the design. The MAX+PLUS II Hierarchy Display, which displays the hierarchical structure of a project, allows designers to easily traverse the hierarchy, automatically opening the appropriate editor for each design file.

Design Compilation

When MAX+PLUS II processes a design, the Compiler reads in design files and produces output files for programming, simulation, and timing analysis. The Message Processor can automatically locate errors deleted during compilation. MAX+PLUS II supports FLEX 10K, MAX 9000, FLEX 8000, MAX 7000, MAX 5000, and Classic devices. Compilation support for FLASHlogic and for EP224, EP310I, EP312, EP324, and EP22V10 devices is provided by Altera's PLDshell Plus software and industry-standard compilers. MAX+PLUS II support for FLASHlogic devices is planned for late 1995.

The MAX+PLUS II Message Processor communicates with all MAX+PLUS II applications, reporting error, information, and warning messages for problems such as connection and syntax errors. Designers can use the Message Processor to automatically open the design file that contains the source of an error and highlight its location. In addition, the Message Processor can locate errors in the floorplan for the current project in the Floorplan Editor. See Figure 5.

Figure 5. MAX+PLUS II Compiler & Message Processor



Logic Synthesis & Fitting

The MAX+PLUS II Compiler's Logic Synthesizer module supports both synthesized and what-you-see-is-what-you-get (WYSIWYG) design implementation. It selects appropriate logic reduction algorithms to minimize and remove redundant logic, ensuring that the device logic resources are used as efficiently as possible for the specified device architecture. It also removes unused logic from the project.

Logic synthesis options help the designer guide the outcome of logic synthesis. Altera provides "ready-made" synthesis styles, which specify the settings for multiple logic synthesis options. The designer can choose a default style to set default synthesis options, create custom styles, and specify individual synthesis options on selected logic functions. Synthesis options can be tailored for a specific device family to take advantage of its architecture. A number of advanced logic options further expand the designer's ability to control logic synthesis.

The Compiler's Fitter module applies heuristic rules to select the best possible implementation for the synthesized project in one or more devices. This automatic fitting relieves the designer of tedious place-and-route tasks. The Fitter generates a Report File (**.rpt**) that shows project implementation as well as any unused resources in the device(s). Fitting results can also be displayed in the MAX+PLUS II Floorplan Editor.

Timing-Driven Compilation

The Compiler can implement user-specified timing requirements for propagation delays (t_{PD}), Clock-to-output delays (t_{CO}), setup times (t_{SU}), and Clock frequency (f_{MAX}). Designers can specify timing requirements on selected logic functions and for a project as a whole. The Fitter's Report File provides detailed information on how the timing requirements have been implemented in the project.

Design-Rule Checking

The MAX+PLUS II Compiler includes the Design Doctor, a design-rule checker. The Design Doctor checks each design file for logic that may cause system-level reliability problems that are usually discovered only after a design has entered production. The user can choose one of three predefined sets of design rules with increasingly thorough design-rule checking, or create a custom set of rules.

Design rules are based on reliability guidelines that cover logic containing features such as asynchronous inputs, ripple Clocks, multi-level logic on Clocks, Preset and Clear configurations, and race conditions. Rule violations are explained to help the designer determine which edits are needed in the design files.

Multi-Device Partitioning

If a project is too large for a single device, the Compiler's Partitioner module divides it into multiple devices from the same device family. It attempts to split the project into the smallest possible number of devices while minimizing the number of pins used for inter-device communication. The Fitter automatically fits the logic into the specified devices.

Partitioning can be totally automatic, partially user-controlled, or fully user-controlled. If a project is too large to fit into a specified device, the designer can specify the type and number of additional devices.

Industry-Standard Output Formats

The MAX+PLUS II Compiler can create netlist files for use in a variety of simulation environments. These netlist files contain post-synthesis functional and timing information that can be used with other standard design verification tools for device- or board-level simulation.

The following interfaces are available:

Interface:	MAX+PLUS II Support:
EDIF	Creates EDIF 2 0 0 and 3 0 0 netlist files that provide functionality and timing for third-party simulators.
Verilog	Creates Verilog netlist files that can be used with Verilog-XL simulators.
VHDL	Creates VHDL netlist files that can be used with VHDL simulators.

For each interface, the Compiler can optionally generate a Standard Delay Format File (**.sdf**) that includes timing information for simulators that require timing and functional information in separate files.

Programming File Generation

The Assembler module creates one or more Programmer Object Files (**.pof**), SRAM Object Files (**.sof**), and/or JEDEC Files (**.jed**) for a compiled project. The MAX+PLUS II Programmer uses these files and standard Altera hardware to program devices. Device programming is also available with other industry-standard programming equipment. In addition, MAX+PLUS II can generate Hexadecimal (Intel-format) Files (**.hex**), Tabular Text Files (**.ttf**), and Serial Bitstream Files (**.sbf**) for configuring FLEX 8000 devices by other means.

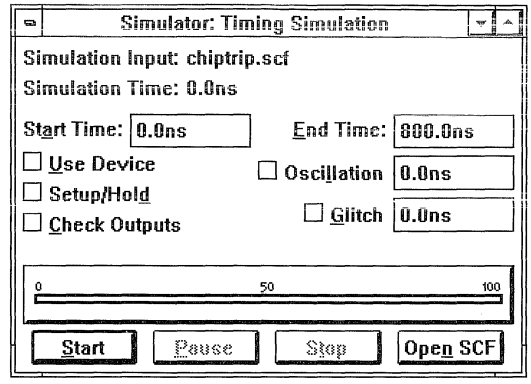
Design Verification

MAX+PLUS II offers design verification processes including design simulation and timing analysis that test the logical operation and internal timing of a design. Design verification tools for Altera devices are also available from a variety of EDA vendors.

Simulation

The MAX+PLUS II Simulator provides flexibility and control for modeling single- or multi-device projects. The Simulator uses a binary simulation netlist files that is generated during compilation to perform functional, timing, or combined linked multi-device simulation for a project. Figure 6 shows the MAX+PLUS II Simulator.

Figure 6. MAX+PLUS II Simulator



The designer either defines input stimuli with a straightforward vector input language or draws waveforms directly with the MAX+PLUS II Waveform Editor. Simulation results can be viewed in the Waveform Editor or Text Editor and printed as waveform or text files.

The designer specifies commands either interactively or in a text-based command file to perform a variety of tasks, such as monitoring the project for glitches, oscillation, and register setup and hold time violations; halting the simulation when user-defined conditions are met; forcing flipflops high or low; and performing functional testing. If a setup or hold time, minimum pulse width, or oscillation period is violated, the Message Processor reports the problem. The designer can then use the Message Processor to locate the time at which the problem occurred in the Waveform Editor and to locate the error in the original design file.

For easy comparison, the designer can superimpose the results of two simulations in the Waveform Editor.

Functional Simulation

The MAX+PLUS II Simulator supports functional simulation to test the logical operation of a project before it is synthesized, thereby allowing the designer to quickly identify and correct logical errors. The MAX+PLUS II Waveform Editor displays the results of functional simulation and provides easy access to all nodes in the project, including combinatorial functions.

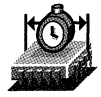
Timing Simulation

In a timing simulation, the MAX+PLUS II Simulator tests the project after it has been fully synthesized and optimized. Timing simulation is performed at 0.1-ns resolution.

Multi-Device Simulation

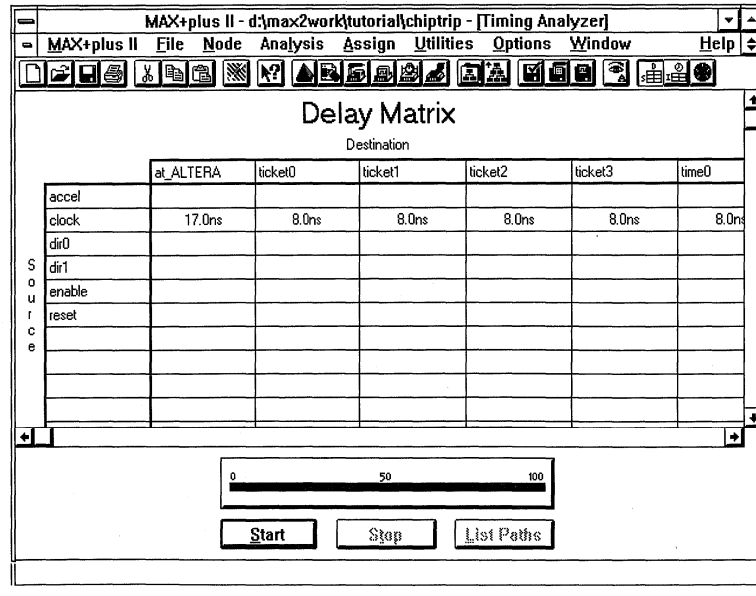
MAX+PLUS II can combine the timing and/or functional information from multiple Altera devices, allowing the designer to simulate several devices operating together. Devices from different Altera device families can be used in the same project.

Timing Analysis



The MAX+PLUS II Timing Analyzer can calculate a matrix of point-to-point device delays, determine setup and hold time requirements at device pins, and calculate maximum Clock frequency. MAX+PLUS II design entry tools are integrated with the Timing Analyzer, allowing the designer to simply tag start and end points in the design files or the Floorplan Editor to determine the shortest and longest propagation delays. In addition, the Message Processor can locate and display critical paths identified by the Timing Analyzer in the source design files or in the Floorplan Editor. See Figure 7.

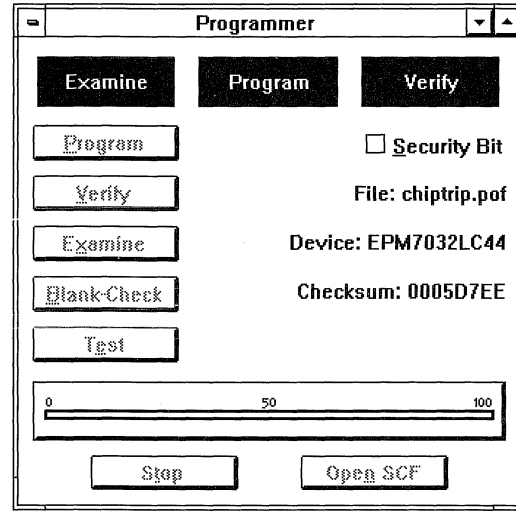
Figure 7. MAX+PLUS II Timing Analyzer



Device Programming

The MAX+PLUS II Programmer, shown in Figure 8, uses programming files generated by the Compiler to program Altera devices. It allows the designer to program, verify, examine, blank-check, and functionally test devices. The programming hardware includes an add-on Logic Programmer card (for PC-AT or compatible computers) that drives the Altera Master Programming Unit (MPU). The MPU performs continuity checking to ensure adequate electrical contact between the programming adapter and the device. With the appropriate programming adapter, the MPU also supports functional testing, so that vectors created for simulation can be applied to a programmed device to verify its functionality.

Figure 8. MAX+PLUS II Programmer



Altera also provides the FLEX Download Cable and the BitBlaster for device programming and configuration. The FLEX Download Cable can connect any Configuration EPROM programming adapter, which is installed on the MPU, to a single target FLEX 10K, FLEX 8000, or FLEX 8000M device in a prototype system. The BitBlaster serial download cable is a hardware interface to a standard RS-232 port that provides configuration data to FLEX 10K and FLEX 8000 devices and programming data to MAX 9000 and MAX 7000S devices on system boards. The BitBlaster allows both PC and workstation users to configure a FLEX 10K or FLEX 8000 device, or program a MAX 9000 or MAX 7000S device independently of the MAX+PLUS II Programmer or any other programming hardware.

For more information on the BitBlaster, refer to the *BitBlaster Serial Download Cable* data sheet in this data book.

All hardware and software necessary for programming and verifying devices is available from Altera (see *Altera Programming Hardware* in this data book). Programming support is also available from many other programming hardware manufacturers (see *Programming Hardware Manufacturers* in this data book).

On-Line Help

On-line help provides access to all information on MAX+PLUS II. It includes complete, up-to-date documentation on all MAX+PLUS II applications, causes and suggested actions for messages, references to related Altera documentation, text file formats (e.g., AHDL), and information on Altera devices and adapters.

On-line help is only a keystroke or a mouse click away. The F1 key provides instant access to information on a dialog box, highlighted menu command, or pop-up message. Typing Shift+F1 or choosing the context-sensitive help button on the toolbar turns the mouse pointer into a question mark pointer that allows the designer to click on any item on the screen—including primitives, macrofunctions, and AHDL keywords—for context-sensitive help on that item.

Software Maintenance Agreement

To guarantee timely upgrades to software and documentation, Altera offers a Software Maintenance Agreement that entitles the customer to software updates, discounts on selected software products, Applications Engineering support, and access to Altera's bulletin board service (BBS).

Recommended System Configurations

To run MAX+PLUS II with optimum results, Altera recommends the following system configurations:

PC System Configuration

- Pentium-based PC-AT or compatible computer
- Minimum of 32 Mbytes of available memory, i.e., combined RAM and virtual memory, consisting of no less than 16 Mbytes of RAM. For large designs, 64 Mbytes of available memory, including 32 Mbytes of RAM, is required.
- DOS version 5.0 or higher
- Microsoft Windows version 3.1
- Microsoft Windows-compatible graphics card and monitor
- CD-ROM drive or 1.44-Mbyte, 3 ½-inch floppy disk drive
- 2- or 3-button mouse compatible with Microsoft Windows 3.1
- Full-length 8-bit ISA slot for Logic Programmer card
- Parallel port

Sun SPARCstation System Configuration

- Sun SPARCstation with color or monochrome monitor
- 32 Mbytes of RAM
- Sun OS 4.1.2 (or Solaris 1.0) or higher
- Sun OpenWindows 3.0 (or Solaris 1.0) or higher
- ISO 9660-compatible CD-ROM drive

HP 9000 Series 700 Workstation System Configuration

- HP 9000 Series 700 workstation with color or monochrome monitor
- 32 Mbytes of RAM
- HP-UX version 9.03 or higher
- HP-VUE
- ISO 9660-compatible CD-ROM drive

IBM RISC System/6000 Workstation System Configuration

- IBM RISC System/6000 workstation with color or monochrome monitor
- 32 Mbytes of RAM
- AIX version 3.2.5 or higher
- AIX Windows version 1.2.5 or higher
- ISO 9660-compatible CD-ROM drive

Package Software Options

Altera offers a variety of tool configurations and add-on migration products for PC- and workstation-based versions of MAX+PLUS II. In addition, any customer who purchases a PC-based MAX+PLUS II software product receives a site license to install an unlimited number of copies of the PLS-ES development software.

For up-to-date information on MAX+PLUS II software packages and development systems, contact Altera Marketing at (408) 894-7104.

For detailed information on software package options, refer to the *MAX+PLUS II Selection Guide* in this data book.

MAX+PLUS II Selection Guide

March 1995, ver. 2

Development Systems & Migration Products

Altera offers a variety of system configurations and migration products for MAX+PLUS II. MAX+PLUS II supports Altera's FLEX 10K, FLEX 8000, MAX 9000, MAX 7000, FLASHlogic, MAX 5000, and Classic device families—including EPROM-, EEPROM-, FLASH-, and SRAM-based devices—for true architecture-independent design.

The first decision to make when selecting a MAX+PLUS II system is to determine the device support and features needed. Once designers purchase a particular MAX+PLUS II configuration, they can add features and device support to it at any time. Table 4 shows the available features and device support provided by each MAX+PLUS II configuration. The Ordering Codes column provides the necessary codes for ordering MAX+PLUS II systems and add-on products.

For up-to-date information on available features and device support, contact Altera Marketing at (408) 894-7104.

For a detailed description of MAX+PLUS II development software, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* in this data book.

Table 1. Altera Development Systems, Software & Device Support

Ordering Codes	Device Support								Design Entry							Compilation						Design Verification					
	FLEX 10K	FLEX 8000	FLEX 8000M	MAX 9000	MAX 7000	FLASHlogic, *Note (1)*	MAX 5000	Classic+Plus, *Note (2)*	Schematic Capture	AHDL	VHDL	Verilog HDL	Waveform	Floorplan Editor	EDA Interfaces	Hierarchical Design	Timing Driven Compilation	Automatic Error Location	Design-Rule Checking	Multi-Device Partitioning	Logic Synthesis & Fitting	Multi-Device Simulation	Functional & Timing Sim.	Timing Analysis	Waveform Editing	On-Line Help	PLS-ES Site License
Base Systems (PC Platform)																											
PLS-ES						✓		✓	✓	✓				✓	✓	✓		✓			✓			✓		✓	✓
PLS-ADV					✓	✓	✓	✓	✓	✓				✓	✓	✓		✓			✓			✓		✓	✓
PLS-FLEX8		✓				✓	✓	✓	✓	✓				✓	✓	✓		✓			✓			✓		✓	✓
PLS-MAGNUM	✓	✓		✓	✓	✓	✓	✓	✓	✓			✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Migration Products (PC Platform)																											
PLSM-5K							✓														✓						
PLSM-7K					✓																✓						
PLSM-8K		✓																			✓						
PLSM-8KM			✓																		✓						
PLSM-9K				✓																	✓						
PLSM-10K	✓																				✓						
PLSM-SIM																							✓		✓		
PLSM-ADE													✓						✓	✓		✓	✓		✓		
PLSM-VHDL											✓																
PLSM-VLOG												✓															
PLSM-TDC																	✓										
Base Systems (Workstation Platform)																											
PLS-WS/HP	✓	✓			✓	✓	✓	✓		✓				✓	✓	✓	✓	✓	✓	✓	✓					✓	
PLS-WS/SN	✓	✓			✓	✓	✓	✓		✓				✓	✓	✓	✓	✓	✓	✓	✓					✓	
PLS-WS/IBMRS	✓	✓			✓	✓	✓	✓		✓				✓	✓	✓	✓	✓	✓	✓	✓					✓	
Migration Products (Workstation Platform)																											
PLSM-8KMWS			✓	✓																	✓						
PLSM- TA																								✓			

Notes to table:
(1) Full support for FLASHlogic devices is planned for the second half of 1995.
(2) Classic+Plus includes device support for the Classic family, as well as the EPM5032, EPM5032A, EPM7032, EPM7032V, EPM7064, EPM7096, EPF8282, and EPF8282V devices.

MAX+PLUS II System Options

Tables 2 through 5 describe the various MAX+PLUS II products listed in Table 1, as well as software maintenance products that provide registered users with regular upgrades for software and documentation.

Table 2. PC-Based System Configurations

System Configuration	Description
PLS-ES	Contains logic synthesis and fitting support for the FLASHlogic and Classic families, as well as the EPM5032, EPM5032A, EPM7032, EPM7032V, EPM7064, EPM7096, EPF8282, and EPF8282V devices. (Support for the FLASHlogic family is planned for the second half of 1995.) PLS-ES also includes schematic capture, text design entry with AHDL, interfaces through EDIF 2 0 0 and 3 0 0 input and output files, the LPM netlist reader, hierarchical design management, on-line help, the PLS-ES Site License, automatic error location, timing analysis, and floorplan editing.
PLS-ADV	Contains logic synthesis and fitting support for the MAX 7000, MAX 5000, FLASHlogic, and Classic families, and the EPF8282 and EPF8282V devices. (Support for the FLASHlogic family is planned for the second half of 1995.) PLS-ADV also includes schematic capture, text design entry with AHDL, interfaces through EDIF 2 0 0 and 3 0 0 input and output files, the LPM netlist reader, hierarchical design management, on-line help, the PLS-ES Site License, automatic error location, timing analysis, and floorplan editing.
PLS-FLEX8	Contains logic synthesis and fitting support for the FLEX 8000, MAX 5000, FLASHlogic, and Classic families, and the EPM7032, EPM7032V, EPM7064, and EPM7096 devices. (Support for the FLASHlogic family is planned for the second half of 1995.) PLS-FLEX8 also includes schematic capture, text design entry with AHDL, interfaces through EDIF 2 0 0 and 3 0 0 input and output files, the LPM netlist reader, hierarchical design management, on-line help, the PLS-ES Site License, automatic error location, timing analysis, and floorplan editing.
PLS-MAGNUM	Contains logic synthesis and fitting support for the FLEX 10K, FLEX 8000, MAX 9000, MAX 7000, FLASHlogic, MAX 5000, and Classic families. (Support for the FLEX 10K and FLASHlogic families is planned for the second half of 1995.) PLS-MAGNUM also includes schematic capture, text design entry with AHDL, waveform design entry, interfaces through EDIF 2 0 0 and 3 0 0 input and output files, the LPM netlist reader, timing-driven compilation, design-rule checking, multi-device partitioning, logic synthesis and fitting, multi-device simulation, functional simulation, timing simulation, waveform editing, hierarchical design management, on-line help, the PLS-ES Site License, automatic error location, timing-driven compilation, design-rule checking, multi-device partitioning, timing and functional simulation, timing analysis, and floorplan editing.

Table 3. PC-Based Migration Products

Product	Description
PLSM-5K	Adds compilation support for the MAX 5000 family to PLS-ES.
PLSM-7K	Adds compilation support for the MAX 7000 family to PLS-ES and PLS-FLEX8.
PLSM-8K	Adds compilation support for the FLEX 8000 family to PLS-ES and PLS-ADV.
PLSM-8KM	Adds compilation support for the FLEX 8000M family to PLS-ES, PLS-ADV, PLS-FLEX8, PLS-HPS, PLS-Quartet, and PLS-MAGNUM. FLEX 8000 and multi-device partitioning support is required for PLSM-8KM.
PLSM-9K	Adds compilation support for the FLEX 10K and MAX 9000 families to PLS-ES, PLS-ADV, PLS-FLEX8, and PLS-HPS.
PLSM-10K	Adds compilation support for the FLEX 10K and MAX 9000 families to PLS-ES, PLS-ADV, PLS-FLEX8, and PLS-HPS.
PLSM-SIM	Adds waveform editing and functional and timing simulation support to PLS-ES, PLS-ADV, and PLS-FLEX8.
PLSM-ADE	Adds waveform design entry and editing; design-rule checking; functional, timing, and multi-device simulation; and multi-device partitioning to PLS-ES, PLS-ADV, and PLS-FLEX8.
PLSM-VHDL	Adds VHDL design entry to any PC-based MAX+PLUS II development system.
PLSM-VLOG	Adds Verilog HDL design entry to any PC-based MAX+PLUS II development system.
PLSM-TDC	Adds the ability to specify timing constraints to any portion of a design during design entry to PLS-ES, PLS-ADV, and PLS-FLEX8.
PLAESW-xxx	Software maintenance products for PC-based MAX+PLUS II. Software Maintenance Agreements ensure that registered users receive all upgrades to software and documentation when development software is upgraded or modified to provide new features and/or to support new devices. To order a Software Maintenance Agreement, use the PLAESW- prefix followed by the appropriate product extension (e.g., PLAESW-MAGNUM).

Table 4. Workstation-Based System Configurations

System Configuration	Description
PLS-WS/SN, PLS-WS/HP, and PLS-WS/IBMRS	These system configurations contain logic synthesis and fitting support for the FLEX 10K, FLEX 8000, MAX 9000, MAX 7000, FLASHlogic, MAX 5000, and Classic families. (Support for the FLEX 10K and FLASHlogic families is planned for the second half of 1995.) Interfaces are provided to Mentor Graphics, Cadence, Synopsys, Viewlogic, Intergraph, and other EDA environments through EDIF 2 0 0 and 3 0 0 input and output files. Workstation support also includes text design entry with AHDL, hierarchal design, timing driven compilation, automatic error location, design-rule checking, multi-device partitioning, logic synthesis, and logic fitting. PLS-WS/SN supports Sun SPARCstations. PLS-WS/HP supports HP 9000 Series 700 workstations. PLS-WS/IBMRS supports IBM RISC System/6000 workstations.

Table 5. Workstation-Based Migration Products

Product	Description
PLSM-8KMWS	Adds compilation support for the FLEX 8000M family to PLS-WS/SN.
PLSM-TA	Adds timing analysis capabilities to MAX+PLUS II for workstations. The MAX+PLUS II Timing Analyzer can calculate a matrix of point-to-point device delays, determine setup and hold time requirements at device pins, and calculate the maximum Clock frequency.
PLSM-VLOGWS	Adds Verilog HDL design entry to the PLS-WS/SN or PLS-WS/HP.
PLSM-VHDLWS	Adds VHDL design entry to PLS-WS/SN or PLS-WS/HP.
PLSM-WS/SN, PLSM-WS/HP, and PLSM-WS/IBMRS	Provides additional floating node licenses for workstation-based MAX+PLUS II system.
PLAESW-WS	Software maintenance product for workstation-based MAX+PLUS II system. Software Maintenance Agreements ensure that registered users receive all upgrades to software and documentation when development software is upgraded or modified to provide new features and/or support for new devices.

Notes:

BitBlaster Serial Download Cable

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Features

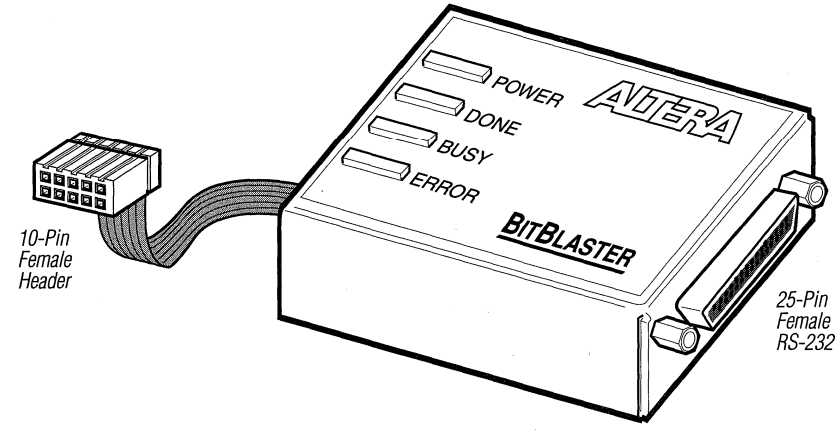
- Programs MAX 9000 and MAX 7000S devices and configures FLEX 10K and FLEX 8000 devices in-circuit via a standard RS-232 serial port
- Downloads configuration and programming data from MAX+PLUS II development software
- Downloads configuration data from a system prompt on both workstations and PCs
- Supports data transfer baud rates from 9,600 baud to 230,400 baud

Functional Description

The BitBlaster serial download cable (ordering code: PL-BITBLASTER) is a hardware interface to a standard RS-232 port (called a "COM port" on a PC). This cable provides configuration data to FLEX 10K and FLEX 8000 devices and programming data to MAX 9000 and MAX 7000S devices. See Figure 13.

13 Development Tools

Figure 1. BitBlaster



The 25-pin female port on the BitBlaster is connected to an RS-232 port with a standard serial cable. The 10-pin female plug on the BitBlaster is connected to a FLEX 10K, FLEX 8000, MAX 9000, or MAX 7000S device on a circuit board via a 10-pin male header. Status lights indicate the state of the device configuration or programming. See Table 9.

Table 1. BitBlaster Status Lights

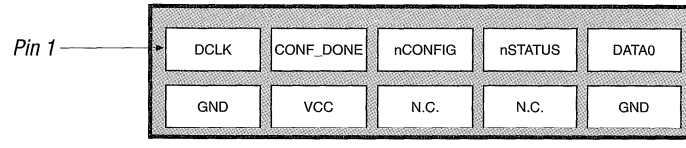
Status Light	Description
POWER	Indicates a connection to the target system's power supply.
DONE	Indicates that device configuration or programming is complete.
BUSY	Indicates that the device is being configured or programmed.
ERROR	Indicates that an error occurred during configuration or programming.

☞ The board must supply V_{CC} and GND to the BitBlaster.

Figure 14 shows the 10-pin female plug connections.

Figure 2. BitBlaster 10-Pin Female Plug Connections

FLEX 8000 Devices



MAX 9000 and MAX 7000S Devices

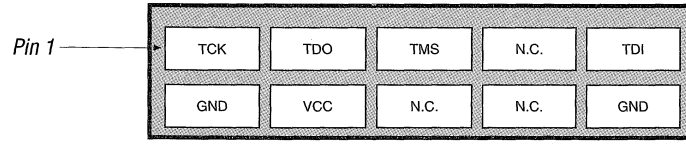


Table 10 lists the significant pin signals for the 25-pin female RS-232 port.

Table 2. BitBlaster 25-Pin Serial Port Pinouts

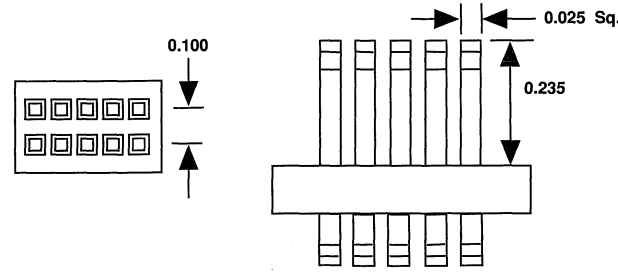
Pin	Signal Name	Description
2	TX	Transmit data
3	RX	Receive data
4	RTS	Request to send
5	CTS	Clear to send
6	DSR	Data set ready
7	GND	Signal ground
20	DTR	Data terminal ready

Circuit Board Male Header Connection

The BitBlaster's 10-pin female header connects to a 10-pin male header on the circuit board. Figure 15 shows the dimensions for a typical 10-pin male header used in their connections. The 10-pin male header has two rows of five pins, spaced 0.1 inch apart from the pin centers, that connect to the programming or configuration pins of the device.

Figure 3. 10-Pin Male Header Dimensions

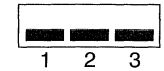
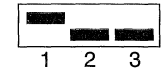
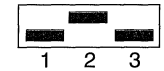
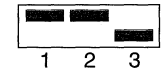
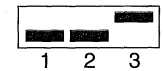
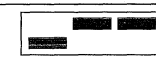
Controlling measurement is in inches.



Data Transfer Rate Control

The three dipswitches on the BitBlaster's side panel control the baud rate of the serial data. Table 11 shows the dipswitch settings, which can be used to specify a baud rate ranging from 9,600 to 230,400 bps. The configuration time for an EPF81188 device, which has 193,000 bits of configuration data, is also provided for reference.

Table 3. Dipswitch Settings

Baud Rate (bps)	Dipswitch Positions	EPF81188 Configuration Time (seconds)
230,400 *Note (1)*	 1 2 3	1.5
115,200	 1 2 3	3.0
76,800	 1 2 3	4.5
57,600	 1 2 3	5.5
38,400	 1 2 3	8.5
19,200	 1 2 3	17.0
14,400	 1 2 3	22.0
9,600	 1 2 3	33.0

Note:
(1) This baud rate is not supported in all systems.

FLEX 10K & FLEX 8000 Device Configuration

The BitBlaster can be used to configure FLEX 10K or FLEX 8000 devices with a command entered at a PC or workstation system prompt or with the PC- or workstation-based MAX+PLUS II Programmer. Prototyping is easy, since design changes are downloaded directly to the device. Contact Altera Marketing for more information on FLEX 10K devices. For information on FLEX 8000 specifications and pin-outs, refer to the *FLEX 8000 Programmable Logic Device Family Data Sheet* in this data book.

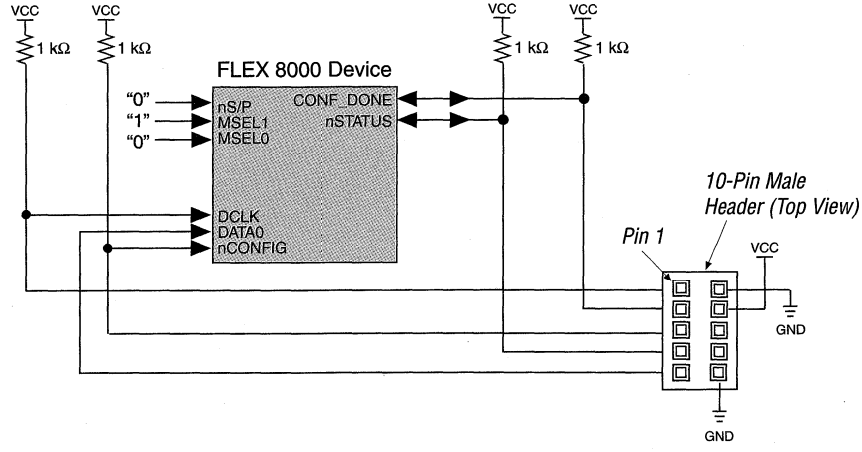
The SRAM-based FLEX 10K and FLEX 8000 device families can be configured in several different schemes. The passive serial (PS) configuration scheme uses an external controller such as the BitBlaster to configure a FLEX 10K or FLEX 8000 device with a serial bitstream. The device is treated as a slave with a 5-wire interface to the external controller.

See *Application Note 33 (Configuring FLEX 8000 Devices)* for more information about device configuration with the BitBlaster.

The BitBlaster can connect any standard RS-232 port to a single FLEX 10K or FLEX 8000 device in the prototype system. The MAX+PLUS II Programmer downloads the configuration data in the SRAM Object File (**.sof**) for the device, which is generated automatically during project compilation. Alternatively, a Serial Bitstream File (**.sbf**) can be used to configure a FLEX 10K or a FLEX 8000 device from a system prompt. Once the device is configured, the programming hardware is tri-stated and electrically removed from the circuit. This configuration method allows the designer to perform multiple design iterations in quick succession.

Figure 16 shows how the BitBlaster interface to a target FLEX 8000 device. If the DATA0 carrier is used in the user mode, it must be isolated during configuration.

Figure 4. FLEX 8000 Passive Serial Device Configuration with the BitBlaster

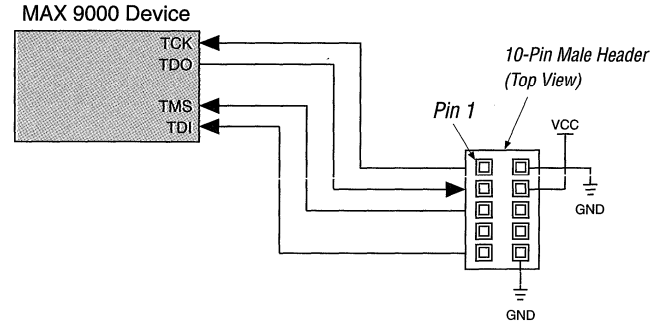


MAX 9000 & MAX 7000S Device Programming

The BitBlaster can be used with the MAX+PLUS II Programmer on a PC or workstation to program a MAX 9000 or MAX 7000S device.

The BitBlaster can connect any standard RS-232 port to a single EEPROM-based MAX 9000 or MAX 7000S device in the prototype system. A Programmer Object File (**.pof**), which is generated automatically during project compilation, is downloaded to the BitBlaster by the MAX+PLUS II Programmer. Programming is accomplished via a subset of the device JTAG pins, specifically: TCK, TMS, TDI, and TDO. Figure 5 shows how the BitBlaster interfaces with the target MAX 9000 or MAX 7000S device. The I/O pins are tri-stated during in-system programming.

Figure 5. MAX 9000 & MAX 7000S Device Programming with the BitBlaster



Step-by-Step Instructions

Configuration or programming data can be downloaded with the MAX+PLUS II Programmer. For FLEX 10K and FLEX 8000 devices, configuration data can also be sent directly from a PC or a workstation by converting the SOF to an SBF, and then copying the SBF to a COM port.

Downloading Configuration or Programming Data from the MAX+PLUS II Programmer

To configure or program devices with the BitBlaster and the MAX+PLUS II Programmer:

1. Compile a project with the MAX+PLUS II Compiler. The Compiler automatically generates an SOF for FLEX 10K and FLEX 8000 device configuration, or a POF for MAX 9000 or MAX 7000S programming.

2. Attach the BitBlaster to an RS-232 port and plug the 10-pin female header into the prototype system that contains the target device. Make sure that the POWER status light is on. The board must supply power to the BitBlaster.

3. If necessary, change the baud rate of the BitBlaster using the dipswitches on its side panel. Dipswitch settings are listed in Table 11.

4. Open the MAX+PLUS II Programmer and choose **Hardware Setup** (Options menu). In the **Hardware Type** dialog box, choose **Auto-Setup** to automatically update the Hardware Type and COM port fields. Choose **OK**.

5. Choose **Select Programming File** (File menu) and specify the correct file type. For a FLEX 10K or a FLEX 8000 device, select an SOF; for a MAX 9000 or MAX 7000S device, select a POF. By default, when you first open the Programmer window, MAX+PLUS II loads the programming file for the current project (usually a POF), or the first programming file for a multi-device project.

6. In the Programmer window, choose **Program** to start downloading the configuration or programming data. The BUSY status light on the BitBlaster turns on.

The BitBlaster downloads the data from the SOF or POF into the device. When configuration or programming is complete, the BUSY status light turns off, and the DONE status light turns on. After the DONE light goes on, you can disconnect the BitBlaster.

Downloading Configuration Data from a System Prompt (FLEX 8000 and FLEX 10K Devices Only)

To configure a FLEX 8000 device with the BitBlaster from a system prompt:

1. Compile a project with the MAX+PLUS II Compiler. The Compiler automatically generates an SOF for FLEX 8000 or FLEX 10K device configuration.

2. Open the MAX+PLUS II Programmer or Compiler and choose the **Combine Programming Files** command (File menu).

3. Specify the SOF name by selecting it in the *Files* box or by typing its name in the *File Name* box under *Input Files*. Choose **Add** to add the file to the *Selected Files* box.

4. Specify the desired configuration file format by selecting *.sbf (Sequential)* in the *File Format* drop-down list box under *Output File*. Choose **OK**.

5. Attach the BitBlaster to an RS-232 port on your PC or workstation, and plug the 10-pin female header into the prototype system that contains the target FLEX 8000 device. Make sure that the POWER status light is on. The board must supply power to the BitBlaster.

6. If necessary, change the baud rate of the BitBlaster using the dipswitches on its side panel . Dipswitch settings are listed in Table 11.

7. Specify an RS-232 port and set its baud rate.

   When configuring from a system prompt on a PC, the serial port transmits but does not receive data. Therefore, baud rates higher than the DOS limit of 9,600 may be used.

   ✓ On a PC, follow these steps:

   a. For 9,600 baud, type the following command from the system prompt:

      `mode com` *<port number>*`:9600,N,8,1` ↵

   b. For baud rates greater than 9,600, type the following command from the system prompt:

      `slikmode/b`*<baud rate>*`/c`*<port number>* ↵

      The **slikmode.exe** utility is available on the Altera bulletin board service (BBS) at (408) 954-0104, or from the Altera ftp site at **ftp.altera.com** in the self-extracting file **bitmode.exe**. For more detailed instructions about options for the **slikmode.exe** utility, type `slikmode` ↵.

   or:

   ✓ On a workstation, type the following command from the system prompt:

      `stty` *<baud rate>* `< /dev/`*<serial port #>* ↵

      Check the workstation specifications to determine the maximum baud rate allowed by the hardware.

8. Configure the FLEX 8000 device by copying the SBF to the serial port to which the BitBlaster is attached.

✓ On a PC, type the following command from the system prompt:

```
copy <filename>.sbf com<port number>: ↵
```

or:

✓ On a workstation, type the following command from the system prompt:

```
cp <filename>.sbf /dev/<serial port#> ↵
```

Notes:

Altera Programming Hardware

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General Description

Altera offers a variety of hardware to program and configure Altera devices. The following products are available:

- Altera Stand-Alone Programmer
- Logic Programmer card
- Master Programming Unit
- FLEX Download Cable
- BitBlaster Serial Download Cable

Altera Stand-Alone Programmer

The Altera Stand-Alone Programmer, PL-ASAP2, together with the appropriate programming adapters, provides the hardware and software needed for programming EPROM-, EEPROM-, and FLASH-based Altera devices. PL-ASAP2 includes an LP6 Logic Programmer card, an MPU, MAX+PLUS II Programmer software (which requires Microsoft Windows or Windows NT), and complete documentation. The MAX+PLUS II Programmer software supports device configuration for FLEX 10K and FLEX 8000 and device programming for MAX 9000, MAX 7000, MAX 5000, and Classic devices. Programming support for the EP224, EP312, EP324, EP22V10E, and EP22V10 is provided by industry-standard programmers.

Ordering Code: PL-ASAP2

Logic Programmer Card

The LP6 Logic Programmer card generates programming waveforms and voltages for the Master Programming Unit (MPU). It interfaces with IBM PC-AT and compatible computers. This card is software-controlled and can be installed into any full-length expansion slot in a computer.

Ordering Code: PLP6

Master Programming Unit

The Master Programming Unit (MPU) is a hardware module that is used together with an appropriate adapter to program Altera devices. The MPU connects to a Logic Programmer card via a 25-pin ribbon cable. The MPU receives power from the Logic Programmer card installed in an IBM PC-AT or compatible computer and does not require an external power supply. Programming and functional test information is transmitted from the Logic Programmer card through the ribbon cable to the MPU. A programming status light on the MPU lights up when the unit is active.

When used with the appropriate adapter, the MPU automatically tests for continuity between the device leads and the programming socket before programming. It can also apply test vectors to functionally test and verify programmed Altera devices. Test vectors can be created in waveform or text format in the MAX+PLUS II Waveform Editor or Text Editor and applied to the device; results can be viewed in waveform or text format.

Ordering Code: PL-MPU

Programming Adapters & FLEX Download Cable

Altera provides three types of programming adapters for Altera devices: PLM-prefix adapters, PLE-prefix adapters, and PLAD3-12 compatibility adapters.

The PLM-prefix adapters plug directly into the MPU. Each of these adapters provides programming support for a specific device package. Additionally, these adapters (except the PLMJ1213 and PLMT1064) support functional testing of programmed Altera devices. The PLMJ1213 and PLMT1064 adapters support the FLEX 8000 devices and their associated Configuration EPROMs. These two adapters may either program the Configuration EPROMs used to configure FLEX 8000 devices or download configuration data directly to the FLEX 8000 device via the FLEX Download Cable.

The PLE-prefix adapters plug into the PLAD3-12 adapter, which in turn plugs into the MPU. Each of these adapters provides programming support for a specific Classic device.

The PLAD3-12 compatibility adapter plugs directly into the MPU. This adapter allows PLE-prefix adapters to be used with the MPU, and provides programming support for EP220 and EP330 devices.

Each adapter contains one of the following sockets: a zero-insertion-force dual in-line package (DIP), J-lead, pin-grid array (PGA), small-outline integrated circuit (SOIC), or quad flat pack (QFP). The adapters for QFP devices with 100 or more pins support Altera's QFP carrier technology.

See the *QFP Carrier & Development Socket Data Sheet* in this data book for more information.

Table 1 lists the required adapters for each Altera device and package option.

Table 1. Device Adapter Support (Part 1 of 3)

Device	Package	Adapter	BitBlaster Support
EP220	DIP J-lead	PLAD3-12 PLEJ330	–
EP224	DIP J-lead	*Note (1)*	–
EP22V10/22V10V/ 22V10E	DIP J-lead	*Note (1)*	–
EP312	DIP J-lead	*Note (1)*	–
EP324	DIP J-lead	*Note (1)*	–
EP330/320I	DIP J-Lead SOIC	PLAD3-12 PLEJ330 PLES330	–
EP600/600I/610/ 610I/610T	DIP J-lead SOIC	PLED610 PLEJ610 PLES610	–
EP900/900I/910/ 910I/910T	DIP J-lead	PLED910 PLEJ910	–
EP1800/1800I/1810/ 1810T	J-lead PGA	PLMJ1810 PLEG1810	–
EPM5032/5032A	DIP J-lead SOIC	PLMD5032A PLMJ5032A PLMS5032A	–
EPM5064/5064A	J-lead	PLMJ5064A	–
EPM5128/5128A	J-lead PGA	PLMJ5128A PLMG5128A	–
EPM5130/5130A	J-lead PGA PQFP	PLMJ5130A PLMG5130A PLMQ5130A	–

Table 1. Device Adapter Support (Part 2 of 3)

Device	Package	Adapter	BitBlaster Support
EPM5192/5192A	J-lead PGA PQFP (EPM5192A only)	PLMJ5192A PLMG5192A PLMQ5192A	–
EPX740	J-lead (44-pin) J-lead (68-pin)	PLMJ740-44 PLMJ740-68	✓ *(2)*
EPX780	J-lead PQFP	PLMJ780-84 *Note (1)*	✓ *(2)*
EPX880	J-lead PQFP	*Note (3)*	✓ *(2)*
EPX8160	PQFP (208-pin)	PLMQ8160-208	✓ *(2)*
EPM7032/7032V	J-lead PQFP TQFP	PLMJ7000-44 PLMQ7000-44 PLMT7000-44	–
EPM7064	J-lead (44-pin) PQFP (44-pin) TQFP (44-pin) J-lead (68-pin) J-lead (84-pin) PQFP (100-pin)	PLMJ7000-44 PLMQ7000-44 PLMT7000-44 PLMJ7000-68 PLMJ7000-84 PLMQ7000-100	–
EPM7096	J-lead (68-pin) J-lead (84-pin) PQFP (100-pin)	PLMJ7000-68 PLMJ7000-84 PLMQ7000-100	–
EPM7128/7128E	J-lead (68-pin) J-lead (84-pin) PQFP (100-pin) PQFP (160-pin)	PLMJ7000-68 PLMJ7000-84 PLMQ7000-100 PLMQ7128/7160-160	–
EPM7160/7160E	J-lead (84-pin) PQFP (100-pin) PQFP (160-pin)	PLMJ7000-84 PLMQ7000-100 PLMQ7128/7160-160	–
EPM7192/7192E	PGA PQFP	PLMG7192-160 PLMQ7192/7256-160	–
EPM7256E	PGA (192-pin) PQFP (160-pin) PQFP (208-pin)	PLMG7256-192 PLMQ7192/7256-160 PLMR7256-208	–
FLEX 8000 devices	All	*Note (4)*	✓
EPC1064	DIP J-lead TQFP	PLMJ1213 PLMJ1213 PLMT1064	–

Table 1. Device Adapter Support (Part 3 of 3)

Device	Package	Adapter	BitBlaster Support
EPC1213	DIP J-lead	PLMJ1213 PLMJ1213	–
EPM9320	J-lead (84-pin) RQFP (160-pin) RQFP (208-pin) PGA (280-pin)	PLMJ9320-84 PLMR9320-160 PLMR9000-208 PLMG9000-280	✓
EPM9400	J-lead (84-pin) RQFP (208-pin) RQFP (240-pin) PGA (280-pin)	PLMJ9400-84 PLMR9000-208 PLMR9000-240 PLMG9000-280	✓
EPM9480	RQPF (160-pin) RQFP (208-pin) RQFP (240-pin) PGA (280-pin)	PLMR9480-160 PLMR9000-208 PLMR9000-240 PLMG9000-280	✓
EPM9560	RQFP (208-pin) RQFP (240-pin) PGA (280-pin) RQFP (304-pin)	PLMR9000-208 PLMR9000-240 PLMG9000-280 PLMR9000-304	✓

Notes:
(1) Programming support is currently provided through third-party vendors. Contact Altera Applications at (800) 800-EPLD for additional information.
(2) This information is preliminary. BitBlaster support for this device will be available in mid 1995.
(3) Consult Altera Applications for information on programming support.
(4) Configuration of FLEX 8000 devices is supported by Configuration EPROMs (EPC1064, EPC1064V, and EPC1213), the FLEX Download Cable, and the BitBlaster.

Ordering Codes: PLE-XXX, PLM-XXX, PLAD3-12

BitBlaster Serial Download Cable

The BitBlaster serial download cable is a hardware interface to a standard RS-232 port (called a "COM port" on a PC) that provides configuration data to FLEX 10K and FLEX 8000 devices and programming data to MAX 9000 and MAX 7000S devices. FLASHlogic support will be available in the second half of 1995.

The 25-pin female port on the BitBlaster is connected to an RS-232 port with a standard serial cable. The 10-pin female plug on the BitBlaster is connected to a device on a circuit board via a 10-pin male header. The BitBlaster contains status lights that indicate the state of the device configuration or programming. Refer to the *BitBlaster Serial Download Cable Data Sheet* in this data book for more information for more information.

Ordering Code: PL-BITBLASTER

Programming Support

Altera customers can create a device programming environment or add to their existing device programming support with the hardware shown in Table 2.

Table 2. Programming Hardware Requirements

If you have . . .	And you want to program . . .	Then you need . . .
No programming hardware	EP610 EP910 EP1810 (PGA)	PL-ASAP2, appropriate programming adapters
No programming hardware	EP1810 (J-lead) Any MAX 5000 device Any MAX 7000 device Any MAX 9000 device Any Configuration EPROM	PL-ASAP2, PLAD3-12 adapter, appropriate programming adapters
LP6 Logic Programmer card	EP610 EP910 EP1810 (PGA)	PL-MPU, PLAD3-12 adapter, appropriate programming adapters
LP6 Logic Programmer card	EP1810 (J-lead) Any MAX 5000 device Any MAX 7000 device Any MAX 9000 device Any Configuration EPROM	PL-MPU, appropriate programming adapters
LP6 Logic Programmer card, PL-MPU Master Programming unit	EP610 EP910 EP1810 (PGA)	PLAD3-12 adapter, appropriate programming adapters
LP6 Logic Programmer card, PL-MPU Master Programming unit	EP1810 (J-lead) Any MAX 5000 device EPX740 EPX780 (J-lead) Any MAX 7000 device Any MAX 9000 device Any Configuration EPROM	Appropriate programming adapters

EDA Software Support

March 1995

Introduction

Altera recognizes the importance of supporting industry-standard design tools, and works closely with leading EDA software manufacturers to provide high-quality development support for Altera programmable logic devices. To ensure strategic partnerships with EDA tool manufacturers, Altera has established the Altera Commitment to Cooperative Engineering Solutions (ACCESS) program. Through this program, Altera and its EDA partners work together to develop either direct support for Altera devices or seamless integration with the Altera MAX+PLUS II development software.

For more information on software support provided by Altera, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* in this data book.

Table 3 summarizes each company's design entry, compilation/ synthesis, and simulation/verification products that support Altera devices directly or provide an interface to MAX+PLUS II. As shown in Table 1, Altera supplies design interface kits for several EDA tools. Altera recommends contacting EDA software manufacturers directly for details on product features, specific device support, and product availability. While Altera provides technical assistance to these companies, final responsibility for the quality and accuracy of these products rests with the manufacturers. This document also describes the typical design flow for Altera's interfaces to Cadence, Mentor Graphics, Synopsys, and Viewlogic. For detailed information on these four interfaces, refer to the following documents: *Application Note 29 (Cadence & MAX+PLUS II Logic Design)*, *Application Note 32 (Mentor Graphics & MAX+PLUS II Logic Design)*, *Application Note 34 (Synopsys & MAX+PLUS II Logic Design)*, and *Application Note 37 (Viewlogic Powerview & MAX+PLUS II Logic Design)*.

Table 1. Standard EDA Support for Altera Devices (Part 1 of 4)

Company	Product	Design Entry	Compilation/ Synthesis	Simulation/ Verification
Accel Technologies, Inc. TEL: (619) 554-1000 FAX: (619) 554-1019	TangoPLD Tango-Schematic	✓ ✓	✓	✓ ✓
ACEO Technology TEL: (510) 656-2189 FAX: (510) 770-9937	Asyn Gatran Softwire		✓ ✓ ✓	
Acugen Software, Inc. TEL: (603) 881-8821 FAX: (603) 881-8906	AADELAY AAMAX ATGEN Test Vectors			✓ ✓ ✓ ✓
Aldec TEL: (805) 499-6867 FAX: (805) 498-7945	Susie-CAD Susie 6	✓		✓
Cadence Design Systems, Inc. TEL: (408) 943-1234 FAX: (408) 943-0402	Composer *(1)* Concept *(1)* FPGA Solution *(1)* Synergy *(1)* RapidSIM *(1)* Verilog-XL *(1)* Leapfrog *(1)*	✓ ✓ ✓	 ✓ ✓	 ✓ ✓ ✓
Chronologic Simulation TEL: (415) 965-3312 FAX: (415) 965-2705	VCS			✓
COMPASS Design Automation TEL: (408) 433-4880 FAX: (408) 434-7820	Logic Assistant ASIC Synthesizer QSIM	✓	 ✓	 ✓
Data I/O Corp. TEL: (800) 247-5700 FAX: (206) 882-1043	ABEL Synario	✓ ✓	✓ ✓	✓ ✓
Exemplar Logic, Inc. TEL: (510) 849-0937 FAX: (510) 849-9935	CORE Solution CORE/V-System CORE/Analyze		✓	 ✓ ✓
Flynn Systems Corp. TEL: (603) 891-1111 FAX: (603) 891-1074	FS-High Density FS-PALibrary			✓ ✓
Front Line TEL: (408) 456-0222 FAX: (408) 456-0265	Baseline			✓

Table 1. Standard EDA Support for Altera Devices (Part 2 of 4)

Company	Product	Design Entry	Compilation/ Synthesis	Simulation/ Verification
Harmonix TEL: (617) 935-8335 FAX: (617) 935-8530	Parthenon		✓	
IBM TEL: (800) 765-4426 FAX: (800) 992-4777	Boole Dozer *(1)*		✓	
IK Technology Co., Ltd. (Japan) TEL: (81) 3-3464-5551 FAX: (81) 3-3464-5689	Galahad	✓	✓	✓
IKOS Systems TEL: (408) 255-4567 FAX: (408) 366-8699	Voyager			✓
i-Logix TEL: (508) 682-2100 FAX: (508) 682-5995	Express V-HDL	✓		✓
Intergraph Corp. TEL: (800) 345-4856 FAX: (303) 581-9972	ACEPlusDesigner Synovation VeriBest AdvanSIM-1076 AdvanSIM VHDL	✓	✓ ✓	 ✓ ✓ ✓
ISDATA GmbH (Germany) TEL: (49) 721/75 10 87 FAX: (49) 721/75 26 34	LOG/iC Hint	✓ ✓	✓	
Innovative Synthesis Technology TEL: (510) 736-2302 FAX: (510) 736-6199	ASYL+		✓	
Logic Modeling Corp. TEL: (503) 690-6900 FAX: (503) 690-6906	SmartModel PLD-Debug			✓ ✓
Logical Devices, Inc. TEL: (800) 331-7766 FAX: (305) 428-1811	CUPL	✓	✓	✓
Mentor Graphics Corp. TEL: (503) 685-7000 FAX: (503) 685-1268	FPGA Station *(1)* Design Architect *(1)* AutoLogic *(1)* PLDSynthesis II QuickVHDL *(1)* QuickSim II *(1)*	✓ ✓ ✓ ✓	✓ ✓ ✓	✓ ✓ ✓

Table 1. Standard EDA Support for Altera Devices (Part 3 of 4)

Company	Product	Design Entry	Compilation/ Synthesis	Simulation/ Verification
MINC Inc. TEL: (719) 590-1155 FAX: (719) 590-7330	PLDesigner-XL	✓	✓	✓
Model Technology TEL: (503) 641-1340 FAX: (503) 526-5410	V-System			✓
OrCAD Systems Corp. TEL: (503) 671-9500 FAX: (503) 671-9501	PLD MOD SDT VST	✓ ✓ 	✓ 	✓ ✓ ✓
Quad Design TEL: (805) 988-8250 FAX: (805) 988-8259	Motive			✓
Simucad TEL: (510) 487-9700 FAX: (510) 487-9721	Silos III			✓
Sophia Systems TEL: (415) 493-6700 FAX: (415) 493-4648	Vanguard	✓		
Summit Design TEL: (503) 643-9281 FAX: (503) 646-4954	Visual-HDL	✓		
Synopsys TEL: (415) 962-5000 FAX: (415) 694-4249	Design Compiler *(1)* FPGA Compiler *(1)* DesignWare *(1)* VSS		✓ ✓ ✓ 	 ✓
Synplicity Inc. TEL: (415) 961-4962 FAX: (415) 961-4974	Synplify-Lite		✓	
Vantage Analysis Systems TEL: (510) 659-0901 FAX: (510) 659-0129	Optima			✓
Veda (formerly GenRad) TEL: (800) 600-VEDA FAX: (408) 970-0174	Hilo Vulcan System HILO 4			✓ ✓ ✓

Table 1. Standard EDA Support for Altera Devices (Part 4 of 4)

Company	Product	Design Entry	Compilation/ Synthesis	Simulation/ Verification
Viewlogic Systems, Inc.	ViewDraw *(1)*	✓		
TEL: (508) 480-0881	PROcapture *(1)*	✓		
FAX: (508) 480-0882	PROchip Altera *(1)*	✓	✓	✓
	Altera Prog. Expert	✓	✓	✓
	ViewFPGA *(1)*	✓	✓	✓
	ViewPLD	✓	✓	✓
	ViewSynthesis *(1)*		✓	
	PROsynthesis		✓	
	ViewSim *(1)*			✓
	Vantage-VHDL *(1)*			✓
	VCS *(1)*			✓
	PROsim *(1)*			✓
	PROvhdl			✓
Vista Technologies	DesignVision	✓		
TEL: (708) 706-9300	Vista Model Creator	✓		
FAX: (708) 706-9317	VHDL Developer Plus	✓		

Note:
(1) Design interface kits are available from Altera.

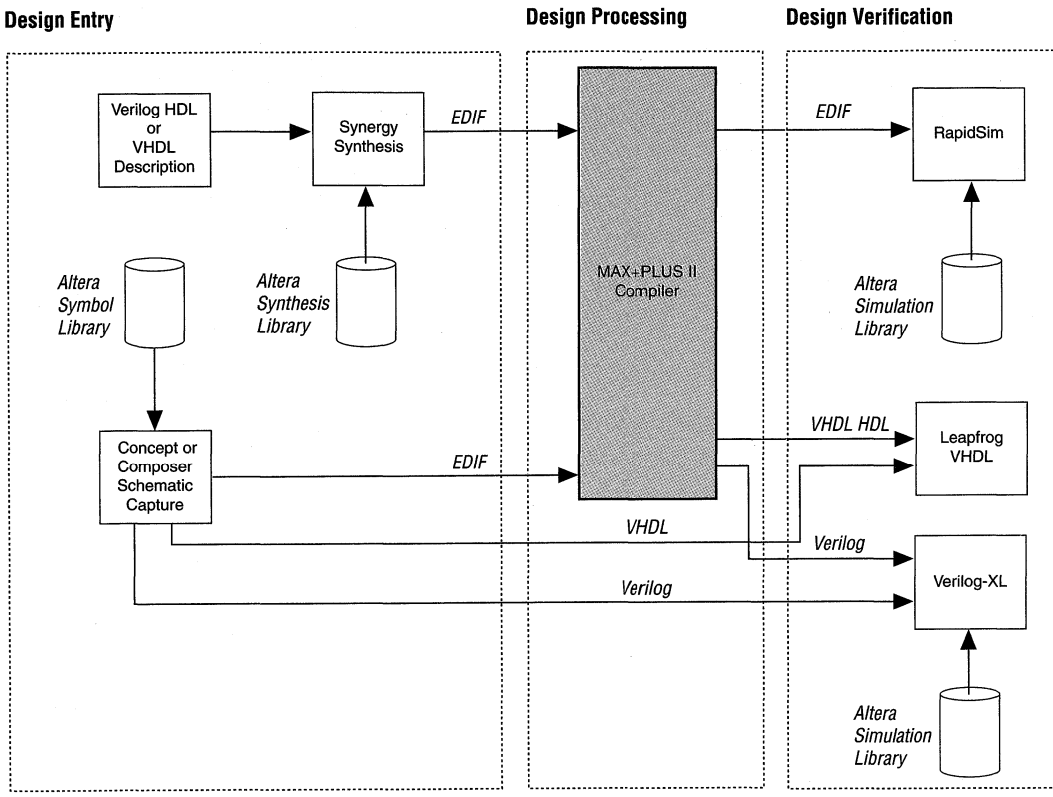
Altera/Cadence Interface

The MAX+PLUS II development software fully supports the Cadence Logic Workbench and Design Framework II design environments. By combining Cadence design entry, synthesis, and verification tools with MAX+PLUS II, designs can be implemented in any of the Altera programmable logic device families.

The Altera/Cadence interface supports a top-down or mixed-level design methodology. Designs can be entered as a mixture of schematics, VHDL, and Verilog HDL. Schematics are entered with Cadence Concept or Composer schematic capture tools using basic gates, macrofunctions, library of parameterized modules (LPM) symbols, and TTL symbols from the symbol libraries supplied by Altera and Cadence. Device resource assignments entered in the schematic are interpreted by MAX+PLUS II. Assignments can also be entered in MAX+PLUS II for all designs using Assign menu commands and the MAX+PLUS II Floorplan Editor. Verilog HDL and VHDL descriptions are synthesized and optimized by the Cadence Synergy synthesis tool and mapped to Altera devices with a technology library supplied by Altera. The design is saved in EDIF format and is then processed by the MAX+PLUS II Compiler, which provides architecture-specific logic synthesis, optimization, and device fitting.

To ensure that a post-routed design is correct and meets customer performance requirements, the MAX+PLUS II Compiler generates timing-annotated Verilog and VHDL netlist files for verification with Cadence Verilog-XL and Leapfrog VHDL simulators. MAX+PLUS II also generates standard EDIF netlist files that contain timing information for simulation with the Cadence RapidSIM simulator. See Figure 1 for a typical design flow.

Figure 1. Design Flow between Cadence & MAX+PLUS II



Altera/Mentor Graphics Interface

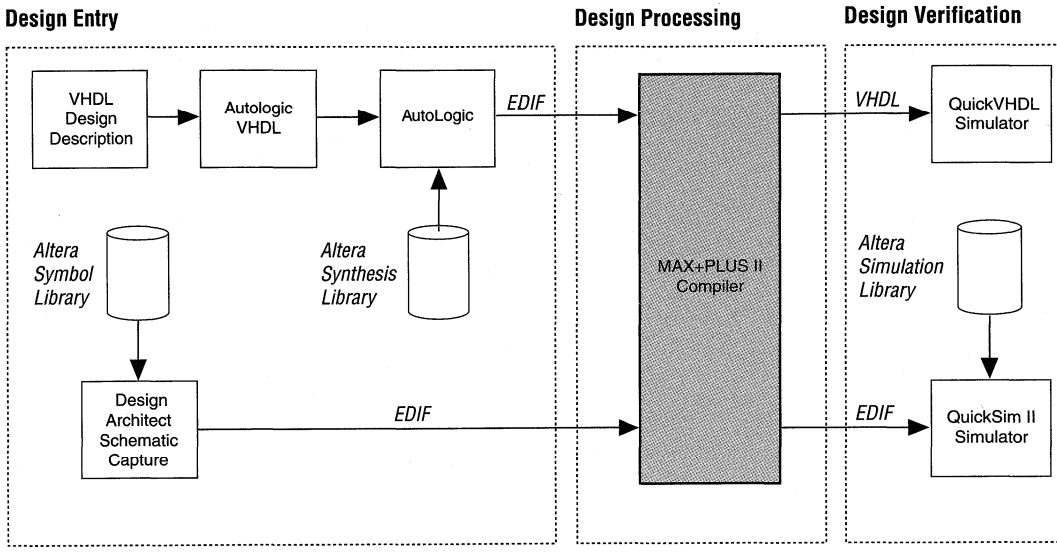
Mentor Graphics Corporation

The MAX+PLUS II software is fully integrated into the Mentor Graphics Falcon Framework. By combining Mentor Graphics design entry, synthesis, and verification tools with MAX+PLUS II, designs can be implemented in any of the Altera programmable logic device families.

The Altera/Mentor Graphics design flow supports a top-down or mixed-level design methodology. Designs can be entered as a mixture of schematics and VHDL. Schematics are entered in the Mentor Graphics Design Architect using familiar basic gates, macrofunctions, LPM, and TTL symbols from a symbol library provided by Altera. Device and resource assignments entered in the schematic are interpreted by MAX+PLUS II. Assignments can also be entered in MAX+PLUS II for all designs using Assign menu commands and the MAX+PLUS II Floorplan Editor. VHDL design descriptions are synthesized and optimized by the Mentor Graphics AutoLogic tool and mapped with an Altera synthesis library to Altera devices. The design is saved in EDIF format and is then processed by the MAX+PLUS II Compiler, which provides architecture-specific logic synthesis, optimization, and device fitting.

To ensure that a post-routed design is correct and meets customer performance requirements, the MAX+PLUS II Compiler generates timing-annotated VHDL netlist files for verification with the Mentor QuickVHDL simulator. MAX+PLUS II also generates timing-annotated industry-standard EDIF netlist files that, combined with the Altera-provided simulation library, support the Mentor QuickSim II simulator. See Figure 2 for a typical design flow.

Figure 2. Design Flow between Mentor Graphics & MAX+PLUS II



Altera/ Synopsys Interface

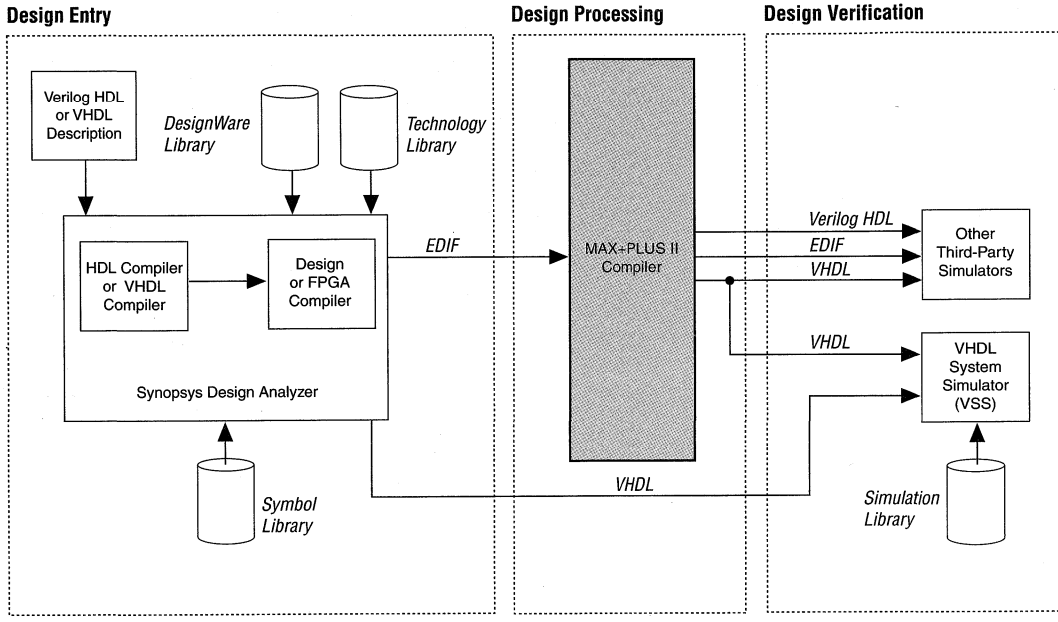
SYNOPSYS®

The MAX+PLUS II software fully supports the Synopsys design environment. The Synopsys/Altera interface brings high-level design methodology to high-density programmable logic. The Design Kit contains Altera synthesis and simulation libraries, which describe logic functions that can be used to implement designs in Altera programmable logic devices. With these libraries, the Synopsys Design Compiler or FPGA Compiler can synthesize VHDL or Verilog HDL design descriptions to target any of the Altera programmable logic device families.

Designs are synthesized to meet user-specified area and timing goals. Design timing constraints entered in the Design Compiler or FPGA Compiler are automatically transferred to the MAX+PLUS II Compiler, providing integration between design concept and implementation. Assignments can also be entered in MAX+PLUS II for all designs using Assign menu commands and the MAX+PLUS II Floorplan Editor. In addition, a DesignWare library is supplied for the Altera FLEX 8000 family of devices, offering area optimization and higher performance. The design is saved in EDIF format and is then processed by the MAX+PLUS II Compiler, which provides architecture-specific logic synthesis, optimization, and device fitting.

To ensure that a post-routed design is correct and meets customer performance requirements, the MAX+PLUS II Compiler generates timing-annotated VHDL netlist files for verification with the Synopsys VHDL System Simulator (VSS). See Figure 3 for a typical design flow.

Figure 3. Design Flow between Synopsys & MAX+PLUS II



Altera/ Viewlogic Interface

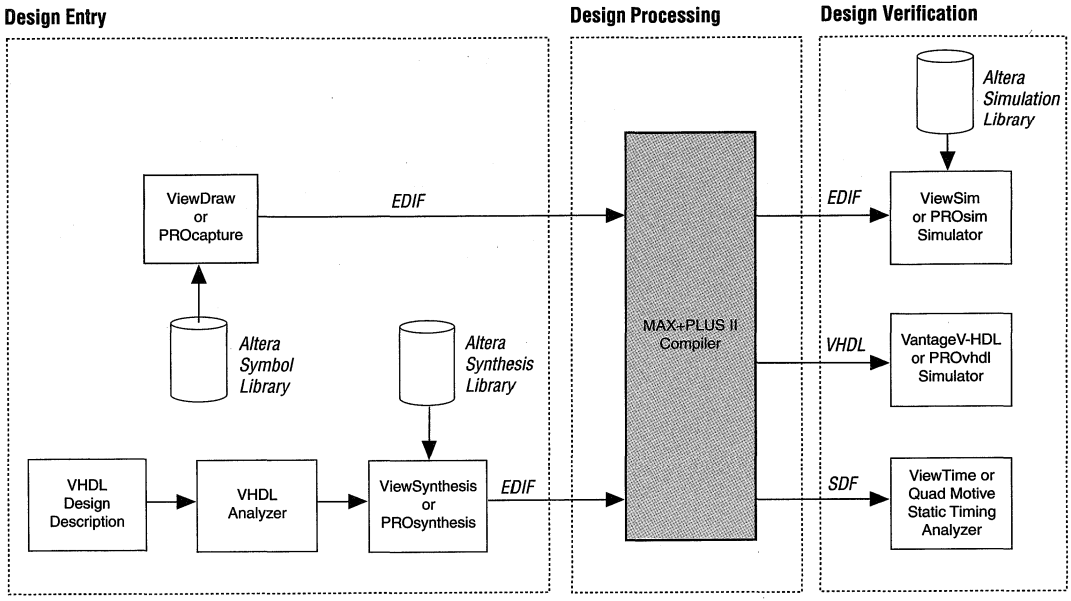
VIEWlogic

The MAX+PLUS II software is fully integrated into Viewlogic Powerview, Workview PLUS, and PRO Series product families, supporting both workstation and PC platforms. By combining Viewlogic design entry, synthesis, and verification tools with MAX+PLUS II, designs can be implemented in any of the Altera programmable logic device families. MAX+PLUS II support for the PRO Series, including PROcapture, PROsynthesis, PROsim, and PROvhdl, is planned for the second half of 1995. Contact Altera Applications for more information.

The Viewlogic/Altera design flow supports a top-down or mixed-level design methodology. Designs can be entered as a mixture of schematics, VHDL, and ABEL. Schematics are entered in Viewlogic ViewDraw or PROcapture using LPM symbols, gates, macrofunctions, and TTL devices from both Viewlogic- and Altera-supplied symbol libraries. Device resource assignments entered in the schematic are interpreted by MAX+PLUS II. Assignments can also be entered in MAX+PLUS II for all designs using Assign menu commands and the MAX+PLUS II Floorplan Editor. VHDL descriptions are synthesized by Viewlogic ViewSynthesis or PROvhdl and mapped with an Altera-supplied technology library to Altera devices. The design is saved in EDIF format and is then processed by the MAX+PLUS II Compiler, which provides architecture-specific logic synthesis, optimization, and device fitting.

To ensure that a post-routed design is correct and meets customer performance requirements, the MAX+PLUS II Compiler generates timing-annotated EDIF netlist files for verification with the ViewSim or PROsim simulators and for timing analysis with the Viewlogic ViewTime and Quad Motive Static Timing Analyzer. MAX+PLUS II also generates post-routed VHDL netlist files for verification with the Viewlogic VantageV-HDL simulator. See Figure 4 for a typical design flow.

Figure 4. Design Flow between Viewlogic & MAX+PLUS II



Notes:

Programming Hardware Manufacturers

March 1995

Introduction

Table 1 lists the manufacturers that offer programming hardware support for Altera devices. Altera recommends contacting manufacturers directly for up-to-date details on product features, specific device support, and product availability. While Altera provides technical assistance to these companies, final responsibility for the quality and accuracy of these products rests with these manufacturers.

Table 1. Programming Hardware Manufacturers (Part 1 of 3)

Manufacturer	Address	Telephone	Fax
Advin Systems, Inc.	1050 E. Duane Avenue, Suite L Sunnyvale, CA 94086	(408) 243-7000	(408) 736-2503
American Advantech	750 East Arques Avenue Sunnyvale, CA 94086	(408) 245-6678	(408) 245-8268
Ando Electric Co. Ltd.	19-7 Kamata, 4-Chome Ota-ku, Tokyo 144 Japan	(81) 3 3733 1161	(81) 3 3739 7310
Aval Data Corp.	M.K. Building 2F 4-8 Nakaitabashi Itabashi-Ku, Tokyo 173 Japan	(81) 3 5375 7321	(81) 3 5375 7717
B & C Microsystems, Inc.	750 N. Pastoria Avenue Sunnyvale, CA 94086	(408) 730-5511	(408) 730-5521
BP Microsystems	1000 N. Post Oak Road, Suite 225 Houston, TX 77055-7237	(713) 688-2620	(713) 688-0920
Bytek Corp.	543 NW 77th Street Boca Raton, FL 33487-1323	(407) 994-3520	(407) 994-3615
Celectronic GmbH	Nordichstrasse, 63-65 D-13406 Berlin 1 Germany	(49) 30 4 13 6075	(49) 30 4 13 6078
Cornelius Consult	Am Siepen 17 D-4630 Bochum 1 Germany	(49) 234 361206	(49) 234 356698
Data I/O Corp.	P.O. Box 97046 Redmond, WA 98073-9746	(206) 881-6444	(206) 882-1043

Table 1. Programming Hardware Manufacturers (Part 2 of 3)

Manufacturer	Address	Telephone	Fax
Elan Digital Systems Limited, U.K.	Elan House, Little Park Farm Road Segensworth West Fareham, Hants PO15 5SJ United Kingdom	(44) 489 579799	(44) 489 577516
ertec GmbH	St. Johann 10 D-8520 Erlangen Germany	(49) 9 131 75570	(49) 9 131 7557 10
HAMIS Haase, Menrad & Co. GmbH	Büssinghof/Böcklerstraße 219 D-3300 Braunschweig Germany	(49) 531 70231	(49) 531 74020
ICE Technical Ltd.	Station Buildings, Penistone South Yorks 530 GHG United Kingdom	(44) 226 767 404	(44) 226 370 434
Instronic Peripherals & Systems	No. 471, 1st Floor, E.S.I. Road, II Block, Rajajinagar Bangalore 560 010 India	(91) 812 324967	(91) 812 324848
Leap Electronic Co., Ltd.	6F-4, No. 4, Lane 609, Sec. 5, Chung Hsin Road, San Chung City, Taipei Hsein Taiwan Republic of China	(86) 2 999 1860	(86) 2 999 0015
Link Computer Graphics, Inc.	369 Passaic Avenue, Suite 100 Fairfield, NJ 07004	(201) 808-8990	(201) 808-8786
Logical Devices, Inc.	130 Capitol Drive Golden, CO 80401	(303) 279-6868 (800) 331-7766	(303) 279-6869
MicroPross	33 Rue Goutois 59000 Lille France	(33) 20 15 11 33	(33) 20 15 11 66
Minato Electronics	3628 Madison Avenue, #5 North Highlands, CA 95660	(916) 348-6066	(916) 348-0926
Needham's Electronics, Inc.	4630 Beloit Drive, Suite 20 Sacramento, CA 95838	(916) 924-8037	(916) 924-8065
Oliver Advanced Engineering	1146 North Central, #360 Glendale, CA 91202	(818) 240-0080	(818) 240-6131
Owen Electronic GmbH	Fritz-Wunderlich-Straße 51 D-6798 Kusel Germany	(49) 6381 4202 0	(49) 6381 4202 85
Products in Motion, Inc.	3054 Fite Circle, #101 Sacramento, CA 95827	(916) 363-0571	(916) 363-0573

Table 1. Programming Hardware Manufacturers (Part 3 of 3)

Manufacturer	Address	Telephone	Fax
Prologic Systems	557-0 Burbank Street Broomfield, CO 80020	(303) 460-0103	(303) 469-5565
SMS GmbH	IM Grund 15 88239 Wangen Germany	(49) 7522-97280	(49) 7522-972850
Stag Microsystems	1600 Wyatt Drive Santa Clara, CA 95054	(408) 988-1118	(408) 988-1232
Sunrise Electronic Inc.	675 Brea Canyon Road, #6 Walnut, CA 91789	(909) 595-7774	(909) 594-7009
Sunshine Electronics Co., Ltd.	Rm. 304, 3F, No. 2, Lane 137 Sec. 5 Ming Shen E. Road Taipei Taiwan Republic of China	(886) 2 7633732	(886) 2 7654065
System General	1603A South Main Street Milpitas, CA 95036	(408) 263-6667	(408) 262-9220
Tribal Microsystems/HiLo Systems	44388 South Grimmer Road Fremont, CA 94538	(510) 623-8859	(510) 623-9925
Xeltek	757 North Pastoria Ave. Sunnyvale, CA 94086	(408) 524-1929	(408) 245-7084

Notes:

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March 1995

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Configuration Elements & Reliability

March 1995, ver. 2 Data Sheet

Introduction

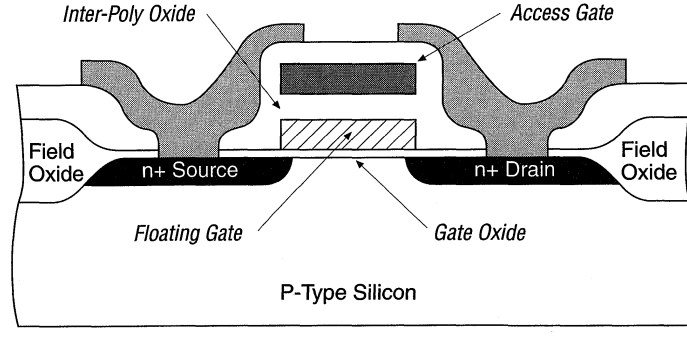
Altera's broad range of programmable logic devices incorporates four types of configuration elements: EPROM, EEPROM, FLASH, and SRAM. To ensure the highest level of device performance and reliability, Altera maintains a comprehensive testing program that carefully monitors the factors affecting the basic programming elements of each device. Altera maintains rigorous quality standards both before a device is put into production and throughout the manufacturing process.

EPROM Configuration Element

The EPROM transistor is a modified NMOS transistor in which the threshold voltage is easily switched between a low voltage (near V_{SS}) and a high voltage (greater than V_{CC}). The different threshold voltages represent the EPROM cell in the on and off states.

The EPROM transistor has a floating polysilicon gate between the access gate and the substrate, as shown in Figure 1. The floating gate is electrically isolated from the substrate by a thin gate oxide that is approximately 200 Å thick, and from the access gate by a thicker dielectric inter-poly oxide that typically consists of oxides and/or nitrides.

Figure 1. EPROM Cell Construction



EPROM transistors are programmed to a high-threshold voltage with hot electron injection. When a high programming voltage, V_{PP} (normally 12.5 V), is applied to the access gate of an EPROM cell, and a slightly lower voltage (V_D) is applied to its drain, electrons flow from the source to the drain. As these electrons pick up kinetic energy, their path is altered by an electric field located between the access gate and substrate. This electric field is generated by the potential difference between V_{PP} on the access gate and V_D on the drain. Electrons that achieve a kinetic energy of 3.2 eV or more accelerate vertically toward the floating gate, pass through the gate oxide, and are trapped on the floating-gate electrode. These excess electrons create a net negative voltage on the floating gate that opposes the electrical field created by the positive voltage on the access gate. The result is a substantial increase in the threshold voltage required to change the EPROM cell into a conducting state. See Figure 2.

Figure 2. EPROM Cell Programming

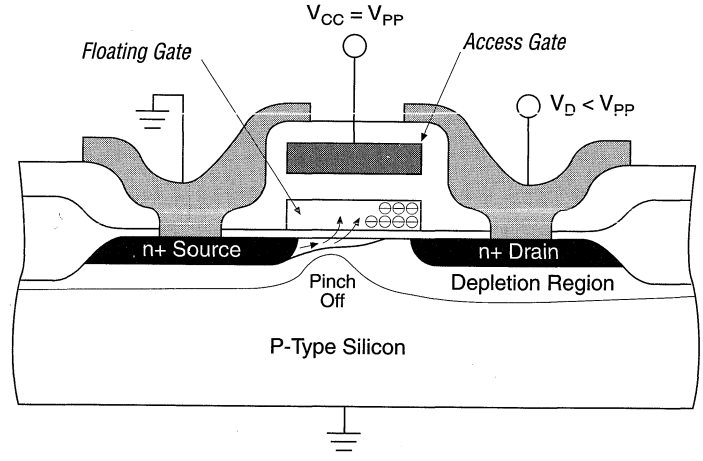
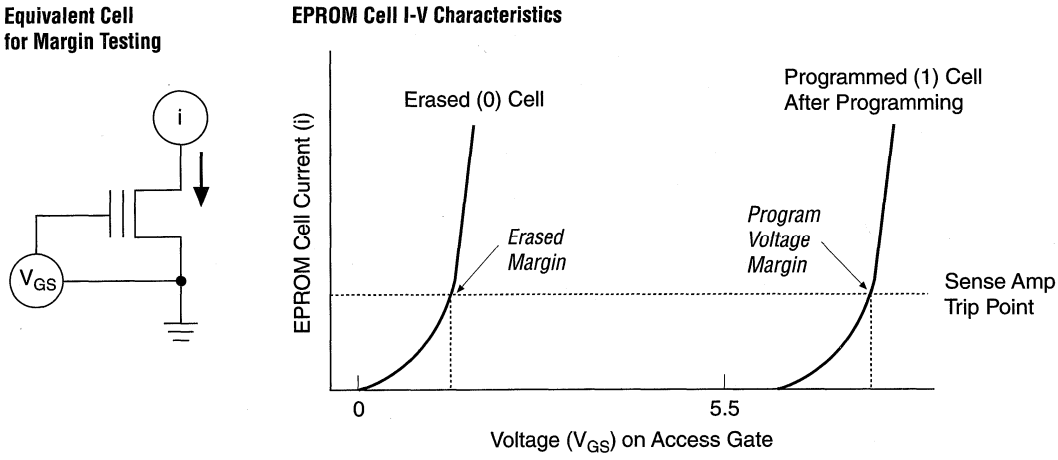


Figure 3 shows the current-voltage (I-V) relationships for programmed (high-threshold voltage) and erased (low-threshold voltage) EPROM cells. The programmed EPROM cell behaves as a transistor that is turned off, because source-drain current does not flow for access-gate voltages ranging from 0 to V_{CC}. In contrast, an erased cell produces source-drain current when its access gate is brought to approximately 1 V, like a transistor that is turned on.

Programmed EPROM cells in the off state are erased by exposing the device to ultraviolet (UV) radiation with wavelengths of 2,540 Å. The excess electrons on the floating gate absorb radiant UV energy; experience a rise in energy level above the 3.2-eV barrier; overcome the oxide-silicon potential barrier; and finally migrate into the substrate where they are neutralized.

Figure 3. Current vs. Voltage Relationships of Erased & Programmed EPROM Cells



EEPROM Configuration Element

The EEPROM transistor, like the EPROM transistor, is an MOS transistor that is either on or off, depending on the threshold voltage. Unlike EPROM devices, however, EEPROM devices can be electrically erased. The EEPROM cell consists of a single, floating polysilicon gate structure used to change the threshold voltage of the transistor. See Figure 4. The threshold voltage is changed when a tunneling mechanism traps an excess of electrons on the floating gate. Fowler-Nordheim tunneling occurs when the floating gate is raised to a high voltage (12 V to 13 V) via capacitive coupling to the N+ implant region. Once the electrons have been trapped on the floating gate, they present a negative shielding voltage and increase the threshold voltage of the transistor, making it impossible to turn the transistor on under normal operating voltages. This process allows the floating gate to act as an on/off switch for the read transistor.

The EEPROM cell is erased with the same tunneling mechanism. Since the electrons are removed from the floating gate, the gate has a net positive charge that allows the EEPROM transistor to be turned on or off, depending on the voltage on the control gate.

For a complete operational description of the EEPROM cell, see *Reliability Report No. 24*, available from Altera or from an Altera sales representative.

Figure 4. EEPROM Cell Construction

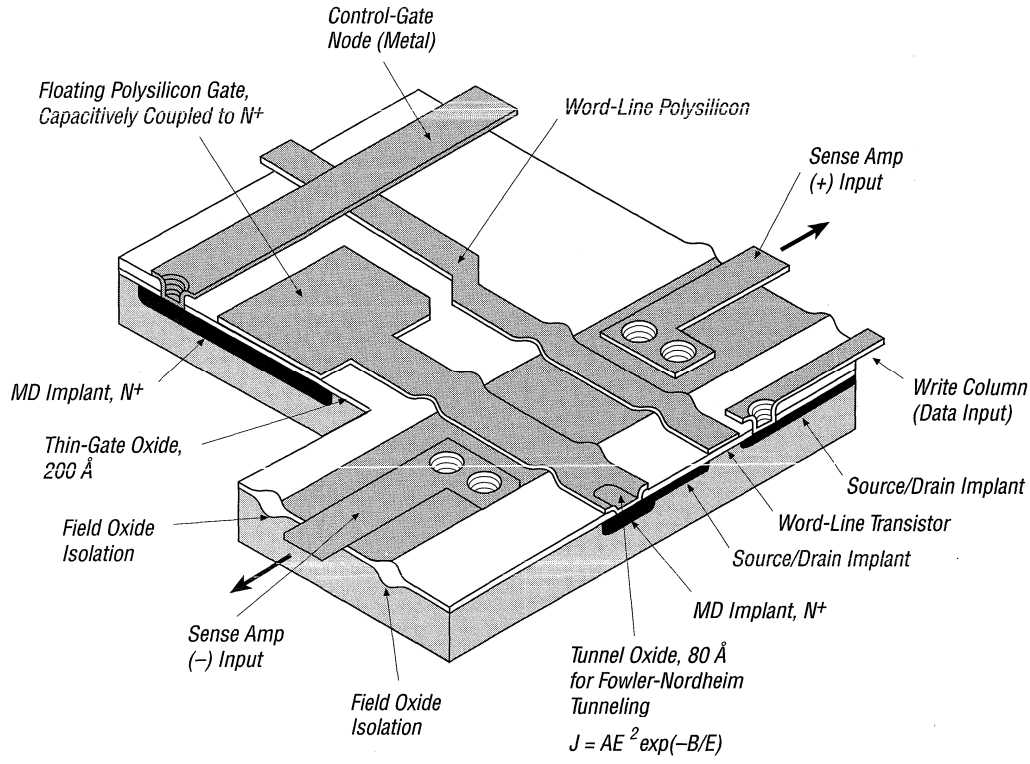
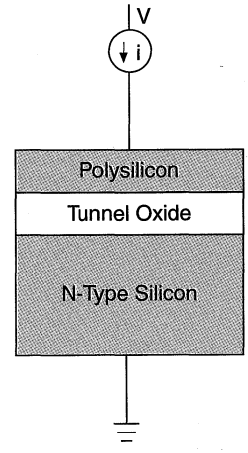


Figure 5 shows a 2-electrode structure in which one electrode is formed by polysilicon and another is formed by a heavily doped N-type silicon diffusion. These electrodes are separated by a tunnel oxide that is approximately 80 Å thick. When typical operating voltages of 5 V or less are applied across the tunnel oxide, it acts as a dielectric and does not conduct electricity. When 12 V to 14 V are applied, however, electrons tunnel through the oxide. This process is characterized by an extremely small tunneling current (less than 10^{-20} A) at typical operating voltages of 5 V or less. At the higher voltages used to erase or program the cell (i.e., charge or discharge the floating gate), the exponential rise in current produces approximately 1 µA of current flow through the tunnel oxide. Depending on the voltage's polarity, this current is sufficient to charge or discharge the cell within a few ms.

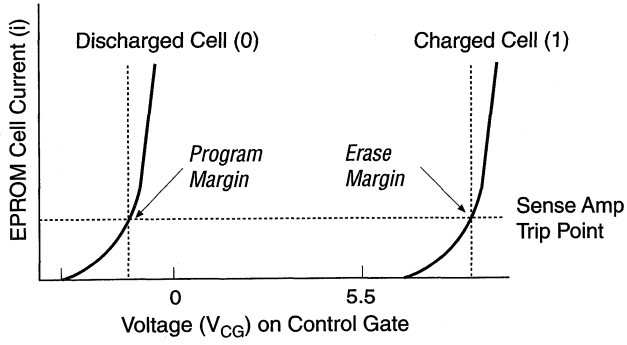
Figure 5. EEPROM Floating-Gate Electrode, Tunnel Oxide & Heavily Doped Diffusion Electrode



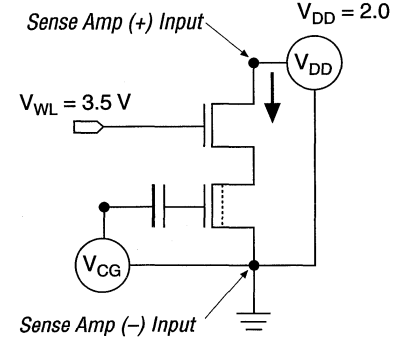
The I-V relationships for programmed and erased EEPROM cells are similar to those of EPROM cells (see Figure 6). Unlike the EPROM cell, however, the threshold voltage of a discharged EEPROM cell is negative (less than 0 V) because electrons are removed from the floating gate. Electron removal gives the floating gate a net positive charge.

Figure 6. Current vs. Voltage Relationships of Erased & Programmed EEPROM Cells

EEPROM Cell I-V Characteristics



Equivalent Circuit for Margin Testing



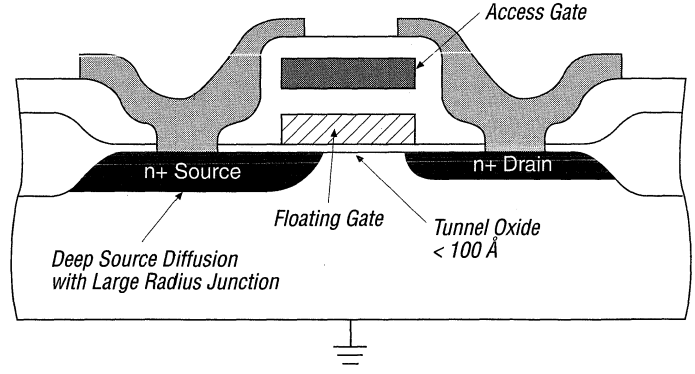
FLASH Configuration Element

The FLASH transistor, used in Altera's FLASHlogic EPX880 and EPX8160 devices, is a hybrid configuration element that combines design, manufacturing, and operational characteristics of EPROM and EEPROM configuration elements.

As shown in Figure 7, the FLASH transistor has two layers of polysilicon in a stacked gate structure that resembles the EPROM transistor. However, the transistors have different gate-oxide thicknesses and source/drain regions: the FLASH cell gate oxide is less than 100 Å thick, while the EPROM gate oxide is approximately 200 Å thick.

The source and drain diffusions of a FLASH cell are asymmetric; the source has a higher diffusion coefficient than the drain. The source-to-gate overlap is greater than the drain-to-gate overlap, causing a graded diffusion with a higher junction breakdown voltage. In contrast, the EPROM transistor has symmetric source and drain diffusions.

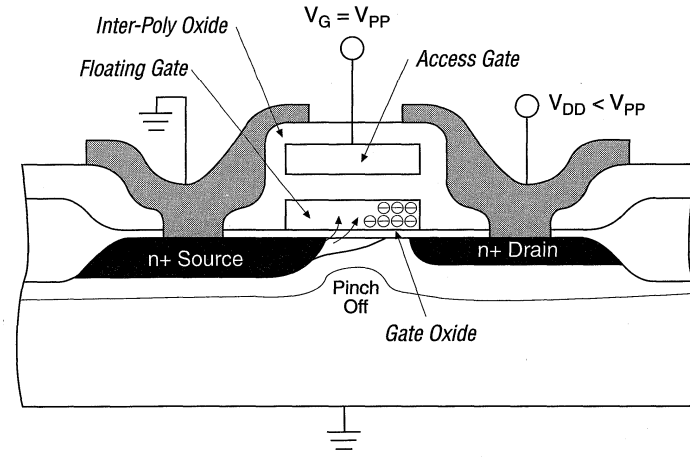
Figure 7. FLASH Configuration Element Construction



A tungsten film overlays the access gate, effectively reducing the resistivity of the second polysilicon layer and improving the performance of the device. The tungsten film does not alter FLASH cell operation.

FLASH transistors, like EPROM transistors, are programmed using hot electron injection. See Figure 8. When a high programming voltage (V_{PP}) of approximately 12 V is applied to the upper access gate, it capacitively couples the access gate to the floating gate, inverting the P-type channel below the gate and turning on the cell. When a lower voltage (V_{DD}) of 5 to 8 V is applied to the drain, it causes a large source-to-drain current, resulting in electron acceleration from the source to the drain.

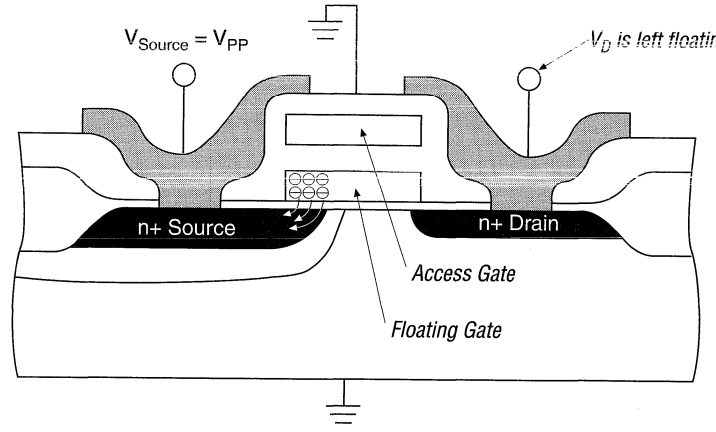
Figure 8. FLASH Configuration Element Charging Operation via Hot Electron Injection



An electric field, generated by the coupled access and floating gates, diverts the flow of electrons towards the gate oxide. Diverted electrons with energy greater than 3.2 eV jump through the gate oxide and are trapped on the polysilicon floating gate. When the programming voltages are removed, the electrons trapped on the floating gate raise the threshold voltage above 5.5 V, turning off the cell.

To erase the FLASH transistor, the excess electrons are removed from the floating polysilicon gate with Fowler-Nordheim tunneling, the same method used to erase EEPROM cells. The access gate is grounded, effectively grounding the floating gate, and a high programming voltage (V_{PP}) is applied to the source junction. As shown in Figure 9, this process applies a high field across the tunnel oxide between the floating gate and the graded source junction. The field, approximately 12×106 V/cm, produces a tunnel current of electrons between the floating gate and the source that discharges the cell.

Figure 9. FLASH Configuration Element Discharging Operation via Fowler-Nordheim Tunneling

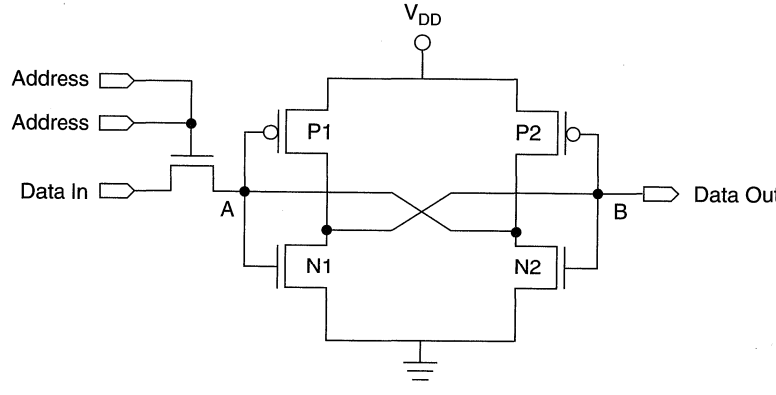


SRAM Configuration Element

The basic programming element of Altera's FLEX 8000 programmable logic devices are SRAM configuration elements. Figure 10 shows the standard CMOS five-transistor cell that comprises the configuration element.

The FLEX 8000 device manufacturing process is a subset of the EEPROM fabrication process. Therefore, all development and reliability enhancements used to manufacture EEPROM devices also apply to SRAM-based devices.

Figure 10. SRAM Configuration Element



Failure Mechanisms & Reliability Screens

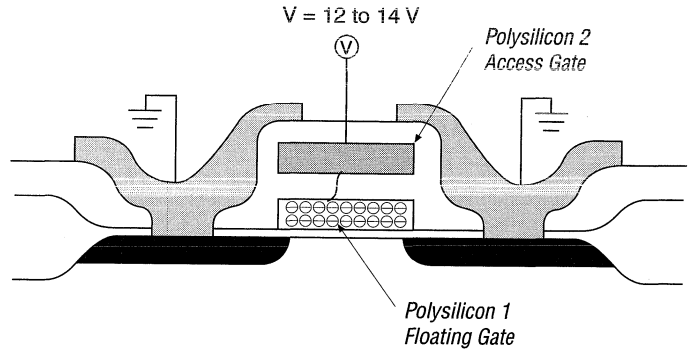
EPROM, EEPROM, and FLASH cells function through a change in threshold voltage. Reliable EPROM, EEPROM, and FLASH cells hold excess electrons placed on the floating gate, thus maintaining their charge and a high-threshold voltage (transistor off) over the expected life of the device. Discharged cells maintain a low-threshold voltage (transistor on), preventing electrons from moving onto the floating gate over the life of the device.

Voltage Margin Testing

Voltage margin testing is used to measure the threshold voltage of EPROM, EEPROM, or FLASH cells. This testing is essential for monitoring the ability of a device to be programmed or erased, and the long-term stability of a device after programming or erasure. Altera devices incorporate special test-mode circuitry that allows measurement of the threshold voltage (i.e., voltage margin) of each EPROM, EEPROM, or FLASH cell on a device. This circuitry is used to determine the programmability of all devices and to implement screens that detect charge loss from programmed devices. During the screening process, any degradation of the threshold voltage is measured for each cell as a function of time, temperature, and voltage. Voltage margin testing does not apply to SRAM cells because they are configured at system power-up by a Configuration EPROM or an external host.

Altera's voltage margin testing is performed during wafer-sort operations. At Wafer Sort 1, devices are tested for combinatorial and registered logic functionality and for cell programming, to ensure that all EPROM, EEPROM, or FLASH cells are fully programmable. Each cell is "voltage-margined" to ensure that its threshold voltage exceeds 5.5 V, the maximum V_{CC} value encountered during normal operation. Next, each cell's access gate is raised to 12 V to pull electrons off the floating gate through any defects in the inter-poly oxide between the floating and access gates. See Figure 11.

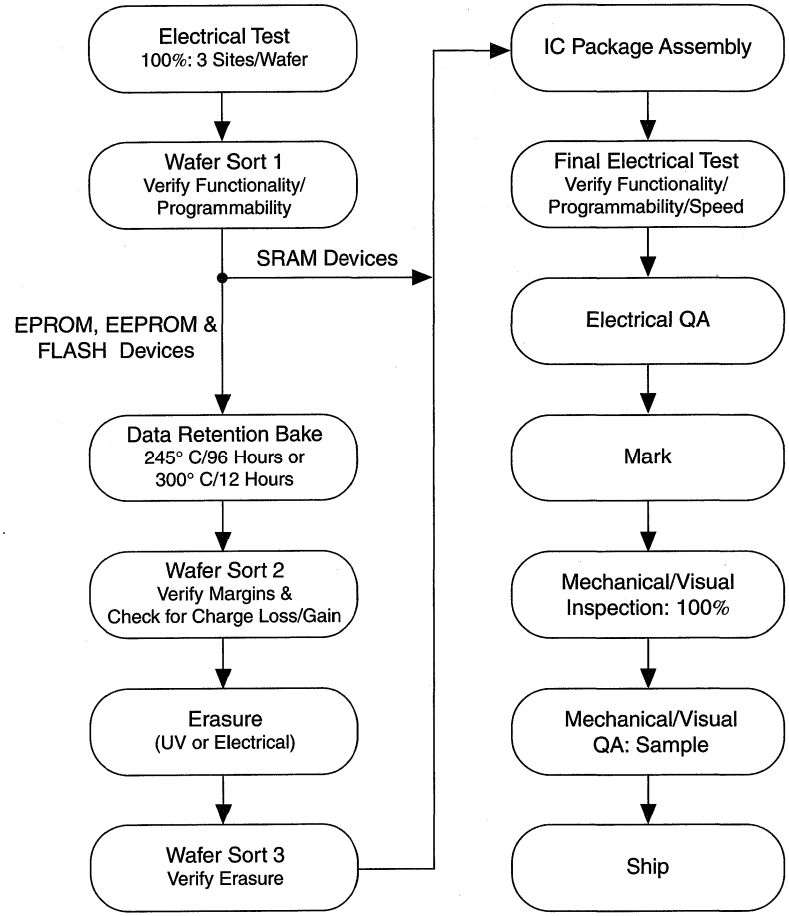
Figure 11. DC Erase Stress for EPROM, EEPROM & FLASH Configuration Elements



As shown in Figures 1, 4, and 7, the floating gate in all cells is completely surrounded by oxide. Any defect in the oxide, or contamination by mobile ionic charges such as Na^+, can cause electrons to migrate off the gate. This "cell stress," or DC erase stress, lowers the threshold voltage of cells with a defective oxide. A cell's base threshold voltage is determined by a voltage margin test performed immediately after programming and before the DC erase stress. After the DC erase stress is applied, each cell's voltage margin is tested again. If any cell shows a significant reduction in threshold voltage, the device is rejected from the manufacturing flow.

Thermally activated charge-loss mechanisms are also reliability hazards. To detect material defects, every device is baked at a high temperature with all cells in the charged state after Wafer Sort 1. Depending on the device, this bake is performed at 300° C for 12 hours or 245° C for 96 hours. After the bake, the threshold voltage for each cell is remeasured during Wafer Sort 2 and compared to its pre-bake value. Devices with cells that exhibit a reduced threshold voltage are rejected from the manufacturing flow. Additional voltage margin testing is performed on packaged devices after assembly. Figure 12 shows a typical wafer-sort process.

Figure 12. Wafer-Sort, Assembly & Final Test Flow for Altera Devices



Reliability Screening

Reliability testing is an integral part of the standard production test flow for all Altera devices. During the various wafer-sort operations, devices are screened for reliability. Voltage- and temperature-accelerated stresses are applied to activate potential charge-loss failure mechanisms within the device. To ensure the effectiveness of Altera's testing program, test results are routinely verified.

After the IC package assembly operation, during which the individual dice are removed from the wafers and placed into packages, each device is tested and the results are compared against data sheet specifications. The test is performed at elevated temperatures to ensure that specifications are met for the maximum guaranteed operating temperature: 70° C for commercial, 85° C for industrial, and 125° C for military devices.

Altera Reliability Program

Altera's integrated circuits must meet rigorous reliability standards. Altera uses a two-phase approach to ensure a consistently high level of reliability from its manufacturing processes and devices:

- New product/production process qualification
- Reliability monitoring

New Product/Production Process Qualification

Altera performs rigorous reliability tests on new devices and subjects new or substantially modified processes to a rigorous series of reliability tests before production. Tests are performed to Altera, industry, and MIL-STD-883 (rev. C) standards. This qualification procedure ensures that all manufacturing processes and products meet Altera's minimum reliability requirements. Tables 1 and 2 summarize the reliability tests for ceramic and plastic package devices, respectively.

Table 1. Ceramic Package Qualification Requirements

Sequence	Test	MIL-STD-883 (Rev. C) Method	Goal LTPD, *Note (1)*	Sample Size	Rejects Allowed	Requirements: Assembly Plant	New Leadframe	New Package	New Lead Finish	Wafer Fabrication Process	Full Qualification
	ESD sensitivity	3015.7	–	4	0					✓	✓
	Latch-up		–	5	0					✓	✓
	Retention bake		5	77	1					✓	✓
B2	Mark permanency	2015	–	4	0	✓	✓		✓		✓
B3	Solderability	2003	10	22	0	✓	✓	✓	✓		✓
B5	Bond strength	2011	15	15	0	✓	✓	✓			✓
C1	Lifetest 1,000/2,000 hours	1005 (125° C)	5	77	1					✓	✓
D1	Physical dimensions	2016	15	0	0	✓	✓	✓			✓
D2	Lead fatigue	2004 B2	15	15	0	✓	✓	✓	✓		✓
	Fine & gross leak	1014									
D3	Thermal shock	1011.7 B	5	77	1	✓	✓	✓		✓	✓
	Temperature cycle	1010.7 C									
	Moisture resistance										
	Fine & gross leak	1014									
	External visual	1004									
	End point electrical	Altera									
D4	Mechanical shock	2002 B	15	15	0	✓	✓		✓		✓
	Vibration variable	2007 A									
	Frequency										
	Constant acceleration	2001 E (30 kg)									
	Fine & gross leak	1014									
	External visual										
	End point electrical	Altera									
D4	Internal water vapor	1018 (5000 ppm maximum)	–	3/5	0/1	✓	✓	✓	✓	✓	✓
D8	Lid torque	2024	–	15	0	✓	✓	✓	✓		✓

Note:
(1) LTPD: Lot tolerance percent defective

Table 2. Plastic Package Qualification Requirements

Sequence		Test	MIL-STD-883 (Rev. C) Method			Requirements						
			Goal LTPD, Note (1)	Sample Size	Rejects Allowed	Assembly Plant	New Package	New Leadframe	New Lead Finish	Wafer Fabrication Process	New Molding Compound	Full Qualification
B1	Physical dimension	2016	–	2	0	✓	✓	✓			✓	✓
B2	Mark permanency	2015	–	4	0	✓	✓		✓		✓	✓
B3	Solderability	2003	10	22	0	✓	✓	✓	✓		✓	✓
B4	Autoclave 121° C/100% rh 15 psi, unbiased: 168 hours		5	77	1	✓	✓	✓	✓	✓	✓	✓
B5	Bond strength	2011	15	15	0	✓	✓	✓			✓	✓
C1	Lifetest 1,000/2,000 hours	1005 (125° C)	5	77	1	✓	✓			✓	✓	✓
C2	85/85 with bias: 1,000 hours	85° C/85% relative humidity	5	77	1					✓	✓	✓
D1	Lead integrity	2004.5	15	15	0	✓	✓	✓			✓	✓
D2	Resistance to solder heat: 260° C for 10 seconds		10	22	0	✓	✓	✓	✓		✓	✓
D3	Thermal shock –55° C to +125° C, 100 cycles	1011.7 B	5	77	1	✓	✓	✓		✓	✓	✓
D4	Temperature cycle –55° C to +125° C, 1,000 cycles	1010.7 B	5	77	1	✓	✓	✓	✓	✓	✓	✓

Note:
(1) LTPD: Lot tolerance percent defective

Reliability Monitoring

Once a device or process is qualified for production, Altera routinely conducts reliability tests throughout its manufacturing life cycle. Reliability tests are conducted under the careful supervision of trained reliability engineers and technicians, and are performed to Altera, industry, and MIL-STD-883 (rev. C) standards. Table 3 describes the reliability tests and shows how often they are performed.

Table 3. Reliability Test Program

Test Type	MIL-STD-883 (Rev. C) Method/Condition	Test Frequency	Plastic Package	Hermetic Package
Life test	2,000 hours at 125° C at rated voltages	1 time per month per process	✓	✓
Data retention bake	1,000 hours (minimum) at 170° C	1 time per month per process	✓	✓
Temperature cycling	1,000 cycles 1010.7; condition C –55° C to +150° C (plastic) –65° C to +150° C (ceramic)	1 time per month per process	✓	✓
Thermal shock	1011.7; condition B –55° C to +125° C	2 times per year per package	✓	✓
Constant acceleration	2001E; 30,000 G force; Y1 only	2 times per year per package	–	✓
Mechanical shock	2002B; 1500G force; 0.5-ms pulse peak	2 times per year per package	–	✓
Lid torque	2024	1 time per month per package	–	✓
Lead integrity	2004 B2	2 times per year per package	✓	✓
Internal water vapor content	1018; 5000 ppm maximum at 100° C	1 time per month per package	–	✓
Temperature/humidity/bias	85° C/85% relative humidity; 5 V; 1,000 hours minimum	1 time per month per package	✓	–
Autoclave (pressure cooker)	121° C; 2 atm; 96 hours minimum	1 time per month per package	✓	–

Altera's Reliability Engineering Lab uses the latest equipment for reliability testing, allowing Altera engineers and technicians to perform accurate reliability qualifications and monitoring on a timely basis. This equipment provides engineers and technicians with the control and precision required to perform rigorous semiconductor stress tests.

Results from Altera's reliability monitoring program are published several times each year in the *Altera Reliability Report*. This report summarizes the test results for all Altera devices over a 15-month period. It includes detailed descriptions of the reliability tests, their implementation, and useful information about semiconductor reliability. For a copy of the *Altera Reliability Report*, contact the Altera Literature Department at (408) 894-7144.

Notes:

QFP Carrier & Development Socket

March 1995, ver. 7

Data Sheet

Features

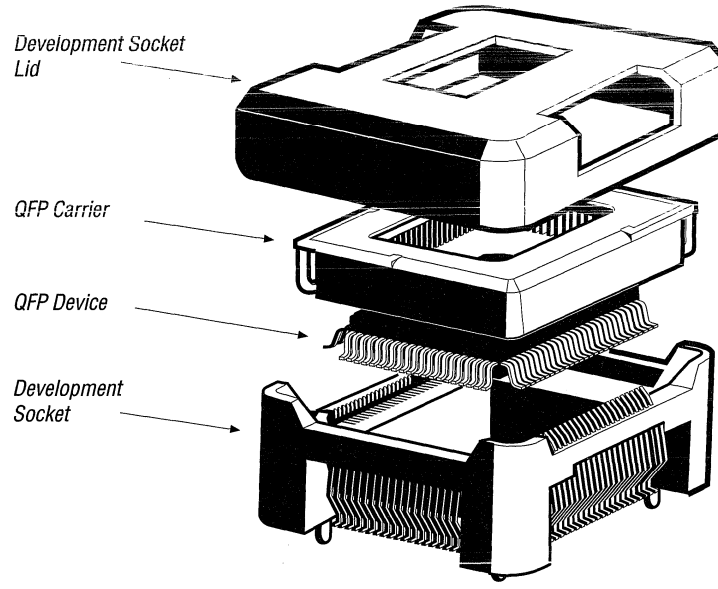
- Quad flat pack (QFP) carriers protect fragile leads on Altera QFP devices during shipping and device handling.
- Development sockets allow on-board electrical and mechanical prototype testing with QFP packages.
- Carriers and sockets are available for 100-, 160-, 208-, 240-, and 304-pin devices.
- Development socket footprints are compatible with QFP footprints, providing a smooth transition from prototype to production.

General Description

The Altera QFP carrier and development socket protect the fragile leads on QFP devices during shipping and throughout the development cycle. The socket has a lead footprint that is compatible with the device, so it can be used during both mechanical and electrical prototyping.

The material used in the carrier and development socket helps prevent electrostatic damage to the devices while providing excellent AC circuit performance. QFP carriers and development sockets are currently available for 100-, 160-, 208-, 240-, and 304-pin QFP packages. Figure 1 shows the 100-pin QFP carrier and development socket.

Figure 1. 100-Pin QFP Carrier & Development Socket



QFP Carrier

The carrier is a static-dissipative, molded plastic shell that holds the device and leads in a secure frame to prevent mechanical damage. The device is held in the carrier by recessed plastic clips (2 clips on the 100-pin carrier and 4 clips on the 160-, 208-, 240-, and 304-pin carriers).

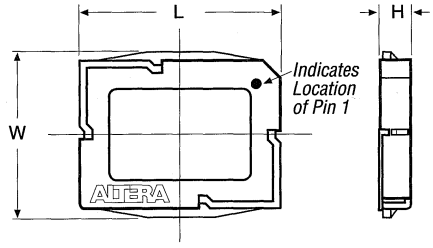
All MAX 9000, MAX 7000, and MAX 5000 devices with 100 to 304 pins can be ordered in carriers, thus eliminating the need to handle the delicate device leads. The device and carrier are packaged either in antistatic rails or strip packs. Devices can be programmed and erased while in the carrier. EPROM-based QFP devices are erased with a UV lamp; EEPROM-based QFP devices are erased in the programming adapter. Figure 2 shows the dimensions of the QFP carriers.

QFP devices without protective carriers should be handled with a vacuum wand in an electrostatically protected workplace to reduce the possibility of mechanical or electrical device damage.

Figure 2. QFP Carrier Dimensions

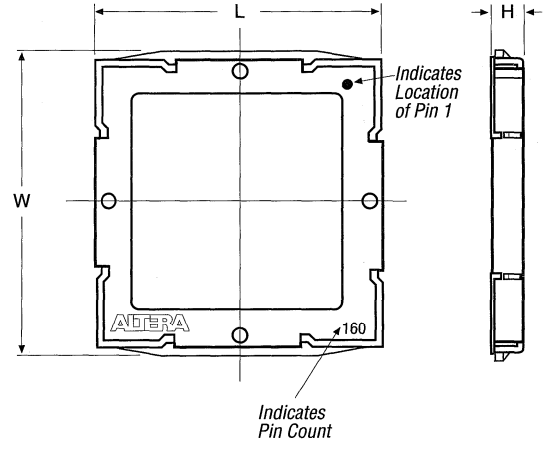
Dimensions are shown in millimeters. The carrier is rated from –65° C to 155° C, and is qualified to handle commercial, industrial, and military operating temperatures.

100-Pin QFP Carrier



Pin Count	L	W	H
100	25.2	21.2	4.2
160	33.2	35.2	5.1
208	33.2	35.2	5.1
240	C. F.	C. F.	C. F.
304	45	48	6.3

160-, 208-, 240- & 304-Pin QFP Carrier



QFP Development Socket

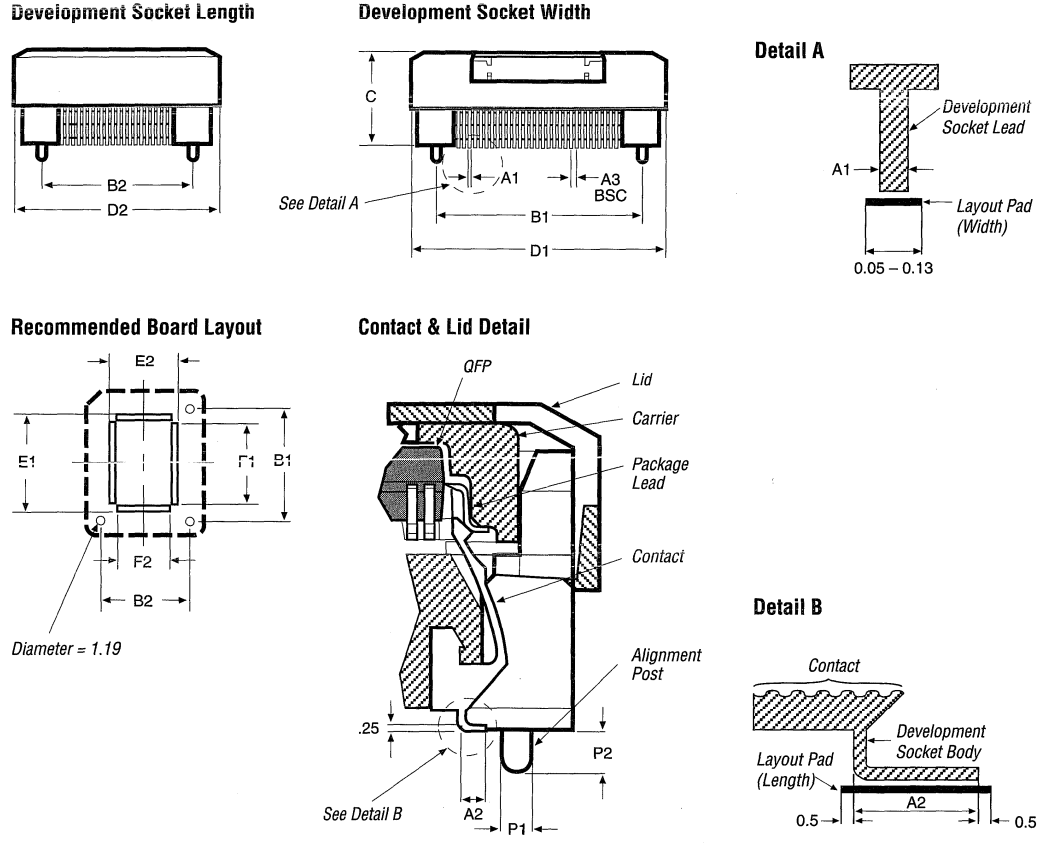
The QFP development socket footprint is compatible with the lead footprint of the QFP device. It ensures the device's electrical connection to the PCB and provides excellent AC circuit performance: low noise, low capacitance, and low inductance. A device mounted directly on the PCB will provide better interconnect capacitance and inductance than a device loaded into the carrier/socket.

Figure 3 shows the dimensions of the QFP development socket. Details A and B show the PCB pad layout length and width recommended for use with the development socket. These industry-standard pad layout dimensions are for the "gull wing" lead that is typically found on QFP packages. The layout pad extends from 0.05 mm to 0.13 mm beyond each side of the lead width (A1), and 0.5 mm beyond each side of the lead length (A2), as shown in Details A and B, respectively. A layout pad of these dimensions is also suitable for use with QFP devices that do not use carriers.

To ensure correct board layout, pad sizes must be compatible with the development socket and the QFP device leads.

Figure 3. QFP Development Socket Dimensions

Dimensions are shown in millimeters. The tolerance of all layout pad dimensions is ±0.025 mm. The carrier lid, carrier base, and socket are qualified to handle commercial, industrial, and military operating temperatures. The lid is rated from –10° C to 155° C, and the base is rated from –65° C to 155° C.



Pin Count	A1	A2	A3	B1	B2	C	D1	D2	E1	E2	F1	F2	P1	P2
100	0.20	0.93	0.65	25.00	19.00	12.00	31.51	25.54	23.63	17.63	18.85	12.35	1.00	1.50
160	0.20	0.93	0.65	33.80	33.80	12.80	39.80	39.80	32.08	32.08	25.35	25.35	1.00	1.50
208	0.20	0.93	0.50	33.80	33.80	12.80	39.80	39.80	31.68	31.68	25.50	25.50	1.00	1.50
240, *(1)*	C. F.	C. F.	C. F.	C. F.	C. F.	C. F.	C. F.	C. F.	C. F.	C. F.	C. F.	C. F.	C. F.	C. F.
304, *(1)*	C. F.	C. F.	C. F.	C. F.	C. F.	C. F.	C. F.	C. F.	C. F.	C. F.	C. F.	C. F.	C. F.	C. F.
Tolerance	±0.12	±0.12	±0.12	±0.12	±0.12	±0.40	±0.20	±0.20	±0.12	±0.12	±0.12	±0.12	±0.12	±0.12

Note:
(1) C.F. = consult factory.

The development socket body is designed to withstand the temperatures required by industry-standard solder reflow technology. Soldering times should not exceed 30 seconds at 260° C. Altera recommends using 100% forced convection reflow ovens rather than IR reflow ovens to perform reflow operations. The large thermal mass of the development socket shields or "shadows" the solder paste from the infrared radiation used in IR reflow ovens. Shadowing prevents the adequate heating and flow of the paste, causing inadequate lead contact with the circuit board and unacceptable solder joints. 100% forced convection reflow ovens provide the even and efficient heat transfer required to form an acceptable solder joint.

The development socket lid and the QFP carrier should not be subjected to the solder reflow process. They cannot withstand the typical reflow temperatures of 180° C to 260° C, and can be harmed by cleaners and solvents used in the reflow process. Only the development socket base should be subjected to solder reflow. The carrier and lid are qualified to handle commercial, industrial, and military operating temperatures.

With the appropriate solder mask, multiple development sockets can be closely spaced on the board. Three alignment posts ensure correct orientation and provide sufficient registration for reflow soldering. When other components must be placed near the development socket, the designer must ensure that component leads do not conflict with the outline of the development socket.

The QFP carrier is held in the development socket by the socket lid, which braces the carrier against the electrical contacts in the socket. These contacts connect the device leads to the development socket, ensuring a positive electrical connection that is not susceptible to mechanical interruption through jarring or impulsive shocks. The carrier design ensures that the pressure of the socket contacts does not significantly affect the coplanarity of the device leads. This carrier/socket combination allows the designer to perform mechanical analysis during the functional prototyping cycle.

Altera also provides a tool to extract the QFP device from the carrier. Although it is possible to extract a QFP device from the carrier without the tool, Altera recommends using the tool for QFP devices with 160 or more pins. See "Extracting a Device from the QFP Carrier with the Extraction Tool" on page 594 of this data sheet for complete details.

Step-by-Step Instructions

The following instructions apply to Altera's 160- and 208-pin development sockets. For 240- and 304-pin development socket instructions, contact Altera Marketing at (408) 894-7104.

This section gives step-by-step instructions for the following procedures:

- Inserting the QFP carrier into the development socket
- Removing the QFP carrier from the development socket
- Programming a device in the QFP carrier
- Extracting a device from the QFP carrier without the extraction tool
- Extracting a device from the QFP carrier with the extraction tool
- Inserting a device into the QFP carrier

☞ The device should be removed from the QFP carrier only after it has been programmed and is ready to be soldered onto the PCB.

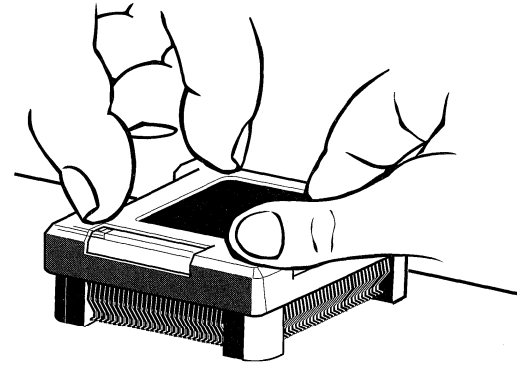
Inserting the QFP Carrier into the Development Socket

To insert the QFP carrier into the development socket:

1. Align the QFP carrier on the development socket by matching the beveled corner of the carrier to the beveled corner of the socket and aligning the corresponding dots.

2. Place the socket lid over the socket and press down firmly on all four corners of the lid. Clicking sounds are clearly audible as the socket lid is pressed into place. See Figure 4.

Figure 4. Inserting the QFP Carrier into the Development Socket



When placing the lid onto the development socket, Altera recommends bracing the side of the board opposite the development socket to prevent the board from flexing. A fair amount of insertion force is required to seat a high-pin-count device. If the board is not properly braced, repeated flexing of the board can cause excessive wear and cracks in the solder joints and in the traces of the board.

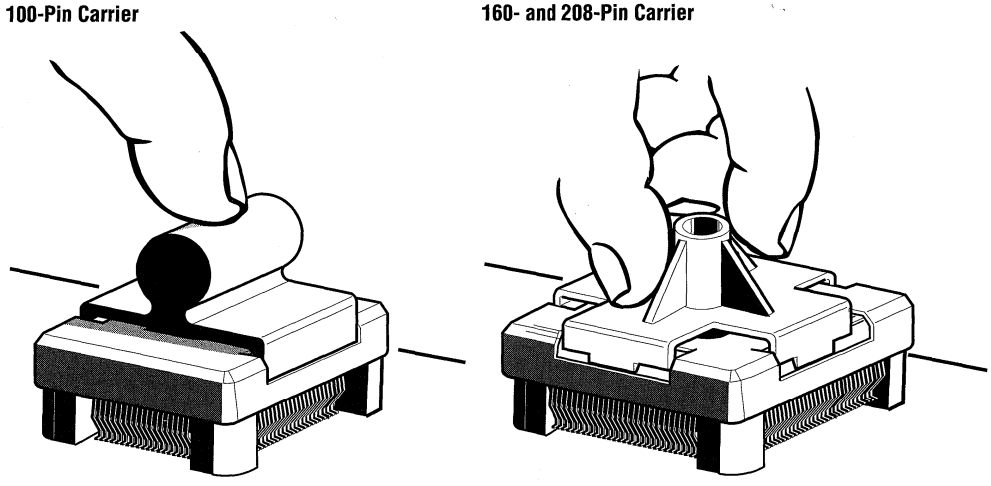
Removing the QFP Carrier from the Development Socket

To remove the QFP carrier from the development socket:

1. Place the removal tool over the QFP socket lid, as shown in Figure 5.
2. Gently press down, making sure that the edges of the tool fit into the slots on the top of the lid. Clicking sounds will be clearly audible.
3. While maintaining pressure, lift the lid and removal tool together.
4. Remove the carrier.

- To ensure that all four tabs of the 160- and 208-pin carrier have been unlatched from the base of the development socket, twist the removal tool back and forth after it is pressed down.
- Altera recommends inserting a carrier into a development socket no more than 25 times.

Figure 5. Removing the QFP Carrier from the Development Socket



Programming a Device in the QFP Carrier

QFP devices that are shipped in the protective QFP carriers are ready to be programmed with the Altera Master Programming Unit (MPU) and the appropriate PLM-prefix programming adapter. With Altera programming software and hardware, test vectors can be directly applied to the device for programming verification and functional testing. Devices in QFP packages can also be programmed with industry-standard programming hardware from other manufacturers.

To program a device in the QFP carrier:

1. Place the QFP carrier with the device into the programming adapter, making sure that carrier and adapter are aligned correctly.
2. Close the retaining latch by pressing the latch against the socket. A clicking sound is clearly audible as the latch fastens over the socket.

☞ The retaining latch on the clamshell-style programming adapter socket ensures good electrical contact between the device leads and the socket. The retaining latch must be shut after the QFP carrier is placed into the programming adapter to ensure proper programming.

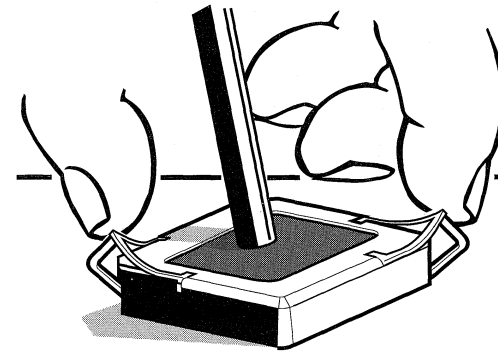
Extracting a Device from the QFP Carrier without the Extraction Tool

To extract a device from the QFP carrier without the extraction tool:

1. Place the QFP carrier against a flat surface.
2. Without applying pressure, hold down the device with the blunt end of a pencil or another similar tool.
3. Bend up the yellow retaining clips located on diagonal corners of the QFP carrier. See Figure 6.

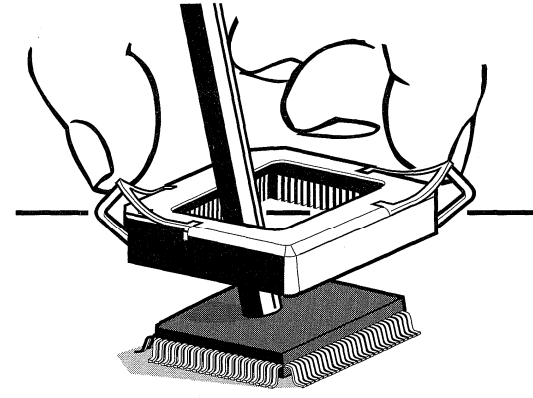
Figure 6. Bending the Retaining Clips to Extract the QFP Device from the QFP Carrier

The clips will remain bent when lifted.



4. Lift the QFP carrier straight up. See Figure 7.

Figure 7. Lifting the QFP Carrier to Extract the QFP Device



5. Use a vacuum wand to move the exposed device.

☞ Altera recommends using the extraction tool to extract QFP devices with 160 or more pins from QFP carriers.

Extracting a Device from the QFP Carrier with the Extraction Tool

Altera produces several extraction tools for 100-, 160-, 208-, 240-, and 304-pin devices. See *Ordering Information* in this data book for more information. The QFP device fits in the QFP carrier extraction tool only when it is correctly oriented in the insertion slot. The pin indicator on the corner of 160- and 208-pin QFP devices, shown in Figure 2, should be aligned with the beveled corner of the extraction tool. A sliding platform slips over the QFP device, securing it in the slot and bending back the yellow retaining clips located on adjacent corners of the QFP carrier. The extraction button ejects the QFP device from the carrier and places the device directly onto a QFP handling tray as shown in Figure 8, or onto a catch plate, which is included with the extraction tool. The catch plate included with the extraction tool for 100-pin devices holds four devices; the catch plate included with the extraction tool for 160- and 208-pin devices holds two devices. For information on 240- and 304-pin extraction tools, contact Altera Marketing.

The bottom of the extraction tool contains ridges that align it with the sides of the handling tray or catch plate. The default size of the extraction tool supports the Peak Plastic Corporation low-profile JEDEC tray. Table 1 provides part numbers for these trays.

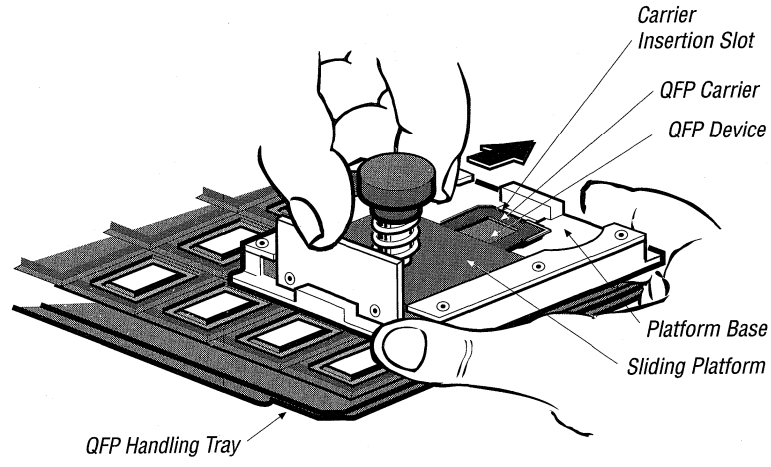
Table 1. QFP Handling Tray Part Numbers

Pin Count	Peak Part Number
100	ND-1420-2.7-0811-8
160	ND-2828-3.5-0308-8
208	ND-2828-3.5-0308-8

To extract a QFP device from the carrier using the extraction tool:

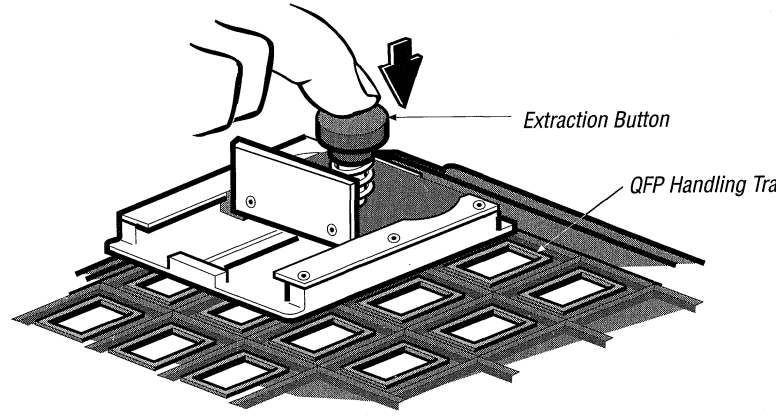
1. Place the tool over an empty slot of the QFP handling tray. Line up the ridges on the bottom of the extraction tool with the sides of the empty slot. To ensure proper device orientation, align the beveled corner of the extraction tool with the beveled corner of the QFP tray. If a handling tray is not available, place the extraction tool over the catch plate provided.
2. Open the extraction tool by moving the sliding platform until the carrier insertion slot is completely exposed.
3. Place the carrier-protected QFP device into the carrier insertion slot. Align the beveled edge of the carrier with the beveled edge of the insertion slot, and make sure that the carrier is flush with the platform base.
4. Move the sliding platform until it completely covers the QFP device. See Figure 8.

Figure 8. Placing the QFP Carrier in the Extraction Tool



5. With the QFP device completely covered, press down on the extraction button to release the QFP device from the carrier and place it in the QFP handling tray or on the catch plate. If a handling tray is not available, use a vacuum wand or other handling device to move the QFP device. See Figure 9.

Figure 9. Pressing on the Extraction Button to Remove the QFP Device



☞ A multi-device extraction tool is available for use in production environments. This tool extracts up to six QFP devices at a time and can be used with both high- and low-profile JEDEC trays. Contact Altera Applications at (800) 800-EPLD for more information.

Inserting a Device into the QFP Carrier

To insert a QFP device into the QFP carrier:

1. Hold the carrier bottom-side up.
2. With thumb and forefinger, bend the yellow retaining clips outward.
3. Place the device into the carrier so that the device leads fit into the molded channels. The beveled corner of the device must be aligned with the beveled corner of the QFP carrier. When the device is securely seated in the carrier, the clips will snap back over the corners of the device and hold it in place.

The yellow plastic clips hold the device securely in place without hindering access to the leads. The open carrier top allows EPROM-based QFP devices to be placed under a UV lamp for device erasure.

☞ Altera does not recommend re-inserting the QFP device into the QFP carrier once it has been removed.

Altera Device Package Outlines

March 1995, ver. 5 Data Sheet

Introduction

This data sheet provides package outlines for all Altera devices. Package outlines are listed here in ascending pin count order. Table 1 summarizes the maximum lead coplanarity for Altera J-lead and QFP packages:

Table 1. Maximum Lead Coplanarity for J-Lead & QFP Packages

Package	Maximum Lead Coplanarity
Ceramic J-lead packages	0.006 inches (0.15 mm)
Plastic J-lead packages	0.004 inches (0.10 mm)
QFP packages with 160 pins or fewer	0.004 inches (0.10 mm)
QFP packages with 208 pins or greater	0.003 inches (0.075 mm)

For information on device package ordering codes, see *Ordering Information* in this data book. Package outline dimensions are shown in the following formats:

min. inches (min. millimeters)
max. inches (max. millimeters)

or:

nominal inches ± tolerance
(nominal millimeters ± tolerance)

or:

inches
(millimeters) BSC, Min., Max., Ref., Typ., R, Dia., Sq.

Table 2 shows the available package types, lead materials, and lead finishes for Altera device packages.

Table 2. Altera Device Packages

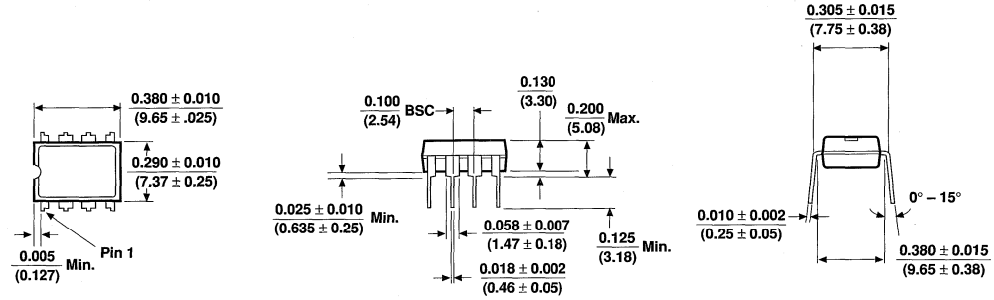
Package Type	Package Code	Lead Material	Lead Finish
Ceramic dual in-line	D	Alloy 42	Solder dip or plate
Plastic dual in-line	P	Copper	Solder dip (60/40)
Ceramic J-lead	J	Alloy 42	Solder dip (60/40)
Plastic J-lead	L	Copper	Solder plate (60/40)
Ceramic pin-grid array	G	Alloy 42	Gold over nickel plate
Plastic small-outline IC	S	Copper	Solder plate (80/20)
Ceramic quad flat pack	W	Alloy 42	Matte tin plate
Plastic quad flat pack	Q	Copper	Solder plate (80/20)
Plastic thin quad flat pack	T	Copper	Solder plate (80/20)
Power quad flat pack	R	Copper	Solder plate (80/20)
Plastic ball grid array	B	Tin-lead Alloy	n/a

Package Outlines

The following figures provide package outlines for all Altera devices.

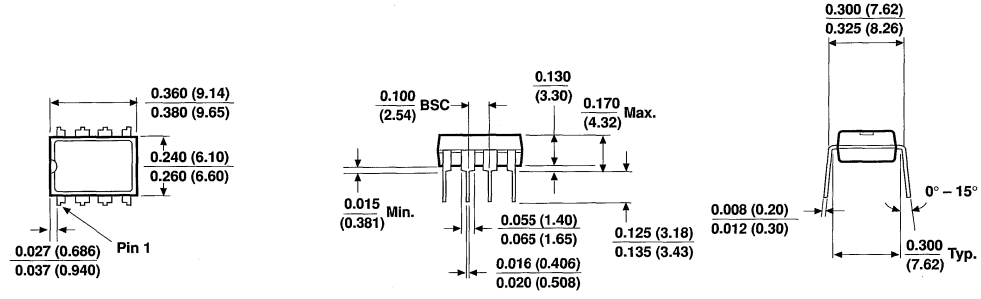
8-Pin Ceramic Dual In-Line Package (CerDIP)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Introduction" on page 597 of this data sheet for dimension formats. For military-qualified products, see case outline GDIPI-T8 in MIL-STD-1835.



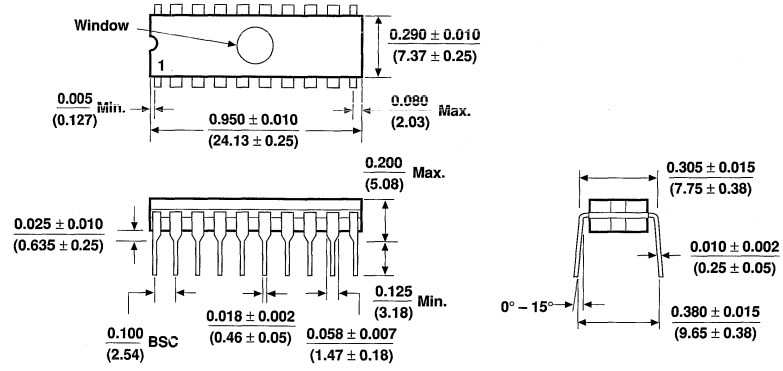
8-Pin Plastic Dual In-Line Package (PDIP)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Introduction" on page 597 of this data sheet for dimension formats.



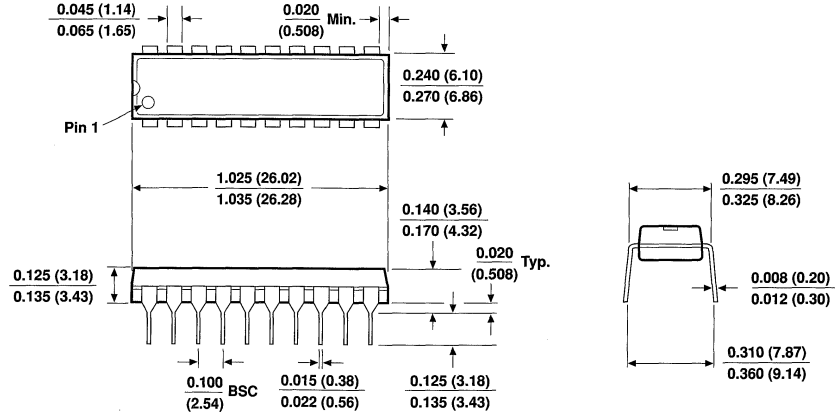
20-Pin Ceramic Dual In-Line Package (CerDIP)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Introduction" on page 597 of this data sheet for dimension formats. For military-qualified products, see case outline in MIL-STD-1835.



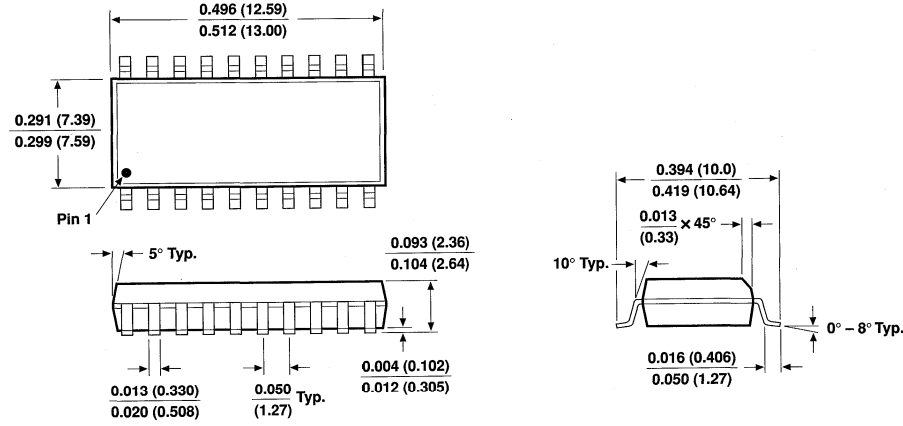
20-Pin Plastic Dual In-Line Package (PDIP)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Introduction" on page 597 of this data sheet for dimension formats.



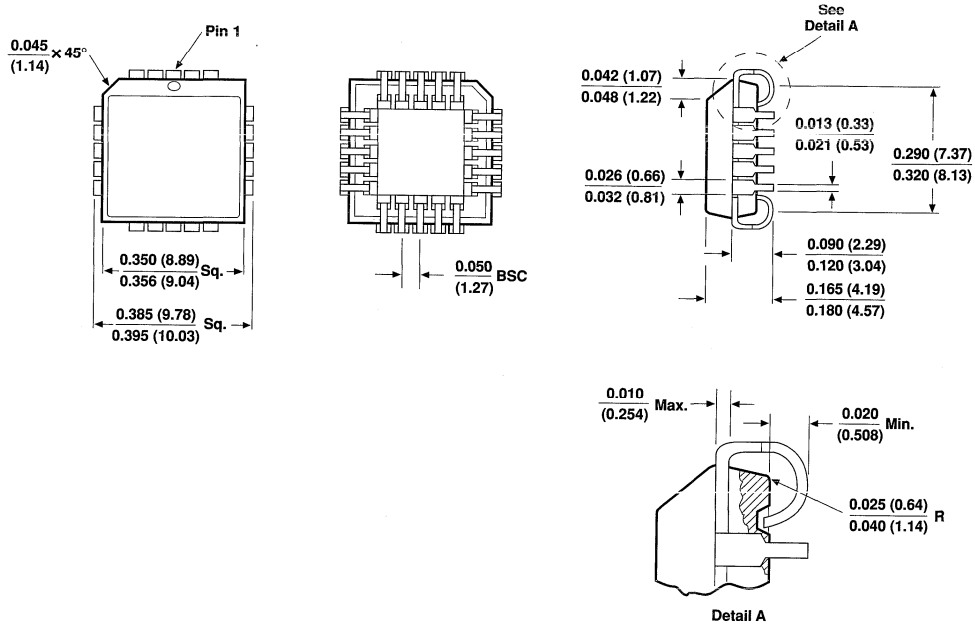
20-Pin Plastic Small-Outline Integrated Circuit (SOIC)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Introduction" on page 597 of this data sheet for dimension formats.



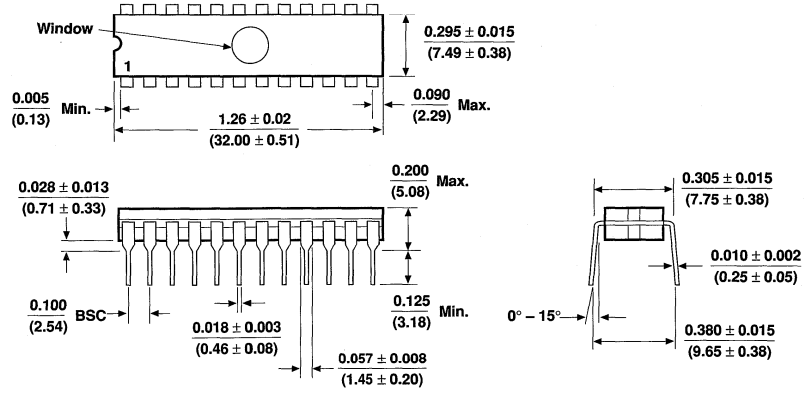
20-Pin Plastic J-Lead Chip Carrier (PLCC)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Introduction" on page 597 of this data sheet for dimension formats.



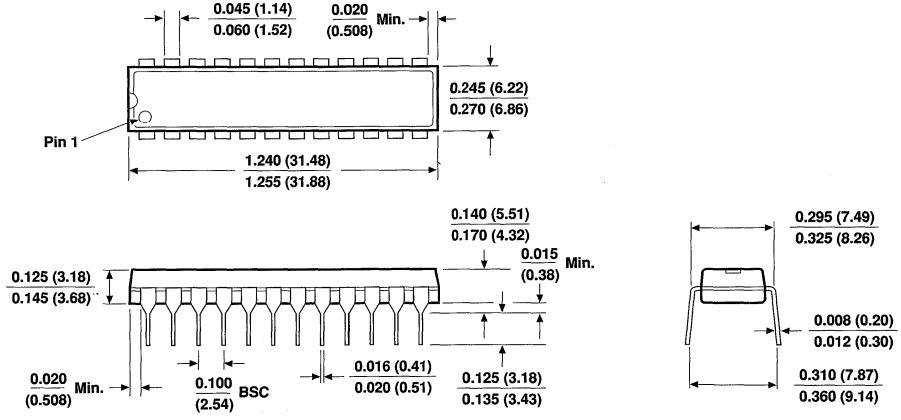
24-Pin Ceramic Dual In-Line Package (CerDIP)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Introduction" on page 597 of this data sheet for dimension formats. For military-qualified products, see case outline GDIP3-T24 in MIL-STD-1835.



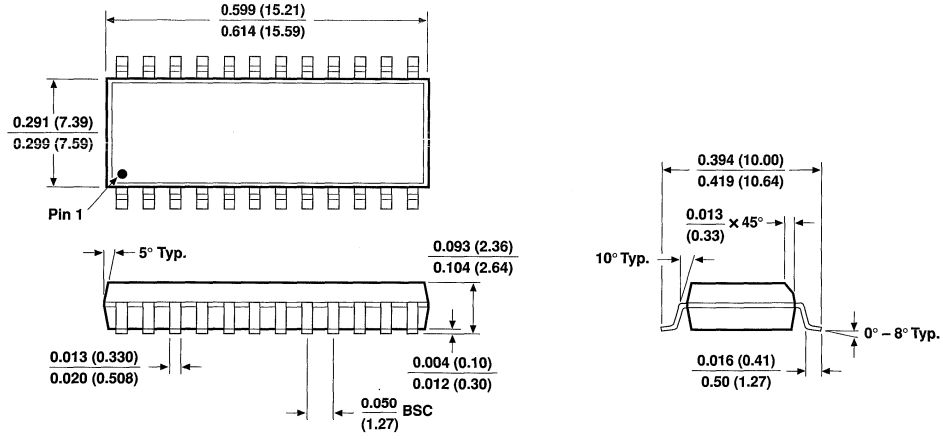
24-Pin Plastic Dual In-Line Package (PDIP)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Introduction" on page 597 of this data sheet for dimension formats.



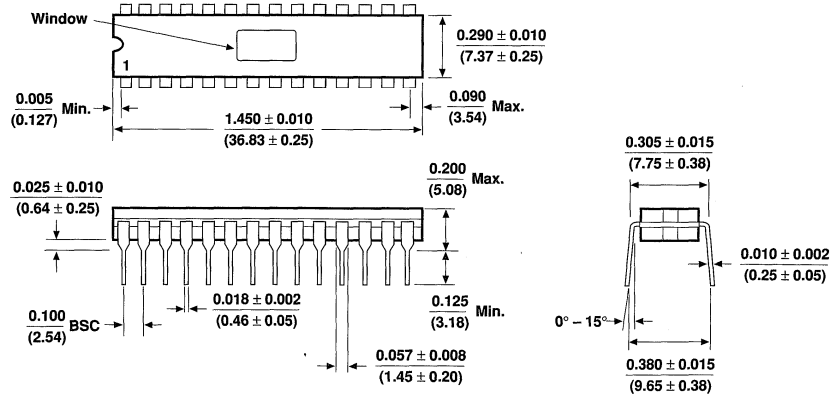
24-Pin Plastic Small-Outline Integrated Circuit (SOIC)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Introduction" on page 597 of this data sheet for dimension formats.



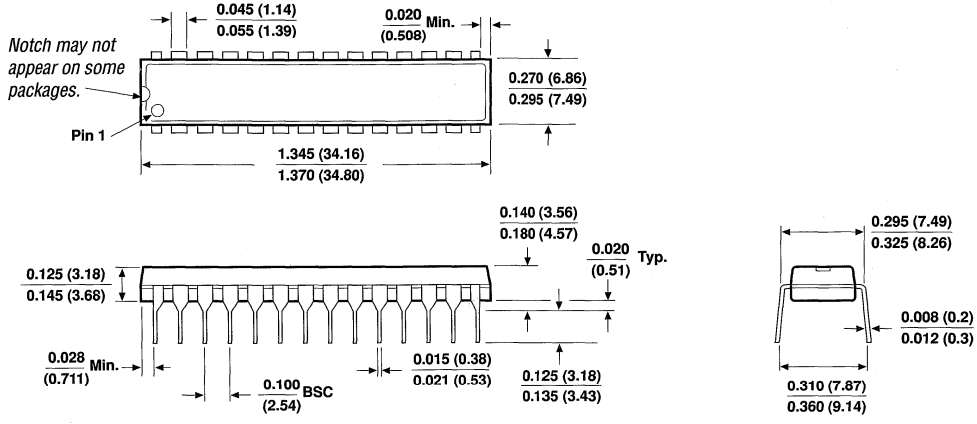
28-Pin Ceramic Dual In-Line Package (CerDIP)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Introduction" on page 597 of this data sheet for dimension formats. For military-qualified products, see case outline D-15 in MIL-STD-1835.



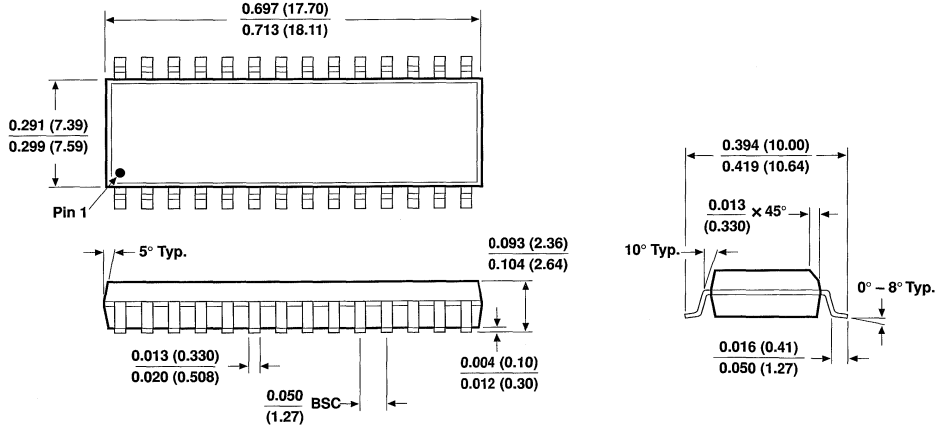
28-Pin Plastic Dual In-Line Package (PDIP)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Introduction" on page 597 of this data sheet for dimension formats.



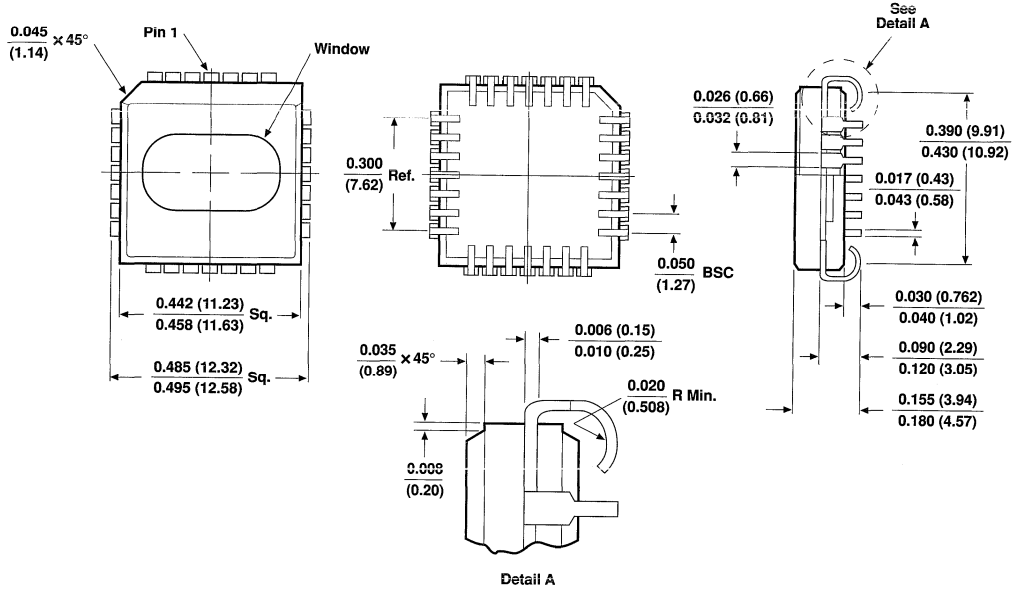
28-Pin Plastic Small-Outline Integrated Circuit (SOIC)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Introduction" on page 597 of this data sheet for dimension formats.



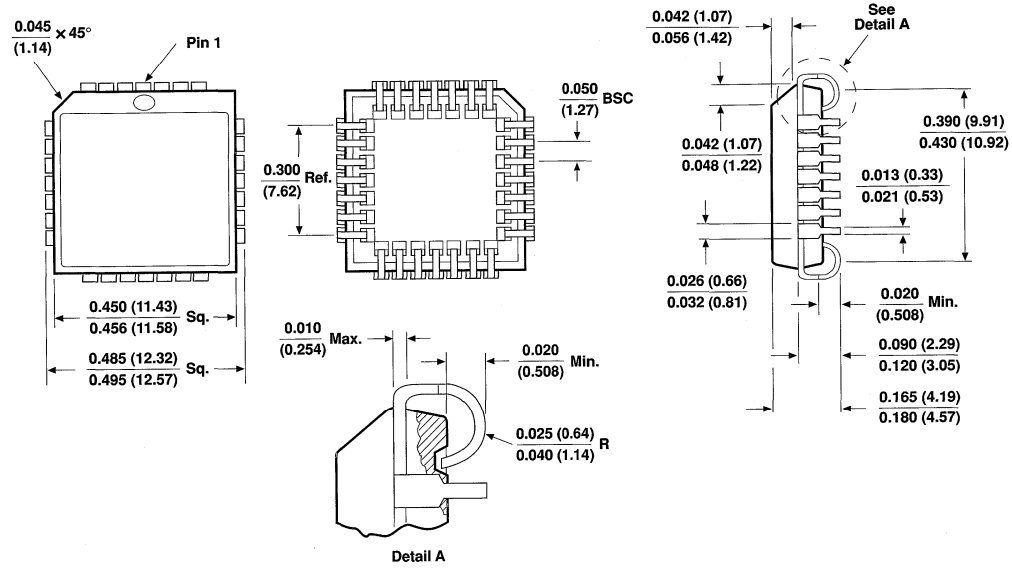
28-Pin Ceramic J-Lead Chip Carrier (JLCC)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Introduction" on page 597 of this data sheet for dimension formats. For military-qualified products, see case outline in Altera Military Product Drawing 02D-00194.



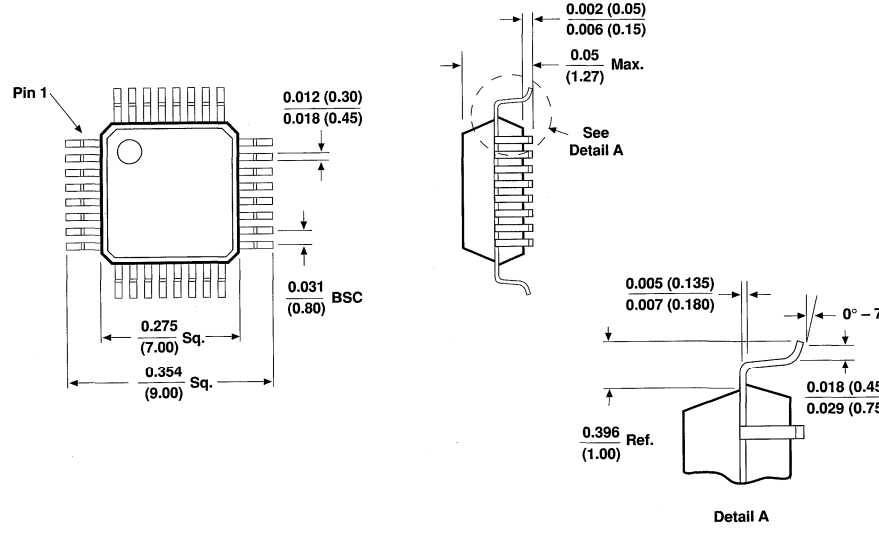
28-Pin Plastic J-Lead Chip Carrier (PLCC)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Introduction" on page 597 of this data sheet for dimension formats.



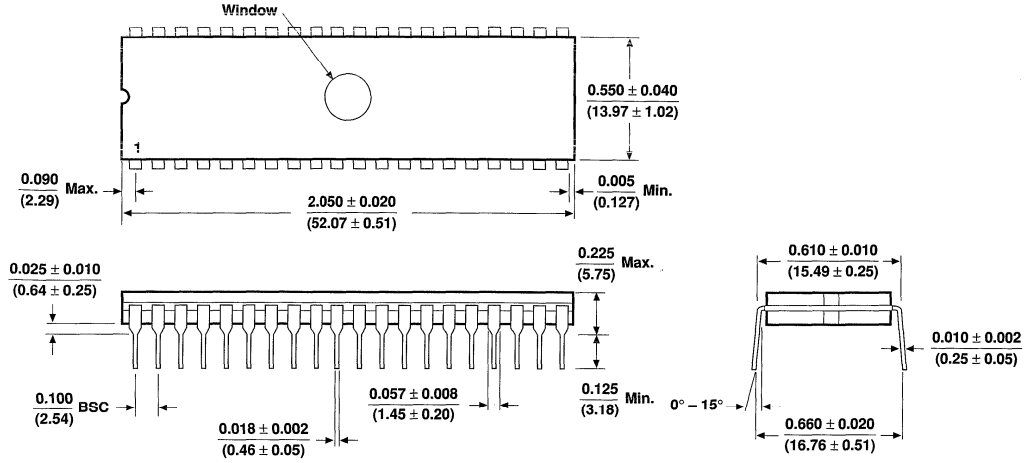
32-Pin Thin Plastic Quad Flat Pack (TQFP)

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Introduction" on page 597 of this data sheet for dimension formats.



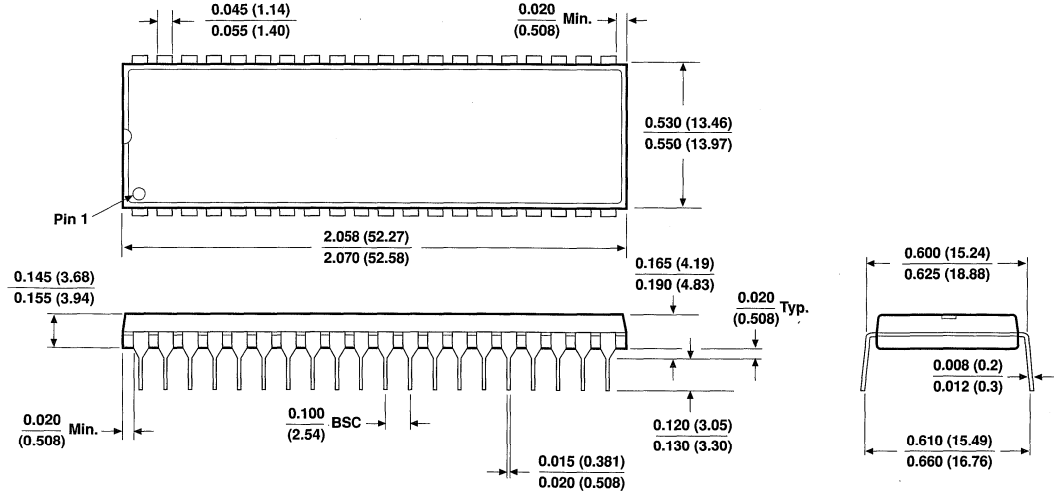
40-Pin Ceramic Dual In-Line Package (CerDIP)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Introduction" on page 597 of this data sheet for dimension formats.



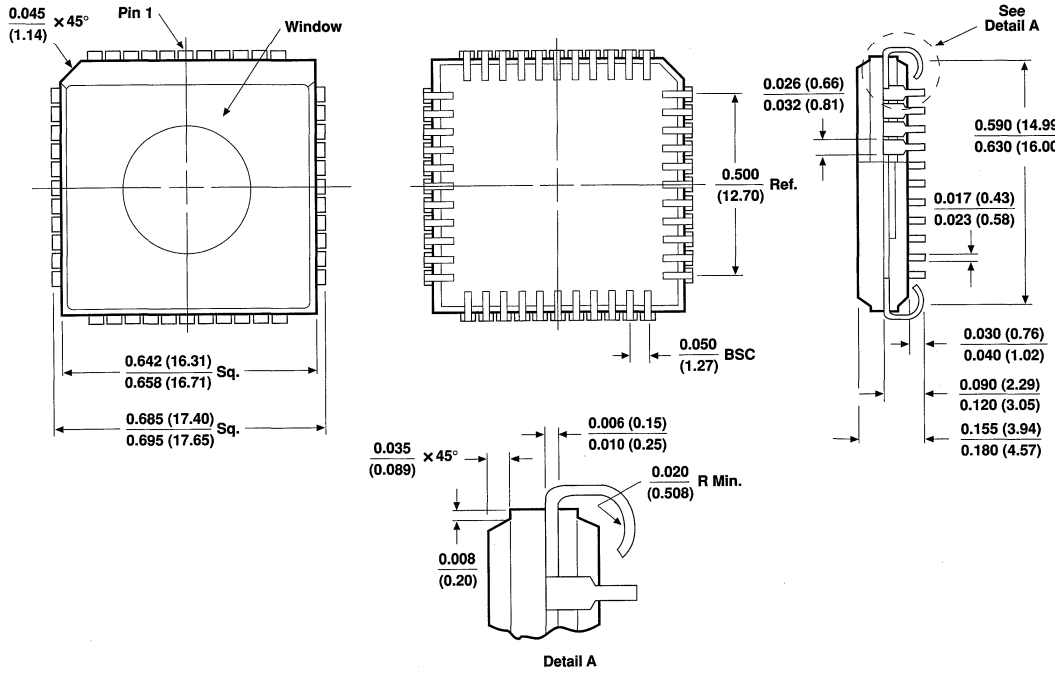
40-Pin Plastic Dual In-Line Package (PDIP)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Introduction" on page 597 of this data sheet for dimension formats.



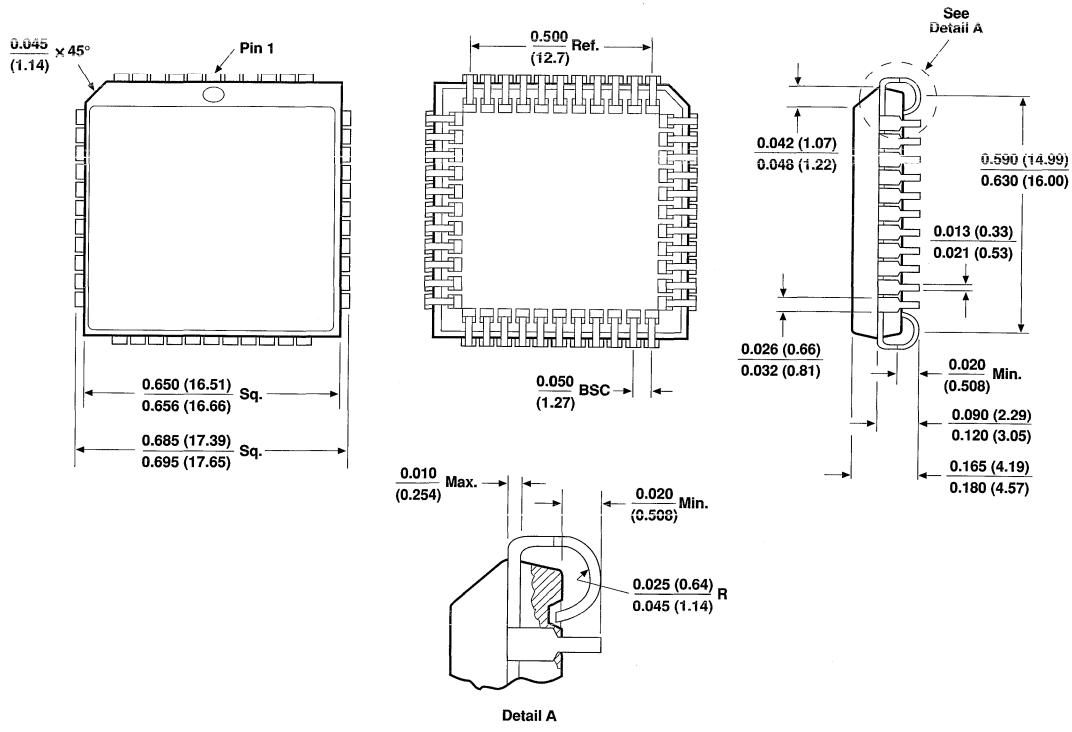
44-Pin Ceramic J-Lead Chip Carrier (JLCC)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Introduction" on page 597 of this data sheet for dimension formats.



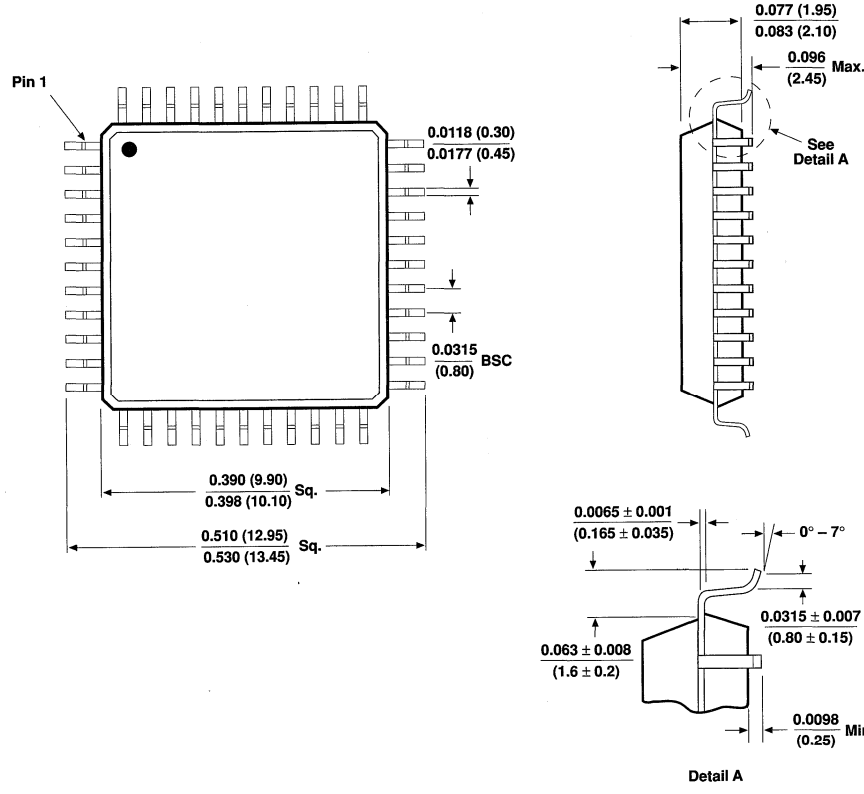
44-Pin Plastic J-Lead Chip Carrier (PLCC)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Introduction" on page 597 of this data sheet for dimension formats.



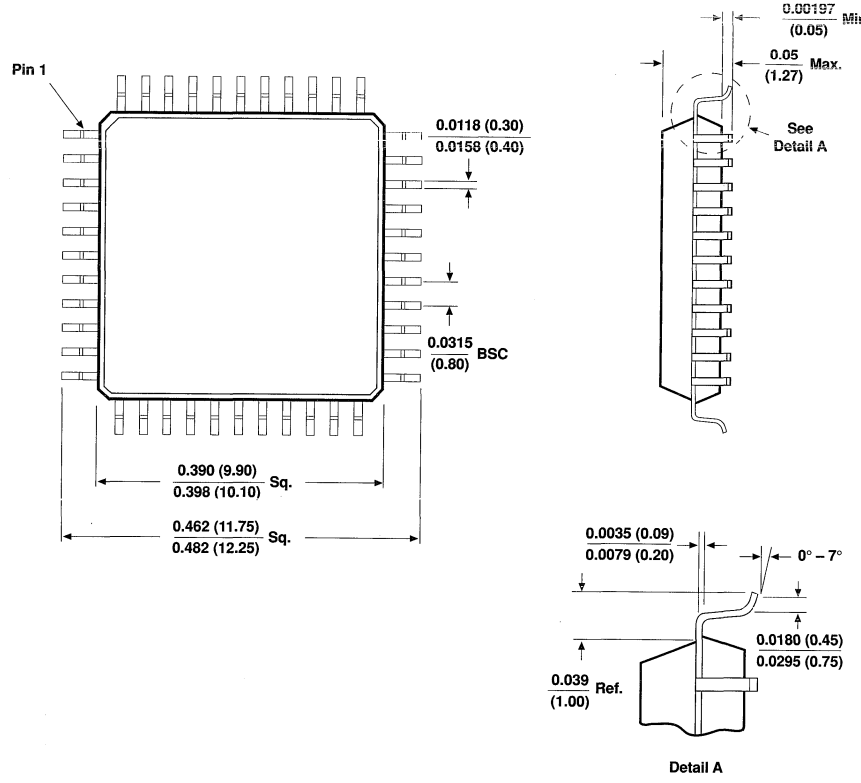
44-Pin Plastic Quad Flat Pack (PQFP)

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Introduction" on page 597 of this data sheet for dimension formats.



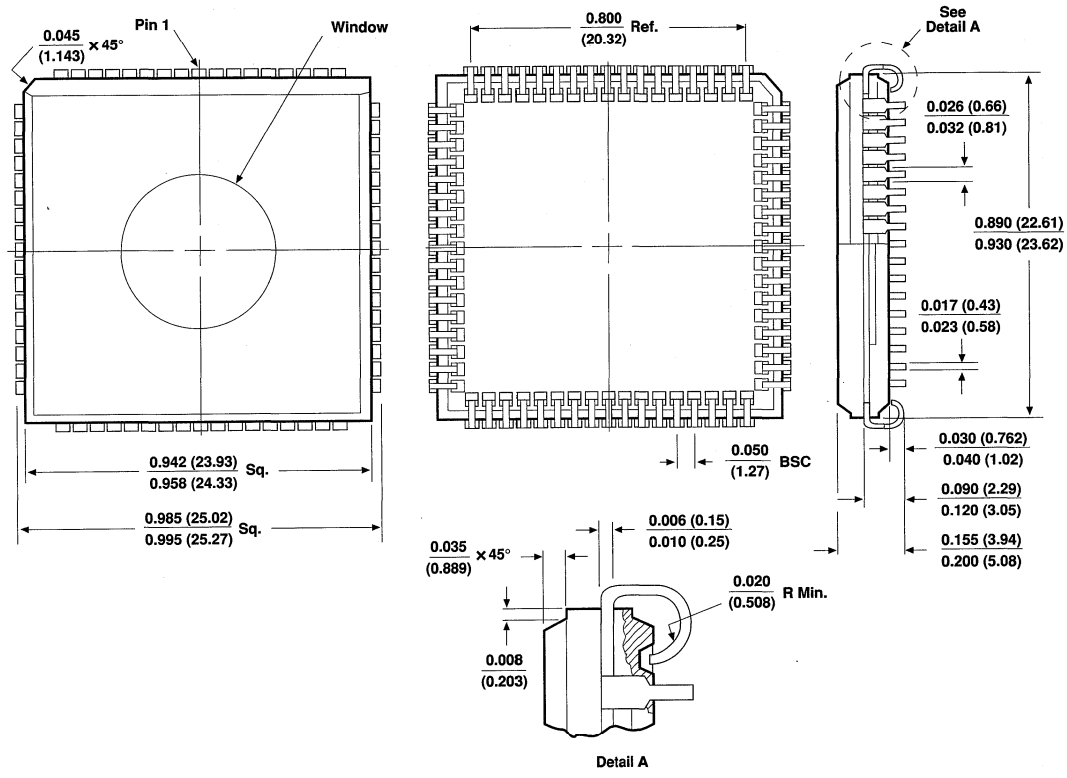
44-Pin Thin Plastic Quad Flat Pack (TQFP)

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Introduction" on page 597 of this data sheet for dimension formats.



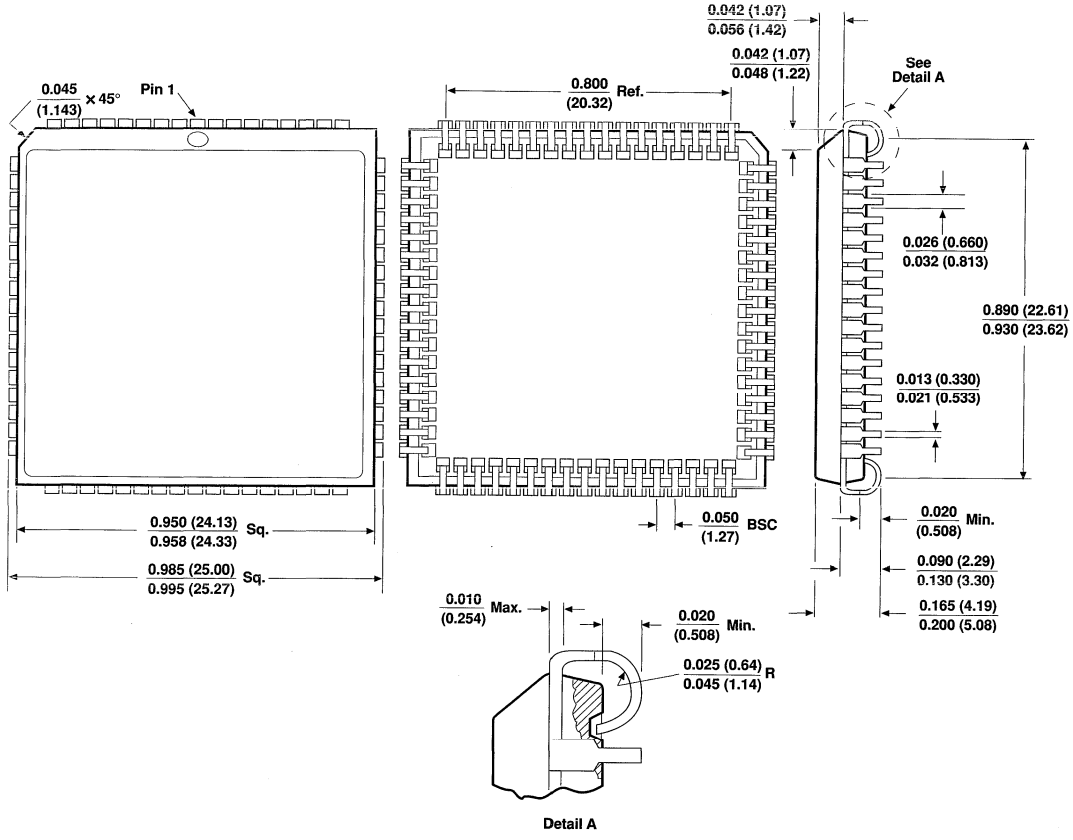
68-Pin Ceramic J-Lead Chip Carrier (JLCC)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Introduction" on page 597 of this data sheet for dimension formats.



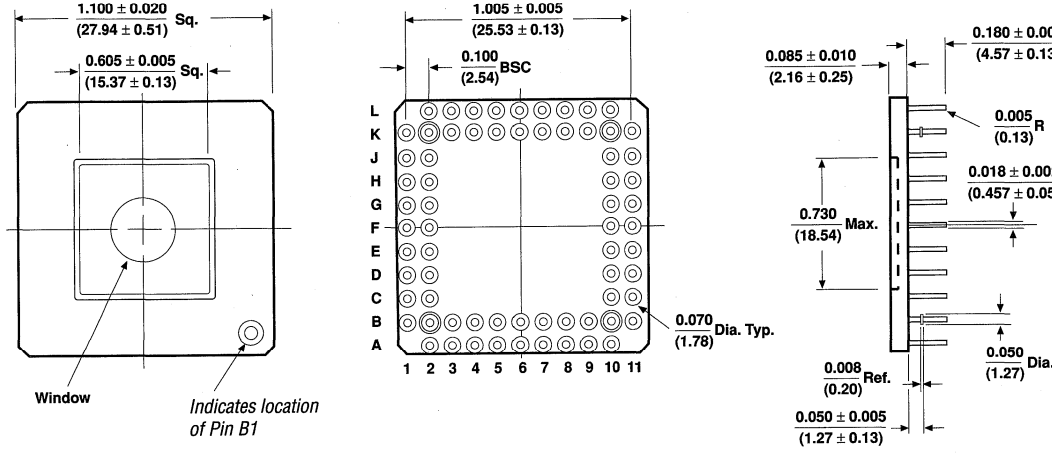
68-Pin Plastic J-Lead Chip Carrier (PLCC)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Introduction" on page 597 of this data sheet for dimension formats.



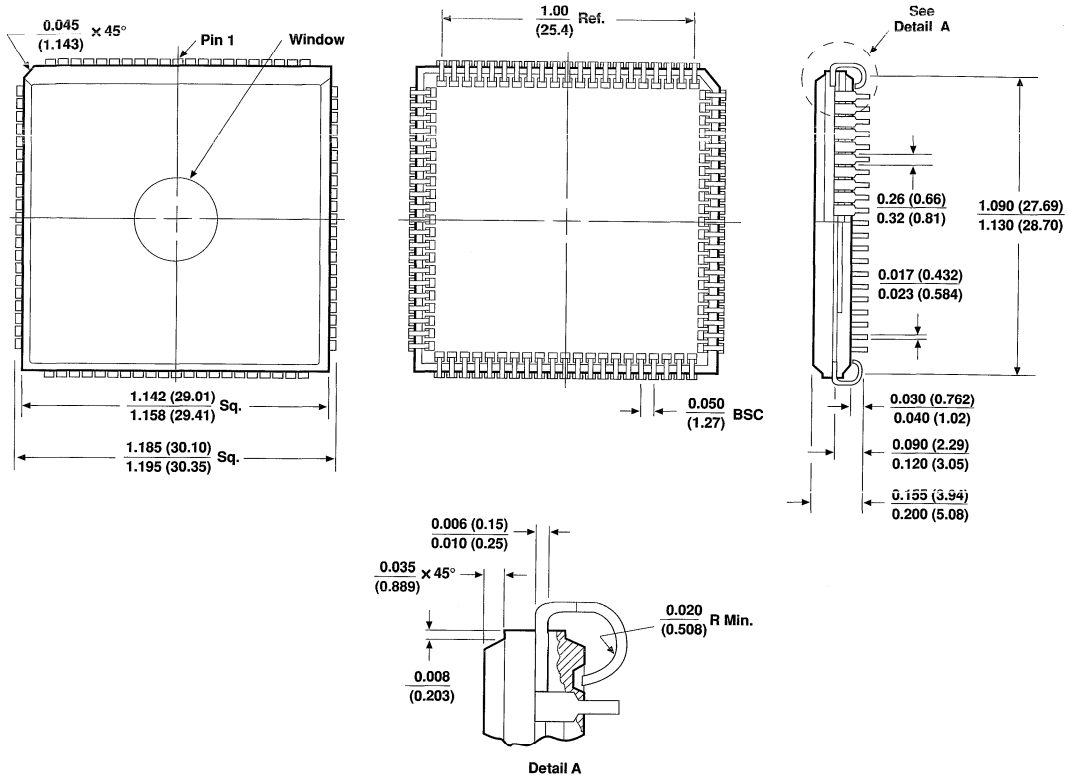
68-Pin Small Outline Ceramic Pin-Grid Array (PGA)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Introduction" on page 597 of this data sheet for dimension formats. For military-qualified products, see case outline CMGA15-PN in MIL-STD-1835.



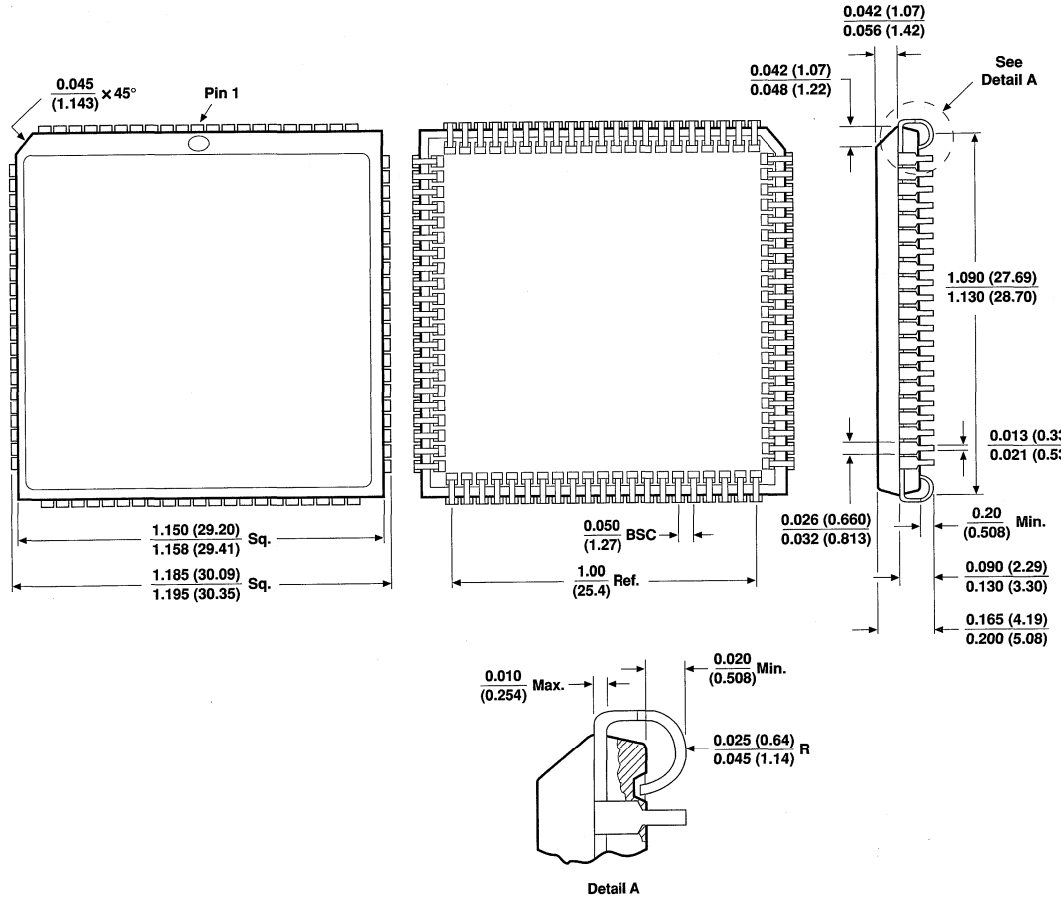
84-Pin Ceramic J-Lead Chip Carrier (JLCC)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Introduction" on page 597 of this data sheet for dimension formats.



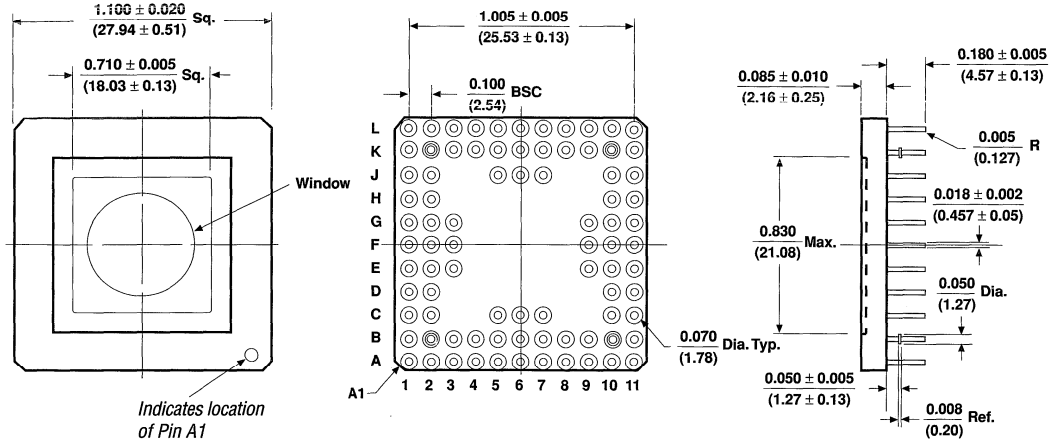
84-Pin Plastic J-Lead Chip Carrier (PLCC)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Introduction" on page 597 of this data sheet for dimension formats.



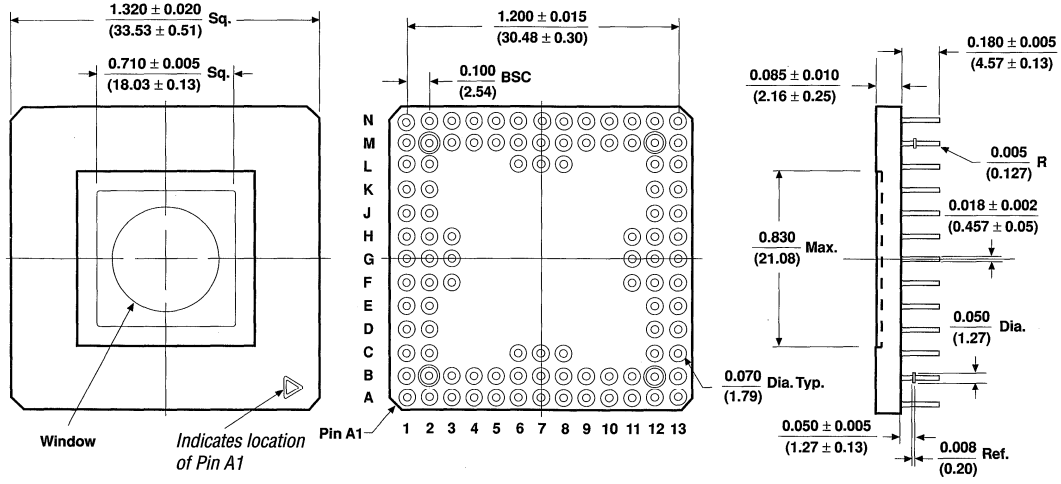
84-Pin Small-Outline Ceramic Pin-Grid Array (PGA)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Introduction" on page 597 of this data sheet for dimension formats. For military-qualified products, see case outline CMGA15-P84E in MIL-STD-1835.



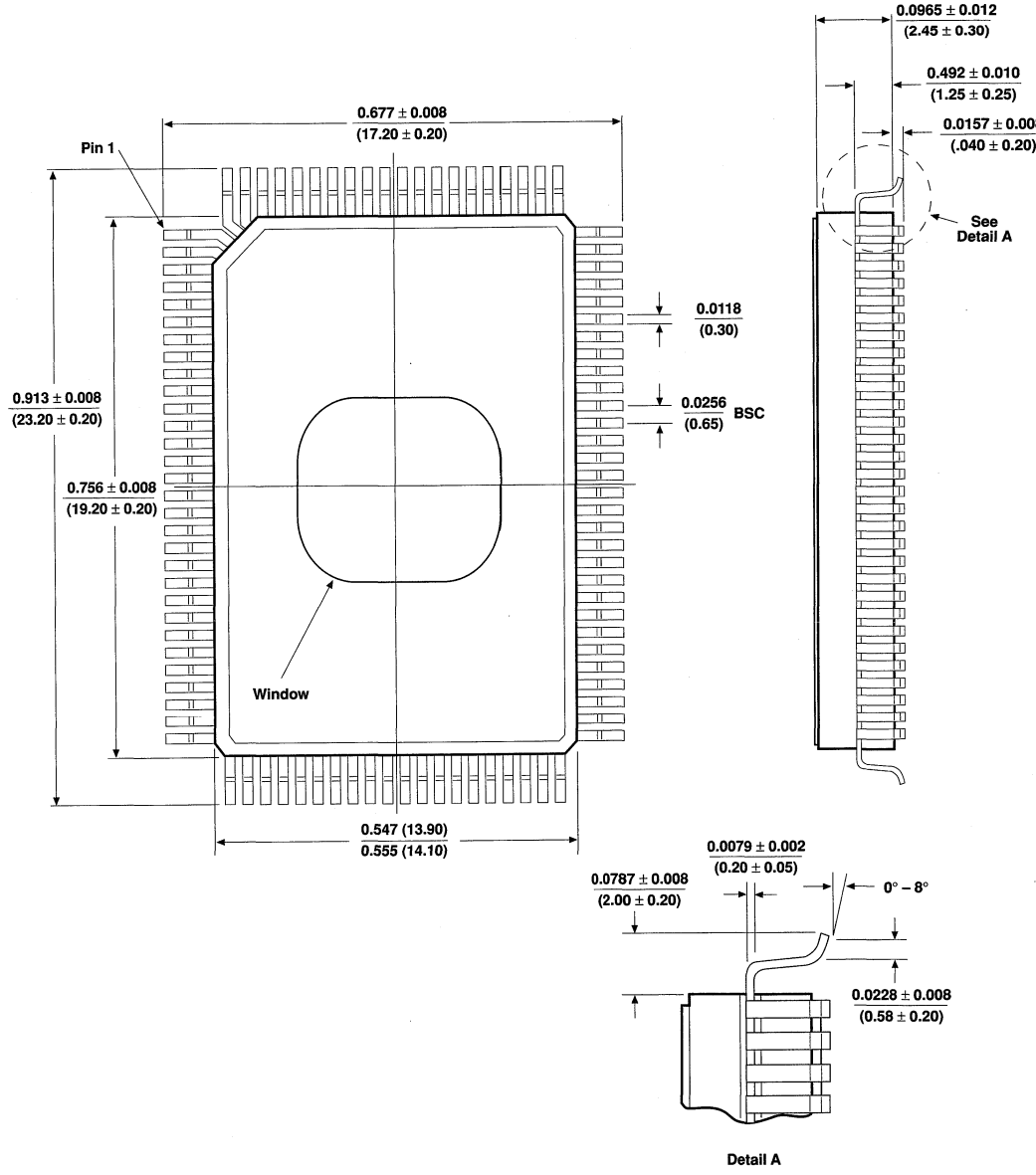
100-Pin Small-Outline Ceramic Pin-Grid Array (PGA)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Introduction" on page 597 of this data sheet for dimension formats. For military-qualified products, see case outline CMGA17-P100E in MIL-STD-1835.



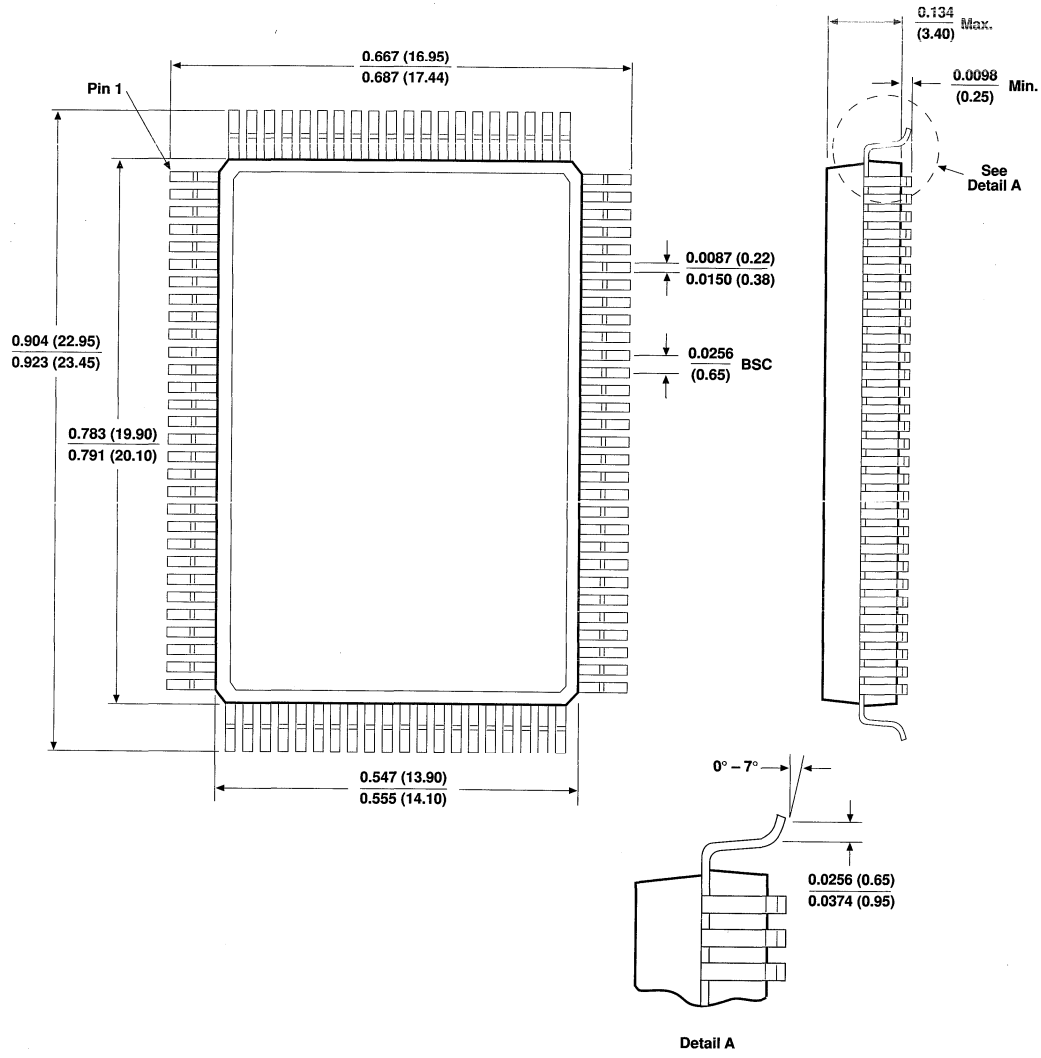
100-Pin Ceramic Quad Flat Pack (CQFP)

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Introduction" on page 597 of this data sheet for dimension formats. For military-qualified products, see case outline in SMD 5962-93144.



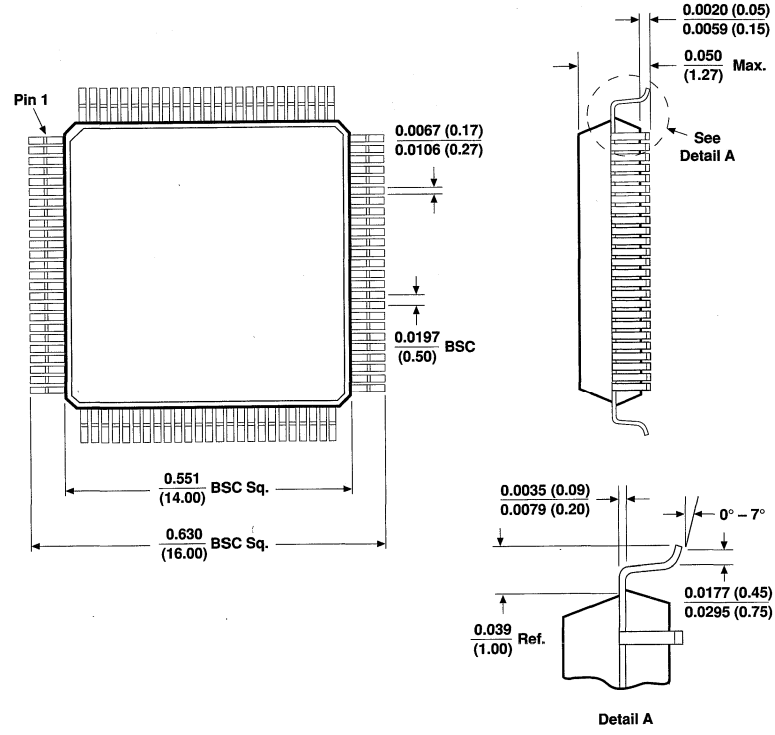
100-Pin Plastic Quad Flat Pack (PQFP)

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Introduction" on page 597 of this data sheet for dimension formats.



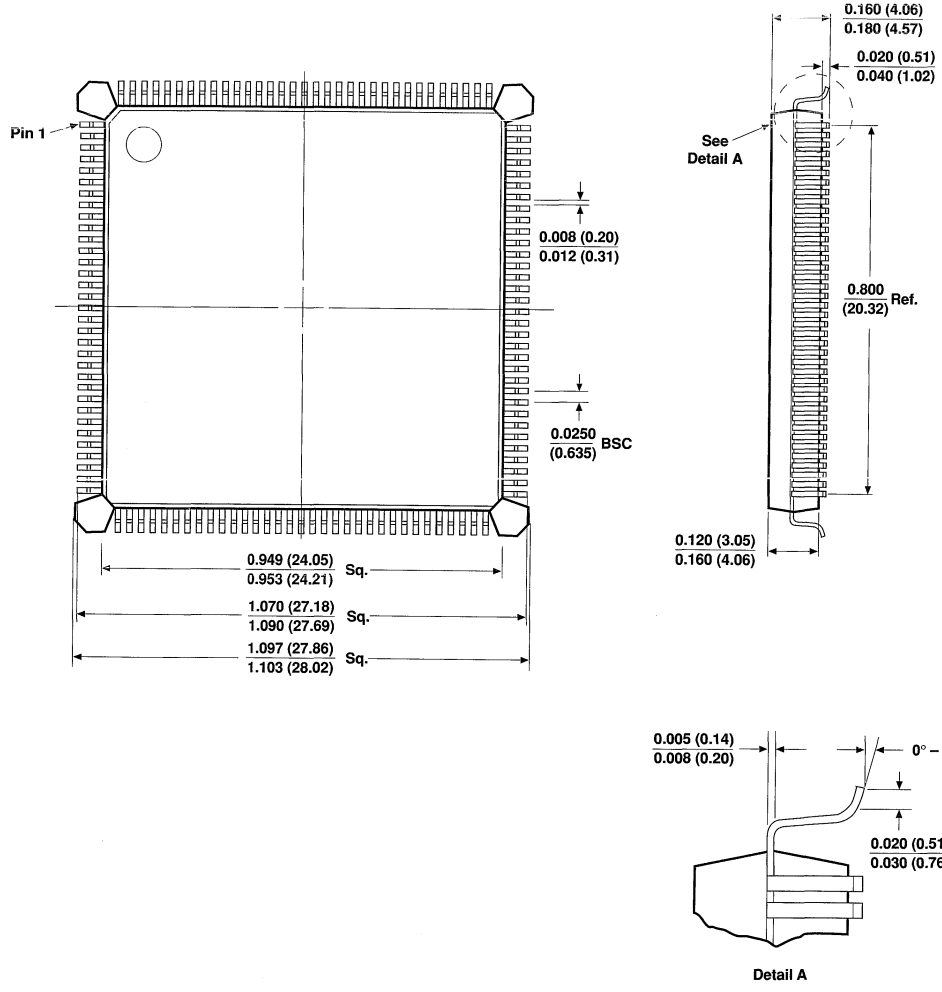
100-Pin Thin Plastic Quad Flat Pack (TQFP)

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Introduction" on page 597 of this data sheet for dimension formats.



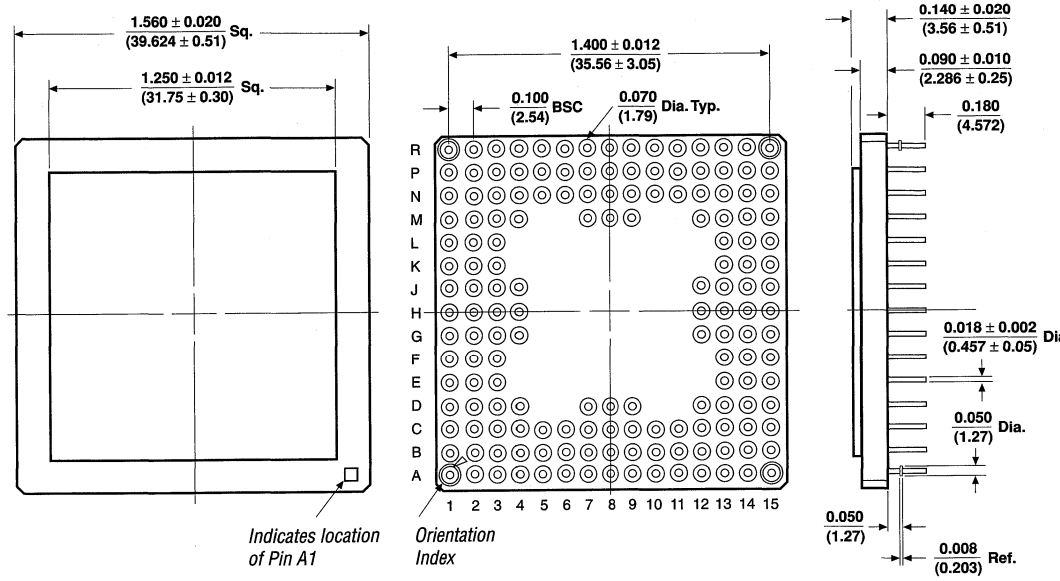
132-Pin Plastic Quad Flat Pack (PQFP)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Introduction" on page 597 of this data sheet for dimension formats.



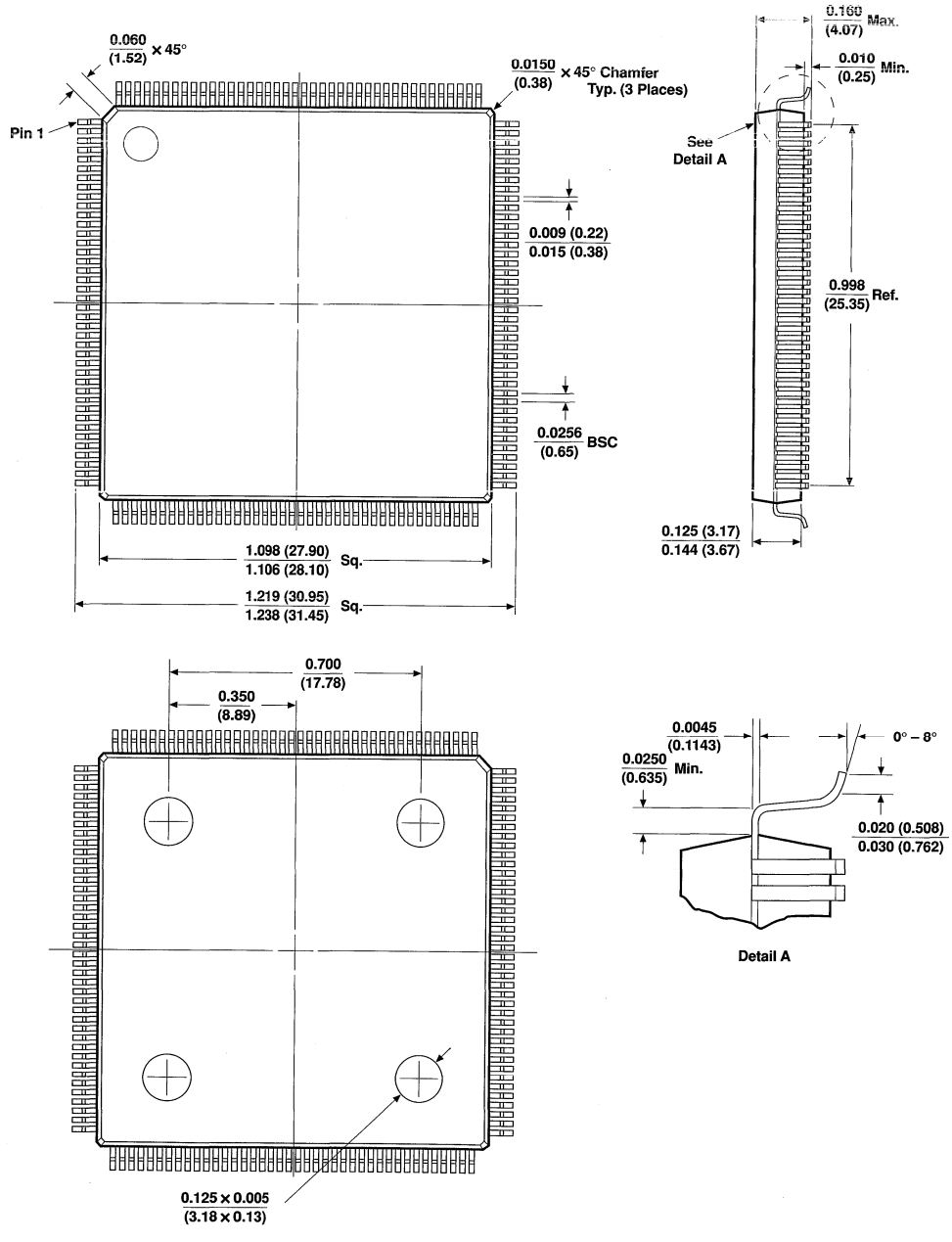
160-Pin Ceramic Pin-Grid Array (PGA)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Introduction" on page 597 of this data sheet for dimension formats. For military-qualified products, see case outline CMGA7-P160 in MIL-STD-1835.



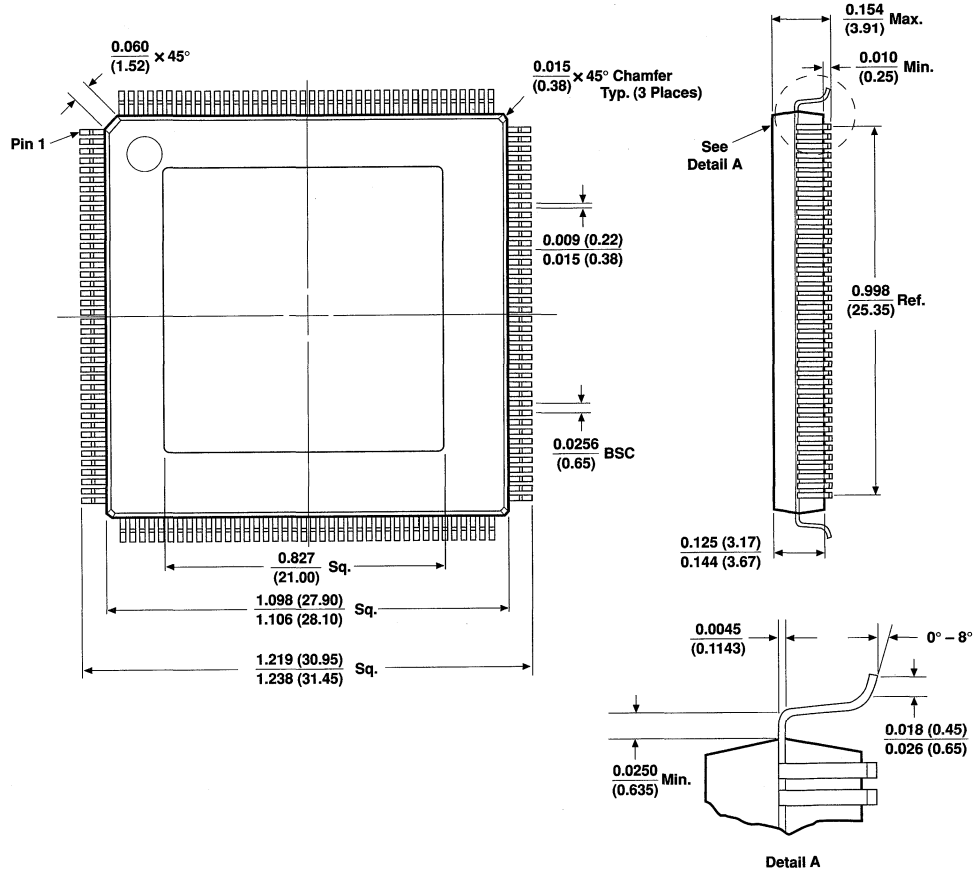
160-Pin Plastic Quad Flat Pack (PQFP)

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "introduction" on page 597 of this data sheet for dimension formats.



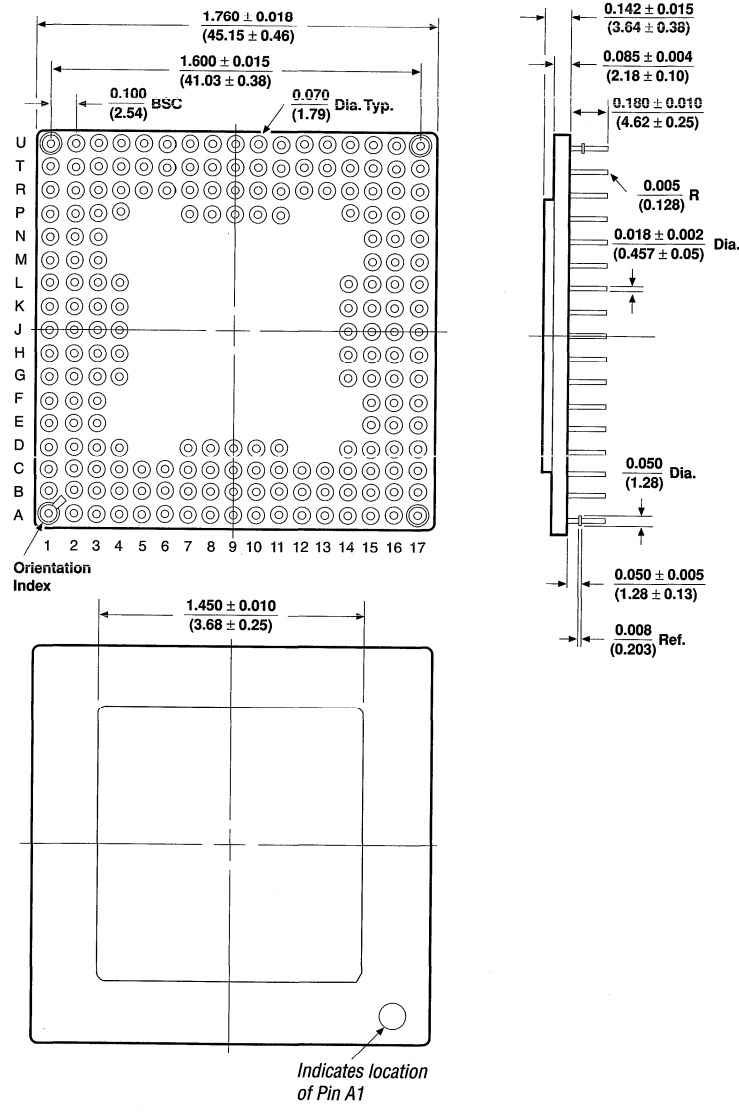
160-Pin Power Quad Flat Pack (RQFP)

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Introduction" on page 597 of this data sheet for dimension formats.



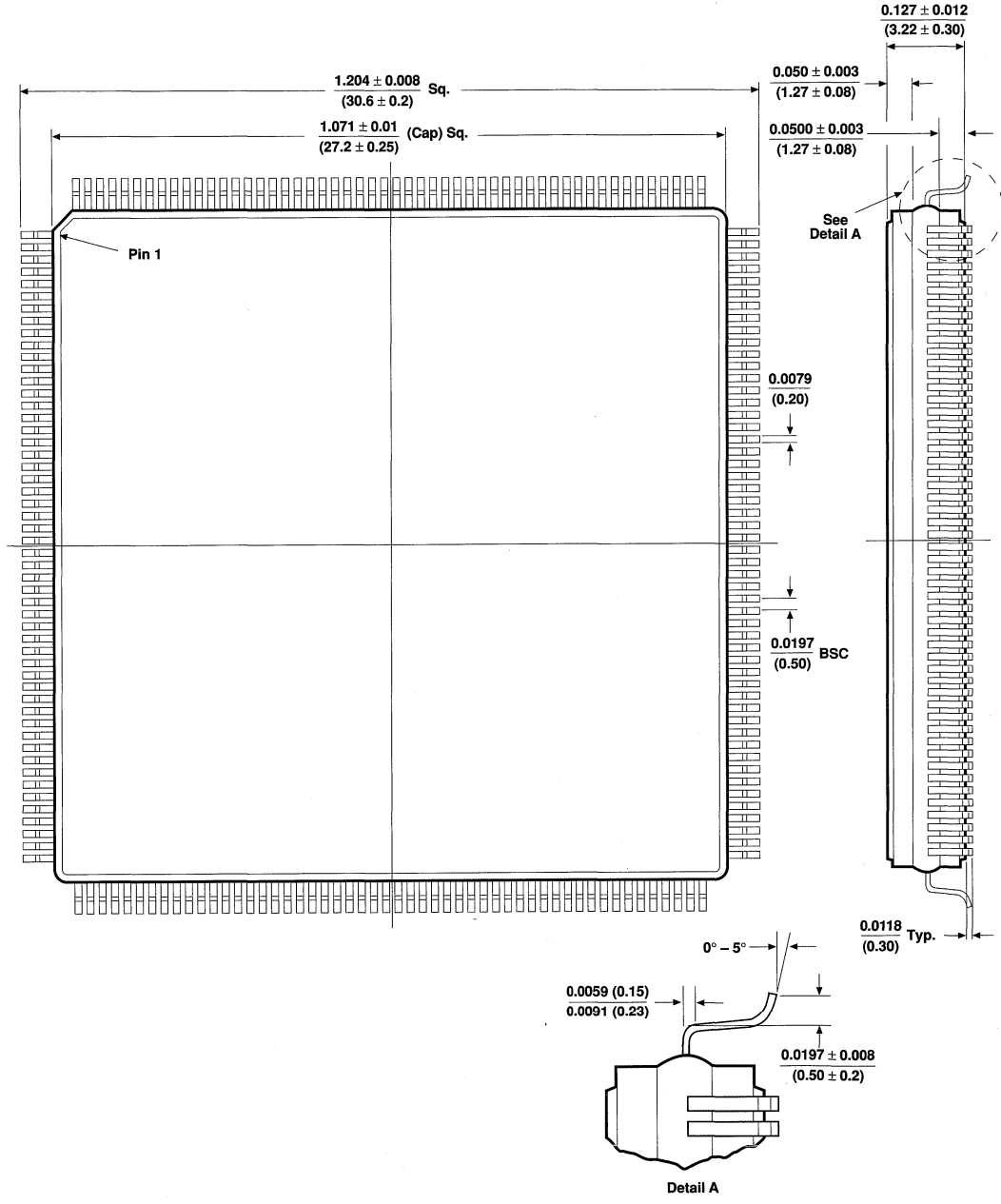
192-Pin Ceramic Pin-Grid Array (PGA)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Introduction" on page 597 of this data sheet for dimension formats. For military-qualified products, see case outline CMGA7-P192 in MIL-STD-1835.



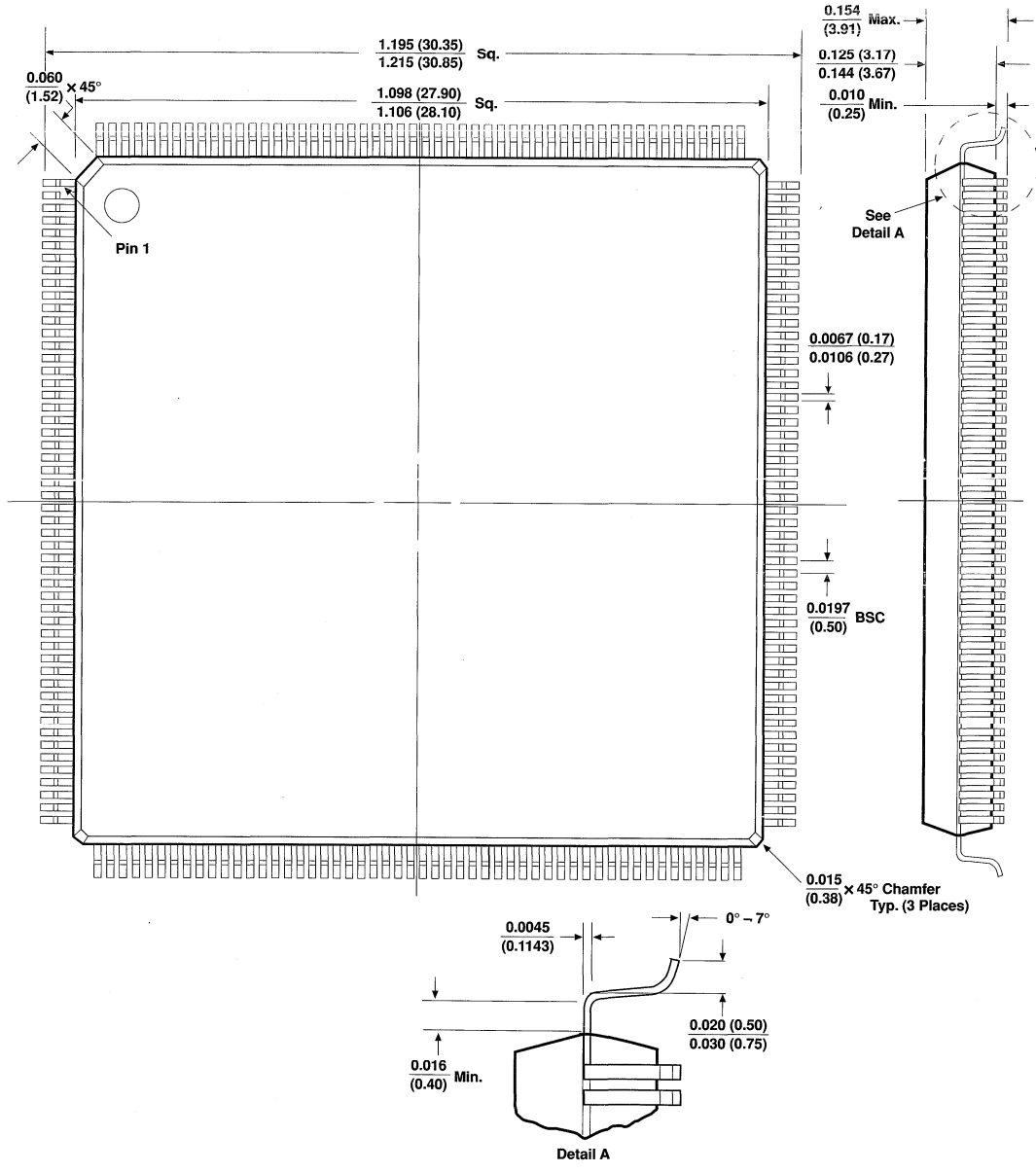
208-Pin Ceramic Quad Flat Pack (CQFP)

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Introduction" on page 597 of this data sheet for dimension formats. For military-qualified products, see case outline in SMD.



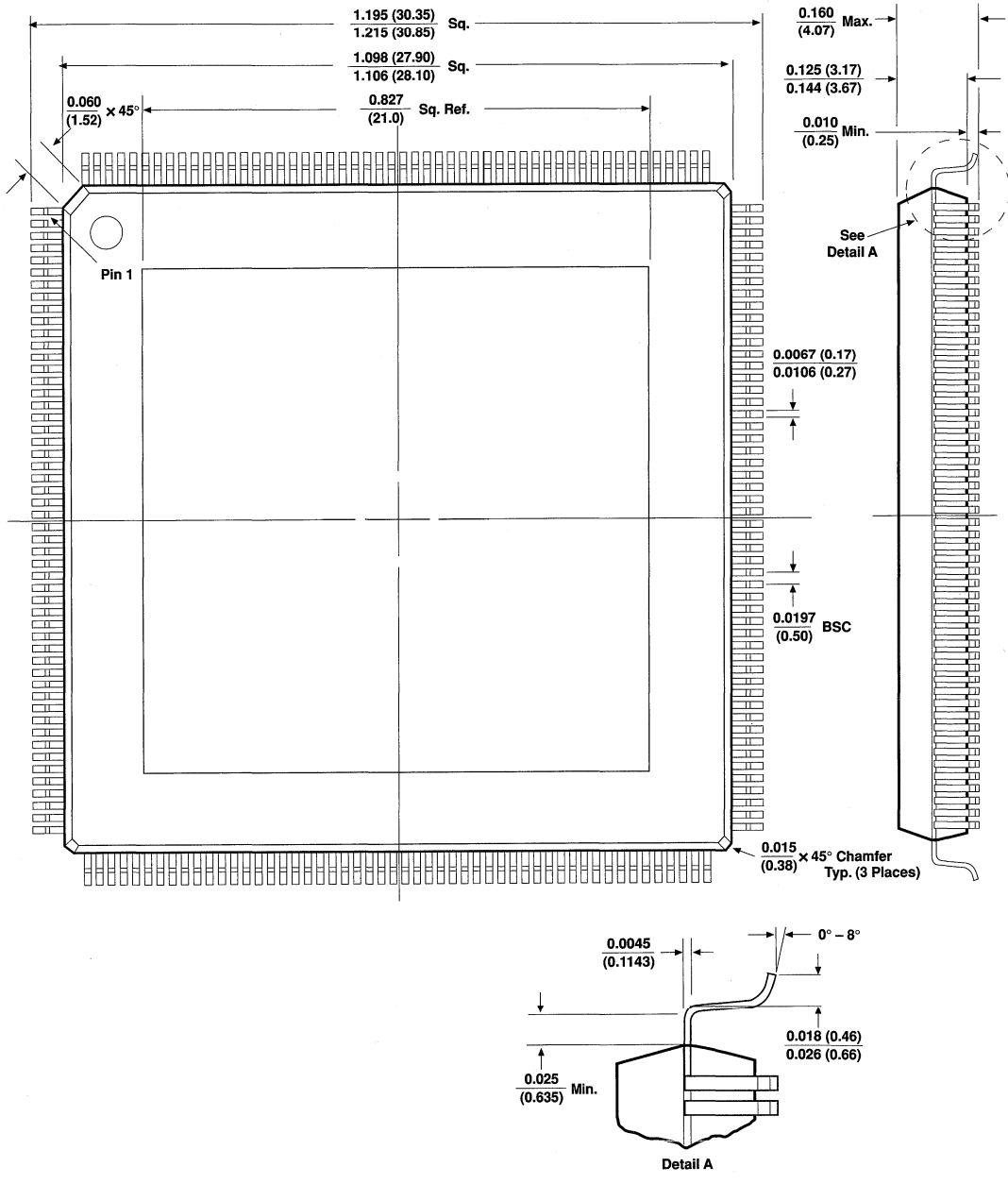
208-Pin Plastic Quad Flat Pack (PQFP)

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Introduction" on page 597 of this data sheet for dimension formats.



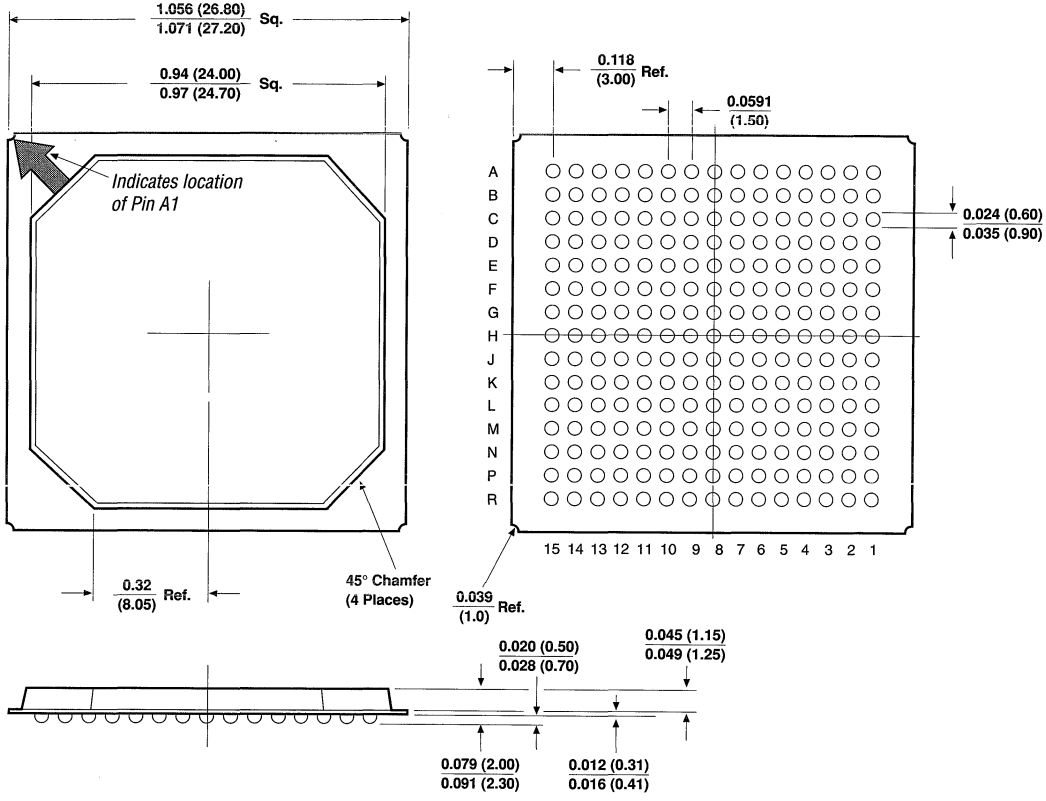
208-Pin Power Quad Flat Pack (RQFP)

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Introduction" on page 597 of this data sheet for dimension formats.



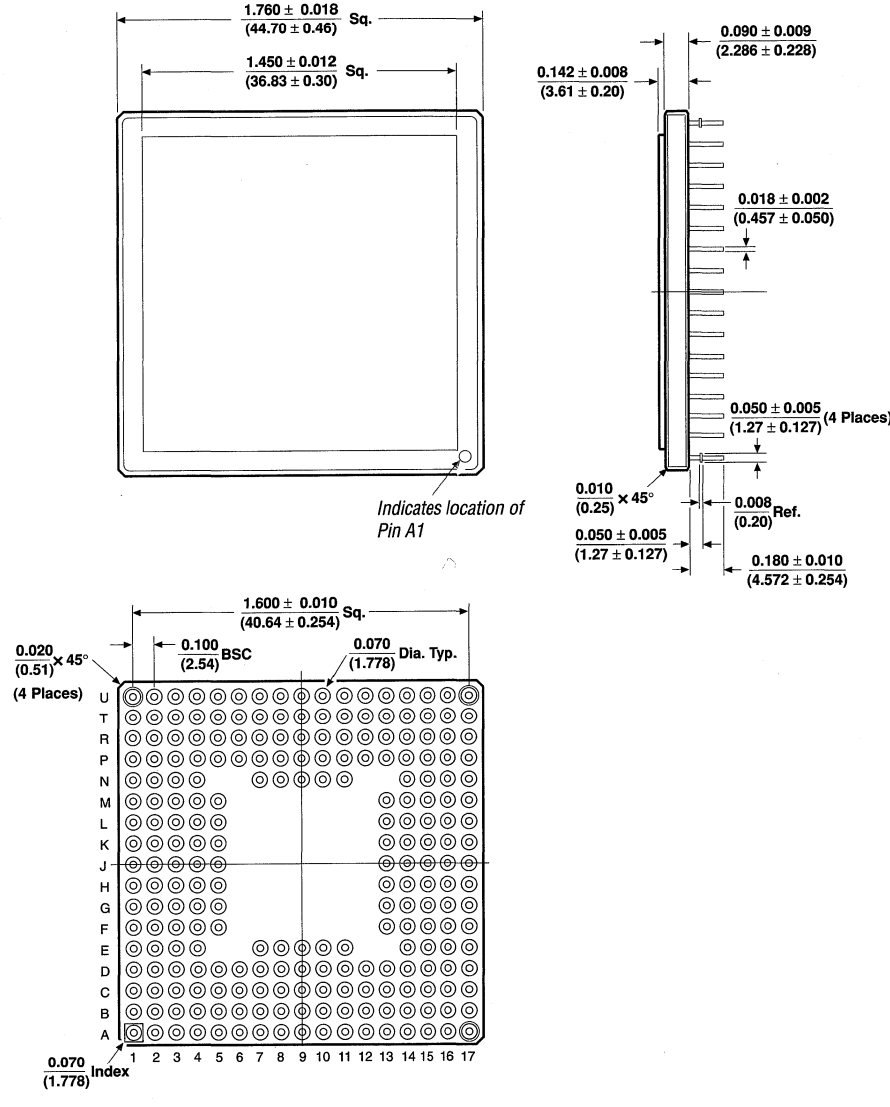
225-Pin Ball-Grid Array (BGA)

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Introduction" on page 597 of this data sheet for dimension formats.



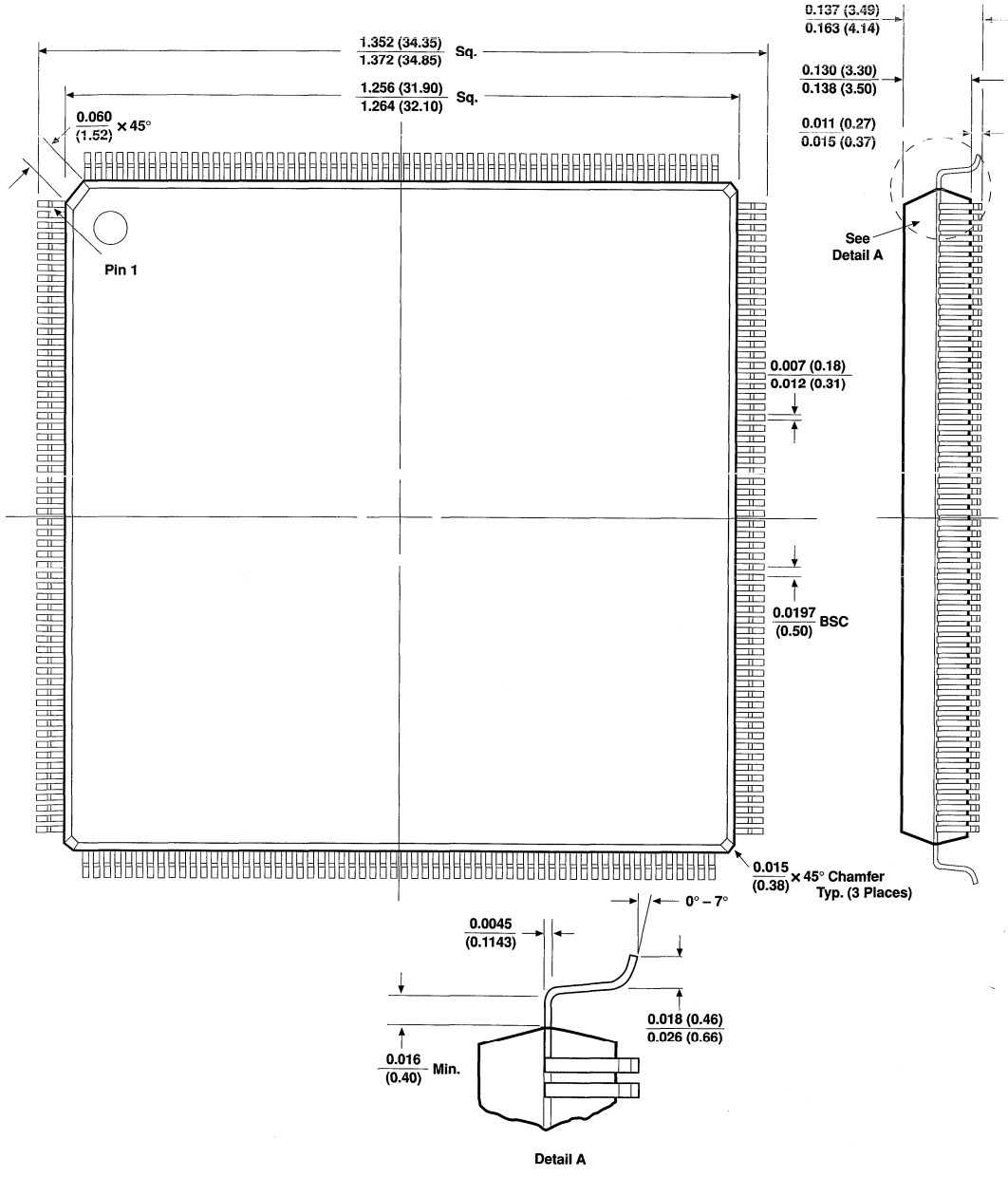
232-Pin Ceramic Pin-Grid Array (PGA)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Introduction" on page 597 of this data sheet for dimension formats.



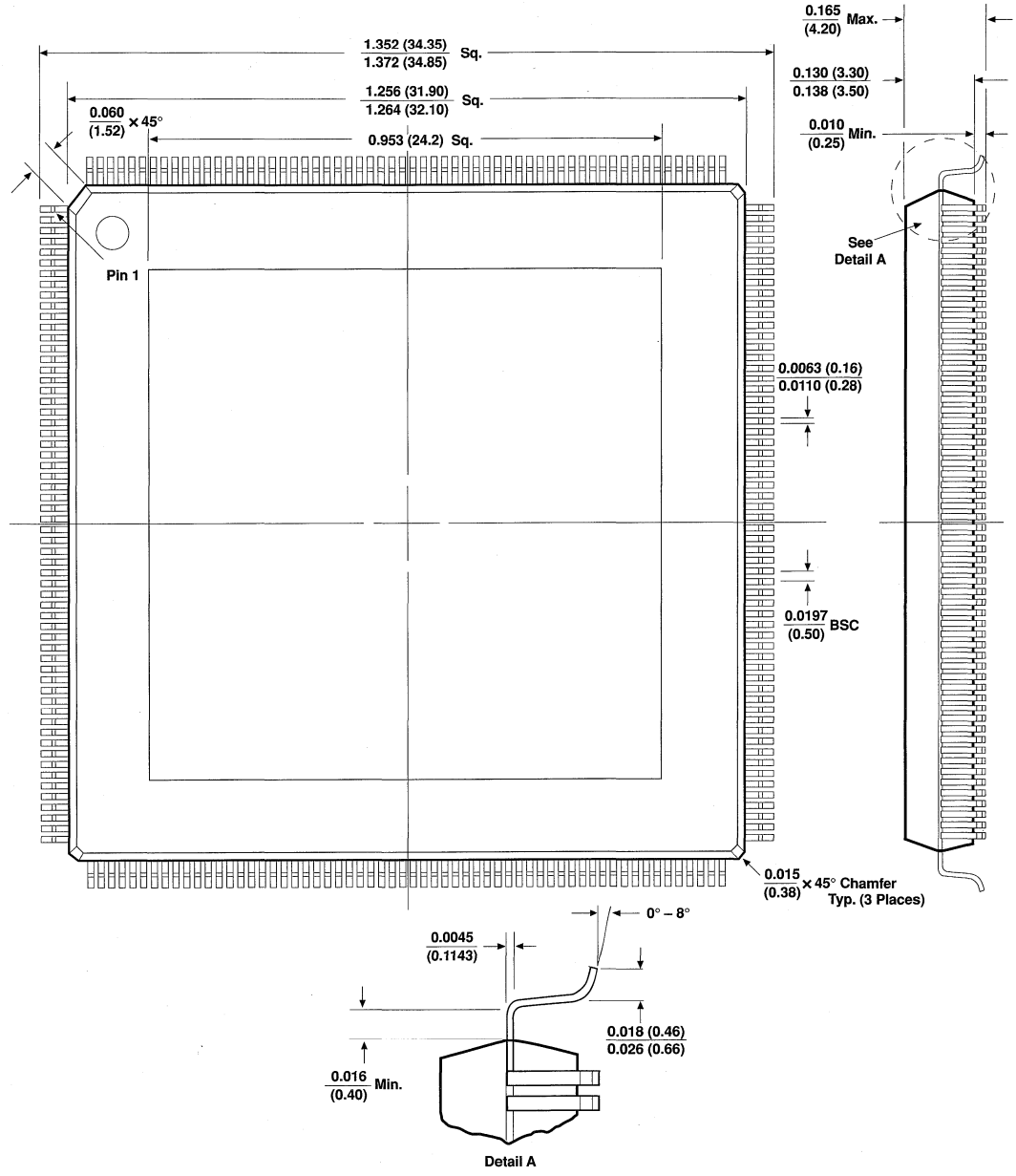
240-Pin Plastic Quad Flat Pack (PQFP)

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Introduction" on page 597 of this data sheet for dimension formats.



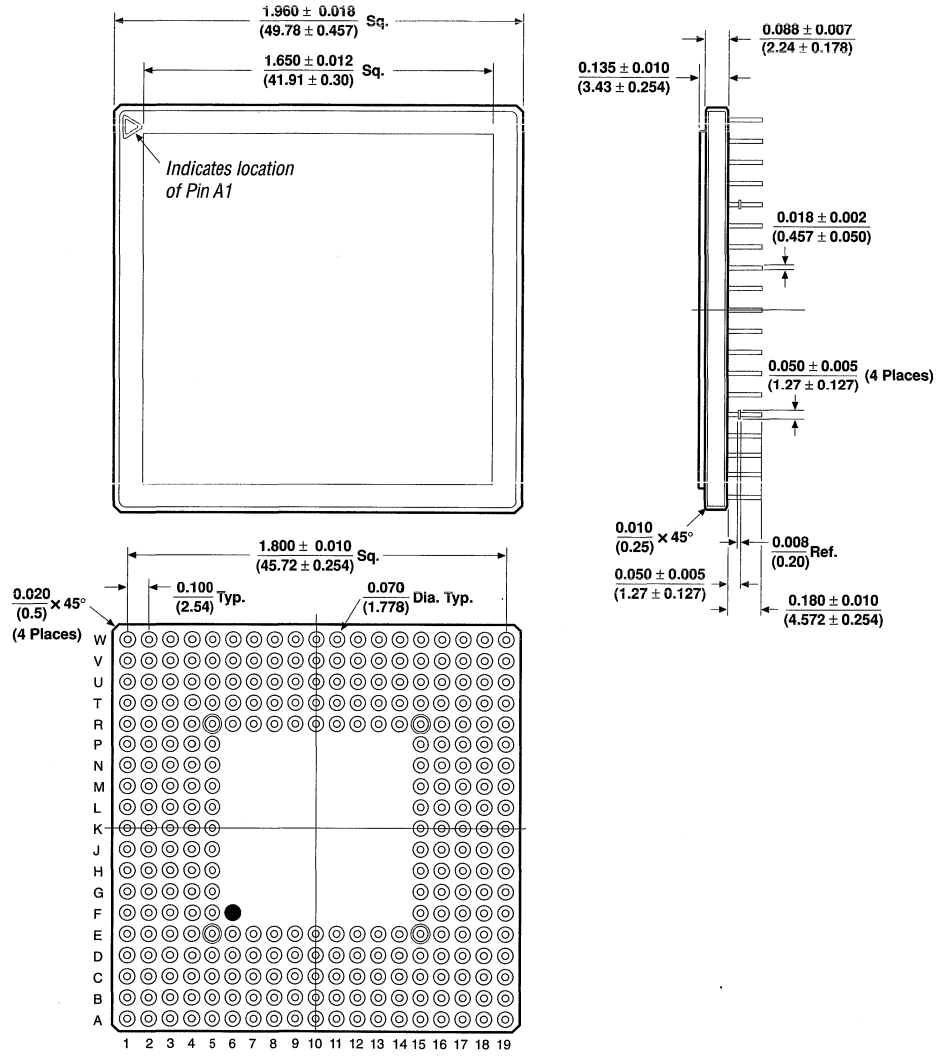
240-Pin Power Quad Flat Pack (RQFP)

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Introduction" on page 597 of this data sheet for dimension formats.



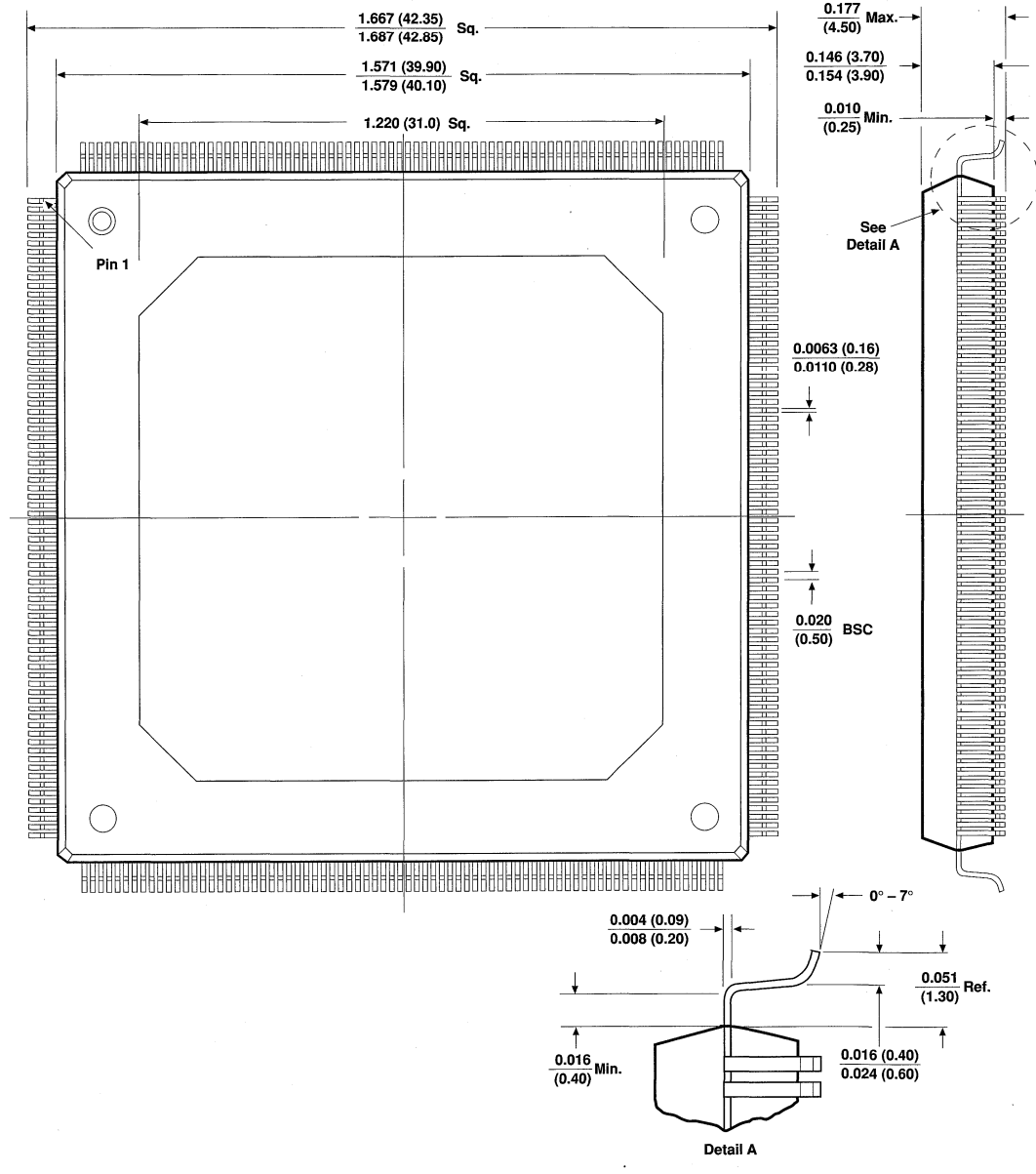
280-Pin Pin-Grid Array (PGA)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "introduction" on page 597 of this data sheet for dimension formats.



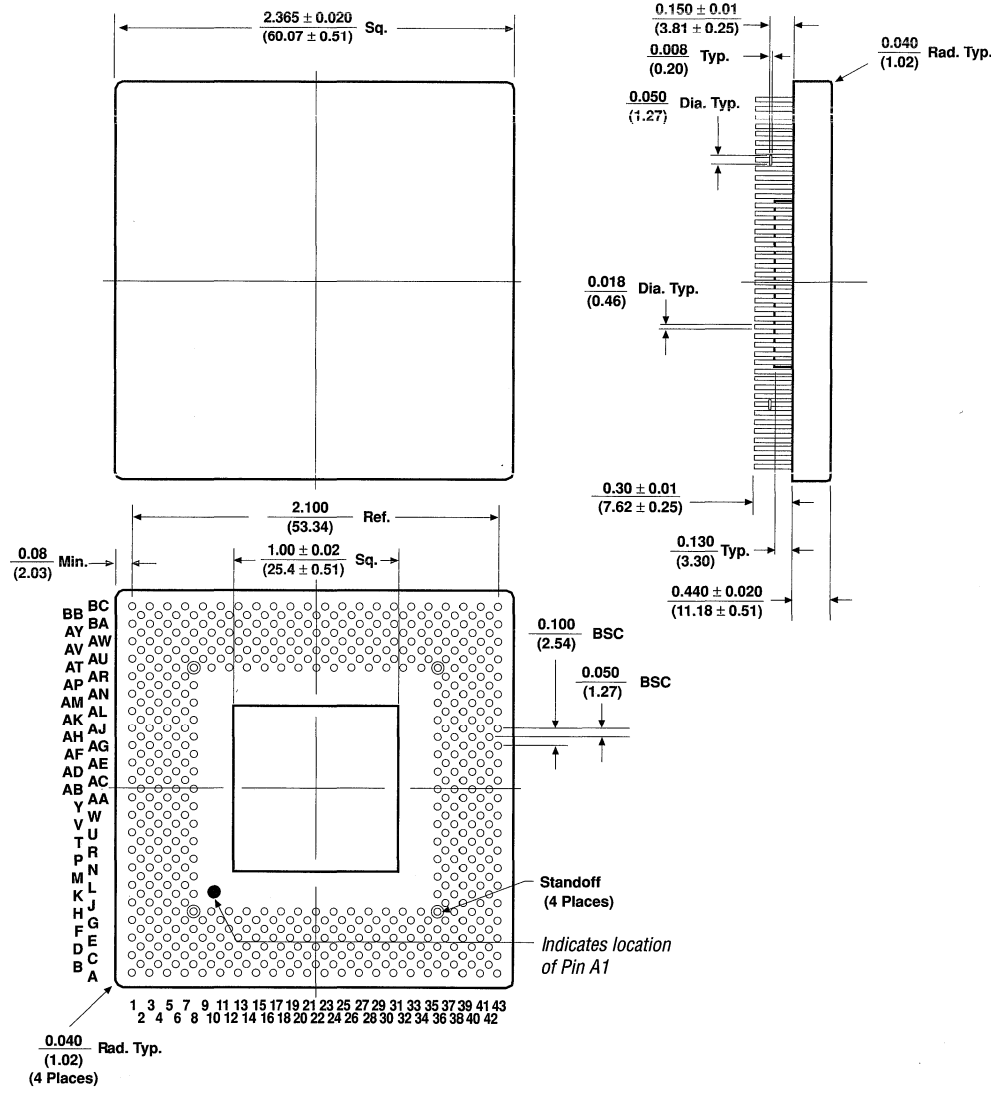
304-Pin Power Quad Flat Pack (RQFP)

Controlling measurement is in millimeters, shown in parentheses. Inch measurements are for reference only. See "Introduction" on page 597 of this data sheet for dimension formats.



560-Pin Ceramic Pin-Grid Array (PGA)

Controlling measurement is in inches. Millimeter measurements, shown in parentheses, are for reference only. See "Introduction" on page 597 of this data sheet for dimension formats.



Ordering Information

March 1995, ver. 7

Altera Devices

Figure 1 explains the ordering codes for Altera devices. Devices that have multiple pin counts for the same package include the pin count in their ordering codes. Some codes use relative numbers (e.g., -1, -2) to designate speed grades; others use actual propagation delay times (e.g., -15, -20). For information on specific package, speed grade, and operating temperature combinations, refer to individual device data sheets in this data book, or contact Altera Marketing at (408) 894-7104.

Figure 1. Device Package Ordering Codes

EPM 7032 L C 44 -7 C

Family Signature:
- EP: Classic device
- EPM: MAX 9000, MAX 7000, or MAX 5000 device
- EPF: FLEX 10K, FLEX 8000, or FLEX 8000M device
- EPC: Configuration EPROM device
- EPX: FLASHlogic device

Device Type:
- EP: 220, 224, 312, 324, 330, 600I, 610, 610I, 900I, 910, 910I, 1800I, 1810, 22V10, 22V10V, 22V10E
- EPM: 5016, 5032, 5032A, 5064, 5064A, 5128, 5128A, 5130, 5130A, 5192, 5192A, 7032, 7032V, 7064, 7096, 7128E, 7160E, 7192E, 7256E, 9320, 9400, 9480, 9560
- EPF: 8282, 8282A, 8282V, 8282AV, 8452, 8452A, 8636A, 8820, 8820A, 81188, 81188A, 81500, 81500A, 8050M
- EPC: 1064, 1064V, 1213
- EPX: 740, 780, 880, 8160

Package Type:
- D: Ceramic dual in-line package (CerDIP)
- P: Plastic dual in-line package (PDIP)
- J: Ceramic J-lead chip carrier (JLCC)
- L: Plastic J-lead chip carrier (PLCC)
- G: Ceramic pin-grid array (PGA)
- B: Ball-grid array (BGA)
- S: Plastic small-outline integrated circuit (SOIC)
- W: Ceramic quad flat pack (CQFP), *Note (1)*
- Q: Plastic quad flat pack (PQFP), *Note (1)*
- T: Thin plastic quad flat pack (TQFP), *Note (1)*
- R: Power quad flat pack (RQFP), *Note (1)*

Carrier:
Indicates device shipment in QFP carriers. This code is optional and applies to MAX 9000 devices only.

Speed Grade:
See individual data sheets in this data book for speed/product relationships (e.g., -2, -15T, or blank).

Pin Count:
Number of pins for devices with different pin-count options (FLEX 10K, FLEX 8000, MAX 9000, MAX 7000, FLASHlogic, and Configuration EPROM devices only).

Operating Temperature/Military Processing:
- C: Commercial temperature (0° C to 70° C)
- I: Industrial temperature (–40° C to 85° C)
- M: Military temperature (–55° C to 125° C)
- M883B: Processed to MIL-STD-883, current revision
- M883BX: Processed to MIL-STD-883, current revision with modified J-lead package dimension
- MB: Fully compliant with deviation to MIL-STD-883, current revision (consult Altera for specific deviations)
- 5962: DESC Standard Military Drawing (SMD)

Examples:

EPF81188AGC232-3	EPF81188A in a ceramic 232-pin PGA package, commercial temperature range, -3 speed grade
EPM5130GM883B	EPM5130 in a ceramic 100-pin PGA package, MIL-STD-883B-qualified

Note:

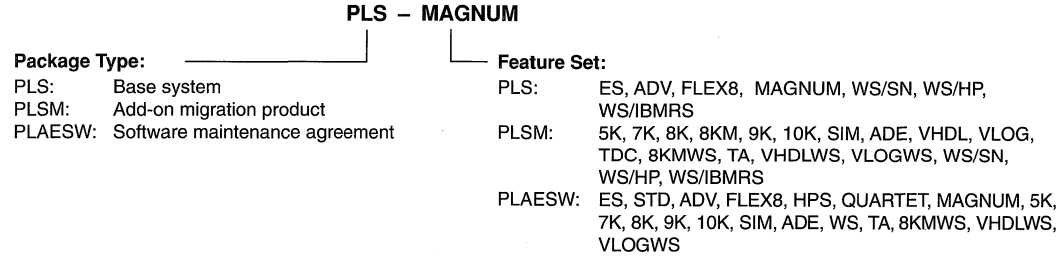
(1) MAX 5000, MAX 7000, and MAX 9000 devices in QFP packages with 100 or more pins can be ordered in QFP carriers. For more information on QFP carriers, see the *QFP Carrier & Development Socket Data Sheet* in this data book; for information on Altera shipment methods, contact Altera Marketing.

Go to the *Military Products Data Sheet* in this data book for MIL-STD-883-compliant product specifications, or contact Altera Marketing at (408) 894-7104.

Development Tools

Figure 2 explains the ordering codes for Altera development systems. For information on specific packages, refer to the *MAX+PLUS II Programmable Logic Development System Data Sheet* and the *MAX+PLUS II Selection Guide* in this data book, or contact Altera Marketing at (408) 894-7104.

Figure 2. Development System Ordering Codes



Programming Hardware

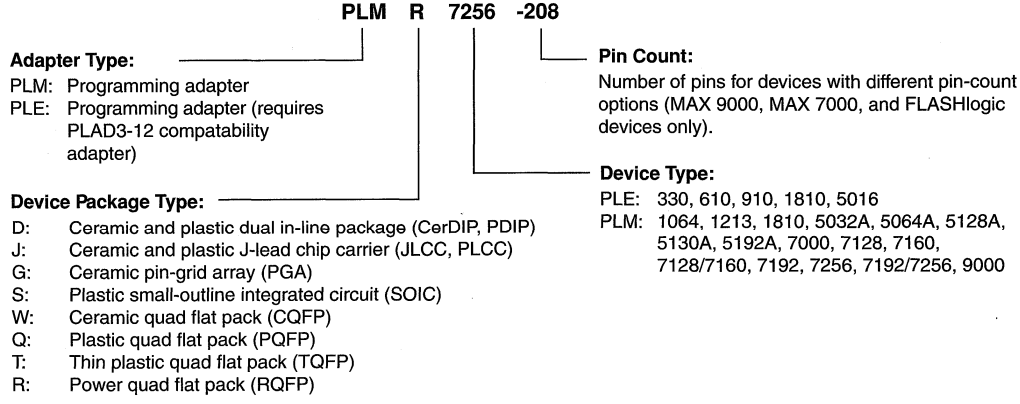
This section provides the ordering codes for Altera programming hardware and adapters. Table 1 lists the ordering codes for the programming cards, cables, and units.

Table 1. Programming Hardware

Product	Ordering Code	Description
Altera Stand-Alone Programmer	PL-ASAP2	Includes programming software, a Logic Programmer card, and the MPU.
LP6 Logic Programmer Card	PLP6	Interfaces with IBM PC-AT and compatible computers.
Master Programming Unit (MPU)	PL-MPU	With the appropriate adapter, programs all Altera devices.
Compatibility Adapter	PLAD3-12	Interfaces PLE-prefix adapters to the MPU. Together with the MPU, directly programs 20-pin Classic devices.
BitBlaster Serial Download Cable	PL-BITBLASTER	Interfaces with IBM PC-AT and compatible computers, and workstations.

Figure 3 explains the ordering codes for Altera programming adapters. Two types of adapters plug directly into the Master Programing Unit (MPU): PLM-prefix and PLAD3-12 adapters. Multiple pin-compatible devices use the same device type code shown in Figure 3; refer to the *Altera Programming Hardware Data Sheet* in this data book, or contact Altera Marketing at (408) 894-7104 for more adapter information.

Figure 3. Programming Adapter Ordering Codes



Development Sockets for QFP Carriers

Table 2 shows the ordering codes for QFP device development sockets. All MAX 5000, MAX 7000, and MAX 9000 QFP devices with 100 or more pins may be ordered in QFP carriers. QFP carriers and development sockets are rated from –65° C to 155° C and are qualified to handle commercial (C), industrial (I), and military (M) operating temperatures.

Table 2. QFP Device Sockets

Product	Ordering Code
100-pin development socket (includes removal tool)	PL-SKT/Q100
160-pin development socket (includes removal tool)	PL-SKT/Q160
208-pin development socket (includes removal tool)	PL-SKT/Q208
240-pin development socket (includes removal tool)	PL-SKT/Q240
304-pin development socket (includes removal tool)	PL-SKT/Q304

Table 3 shows the ordering codes for QFP carrier extraction tools.

Table 3. QFP Carrier Extraction Tools

Product	Ordering Code
100-pin QFP carrier extraction tool	PL-EXT1
160- and 208-pin QFP carrier extraction tool	PL-EXT2
240-pin QFP carrier extraction tool	*Note (1)*
304-pin QFP carrier extraction tool	*Note (1)*

Note:
(1) Contact Altera Marketing for ordering codes.

Selecting Sockets
for J-Lead Packages

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Introduction

Altera offers ceramic and plastic J-lead chip carrier packages (JLCC and PLCC) for many devices to reduce the "real estate" demands of a system. These small packages are generally intended for surface mounting. However, surface-mount assembly places unique demands on the development and manufacturing processes by requiring different CAD symbols for printed circuit board (PCB) layout, a different soldering process for production (reflow vs. wave solder), and different test and reliability issues. Bonding programmable devices to a PCB also prevents convenient erasure and reprogramming, which are particularly important during development.

Socketing the J-lead device is a popular compromise. Conventional mounting techniques can be used on the socketed device, either by through-hole soldering to a PCB or by mounting in a socketed carrier board for wire wrap.

This application brief discusses the following topics:

- Mechanical considerations
- Socket evaluation
- Packaging operations for wire-wrap applications
- Socket manufacturers

Mechanical Considerations

Burn-in sockets are zero-insertion-force sockets that do not deform a device's leads. Currently, burn-in sockets have dimensions similar to those of production sockets, making them the best option for prolonging the life of a reprogrammable device during prototyping, while still allowing the use of production sockets later in the design process.

Once a design enters the production phase, cost becomes a major concern. Low-cost production sockets, designed to hold a device permanently and securely, are widely available. These sockets must exert a reasonable force on the device leads to prevent the device from popping out of the socket. After several insertions, this force can deform the leads, causing them to short out or fail to make contact, and render the device unusable. Therefore, Altera strongly recommends using a burn-in socket during the design and development phases of a project, and a low-cost production socket.

Production sockets must be chosen carefully. If an erasable device needs to be removed up to 10 times for reprogramming, it is preferable to use non-deforming, low-insertion-force sockets. In high-stress environments (e.g., strong G-forces, thermal shock, high humidity), sockets with high insertion forces and optional retention clips are needed. To reduce the possibility of damaging device pins, most manufacturers of high-quality sockets include a stand-off inside the socket that prevents a device from being forced too far into a socket.

Socket Evaluation

Altera tested available production sockets for use with 44-, 68-, and 84-pin windowed ceramic J-lead devices. Each socket was subjected to three tests:

- The change in the gap between the corner pins of each device was measured before and after each of 10 insertions.
- Each pin of the socket was wired in series and tested for open or short circuits lasting longer than 10 µs. This opens-and-shorts test was performed while the socket was attached to a vibration block. The amplitude of vibration was 3.0 mm peak-to-peak at a frequency that varied from 10 Hz to 55 Hz to 10 Hz, in 1-minute cycles for 2 hours. The vibration test was performed on all three axes at a temperature of 70° C.
- The actual point of contact between the socket pin and the device lead was photographed to determine the direction of the forces and the amount of surface contact between them.

Sockets from eight manufacturers were tested. Tables 1, 2, and 3 show the results of the opens-and-shorts tests for the 44-, 68-, and 84-pin production sockets that passed the tests. Sockets are ranked by their ability to maintain the device's pin integrity after multiple device insertions.

Table 1. Summary of 44-Pin Production Socket Analysis

Vendor and Part Number	Comments
Augat, Inc. PCS-044A-1	Least pin deformation. Contact force has a downward component. No retainer clip option.
AMP, Inc. 821575-1	Moderate pin deformation. Contact force has a downward component. No retainer clip option.

Table 2. Summary of 68-Pin Production Socket Analysis

Vendor and Part Number	Comments
Augat, Inc. PCS-068A-1	Least pin deformation. Contact force has a downward component. No retainer clip option.
ITT/Cannon Corporation LCS-68-2	Low pin deformation. Contact force has a downward component. Has a retainer clip option.
AMP, Inc. 821574-1	Moderate pin deformation. Contact force has a downward component. No retainer clip option.

Table 3. Summary of 84-Pin Production Socket Analysis

Vendor and Part Number	Comments
Augat, Inc. PCS-084A-1	Least pin deformation. Contact force has a downward component. No retainer clip option.
ITT/Cannon Corporation LCS-84-2	Moderate pin deformation. Contact force has a downward component. Has a retainer clip option.
AMP, Inc. 822151-1 (for surface mount)	Moderate pin deformation. Contact force has a downward component. No retainer clip option. Designed for plastic packages.
AMP, Inc. 821573-1	Large pin deformation. Very tight fit. No retainer clip option. Due to pin deformation, Altera recommends a maximum of three insertions. Designed for ceramic packages.
Burndy Corporation QILE-84P-410T	Large pin deformation. Very tight fit. No retainer clip option. Due to pin deformation, Altera recommends a maximum of three insertions.

Vendors may provide additional information about their products, such as material selection, prevention of solder ingress during wave soldering, or lead shape. Altera recommends qualifying sockets before committing to a particular vendor.

Table 4 shows the contact distance for Altera packages. These measurements should be used to select a socket, preferably with internal stand-offs, for use with Altera devices.

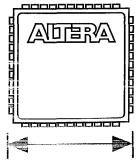

Table 4. Device Contact Distances

Package	Pins	Contact Distance (Minimum mils)	Contact Distance (Maximum mils)
PLCC	20	385	395
PLCC, JLCC	28	485	495
PLCC, JLCC	44	685	695
PLCC, JLCC	68	985	995
PLCC, JLCC	84	1,185	1,195

Packaging Operations for Wire-Wrap Applications

Wire-wrap applications require a through-hole mount compatible with the J-lead package. The sockets specified do not typically conform mechanically to most wire-wrap panels. Wire-wrap cards have machine receptacles in rows with 100-mil spacing between receptacles and 300-mil spacing between rows. Carrier boards provide an effective way to bridge the gap. Mounting a socket to a carrier board provides the convenience of wire wrap with only a small real estate penalty. Some carrier boards have signal routing with shorter paths or 45° bends to minimize signal reflection.

Socket Manufacturers

Table 5 lists telephone numbers for the vendors noted in this application brief. Contact the appropriate vendor for additional information.

Table 5. Manufacturers

Product	Company	Telephone Number
Production sockets	3M/Textool Corporation	(800) 328-0411
	AMP, Inc.	(800) 522-6752
	Augat Inc.	(508) 699-9800
	Burndy Corporation	(408) 245-2590
	ITT/Cannon Corporation	(714) 261-5300
Test and burn-in sockets	3M/Textool Corporation	(800) 328-0411
	AMP, Inc.	(800) 522-6752
	Advanced Interconnections Corporation	(401) 823-5200
	Dai-Ichi Seiko Company, Ltd. (Japan)	(81) 0482-53-3131
	Emulation Technology, Inc.	(408) 982-0660
Carrier boards and wire-wrap adapters	Advanced Interconnections Corporation	(401) 823-5200
	Emulation Technology, Inc.	(408) 982-0660

Information in this application brief is based on tests performed by Altera and information provided to Altera by various vendors. Altera assumes no liability for the use of third-party products mentioned in this publication.

Technical Support
from Altera Applications

March 1995, ver. 2

Introduction

Altera's technical support team includes over 50 Application Engineers dedicated to promptly resolving customers' technical issues. Altera responds to customers' questions promptly and efficiently via e-mail, telephone, or fax. Application Engineers are located at Altera headquarters in San Jose, California, and at locations around the world.

Altera Applications offers the following services:

- Technical support hotline
- Technical publications
- Altera Express
- Electronic mail
- Bulletin board service
- Altera FTP site
- CompuServe
- World-Wide Web site
- Training courses
- Design evaluations
- On-site support

Technical Support Hotline

Customers in the United States and Canada can receive direct technical support on Altera devices and software by calling Altera Applications at (800) 800-EPLD between the hours of 7:30 a.m. and 5:00 p.m. Pacific Time. Customers outside the United States and Canada can receive technical assistance by calling an Application Engineer at (408) 894-7000 between the hours of 7:30 a.m. and 5:00 p.m. Pacific Time, or by contacting their local Altera distributor or sales office. Customers can also fax technical support questions to (408) 954-0348.

Technical Publications

Altera produces a variety of technical literature to help customers select and design with programmable logic, including application notes, application briefs, and data sheets. Altera also provides *News & Views*, a quarterly newsletter that includes the latest information on Altera products, technical articles written by Altera Application Engineers, and a question and answer section that addresses many commonly asked questions. All registered users of Altera products receive *News & Views* each quarter. Customers who wish to request Altera technical publications, or add their name to the *News & Views* mailing list, can contact Altera Literature Services at (408) 894-7144.

Altera Express

The Altera Express automated fax system allows customers to receive the latest information or literature from Altera 24 hours a day, 7 days a week. Customers who wish to order documents or catalogs, should simply dial the appropriate number and follow the instructions. Customers in the United States or Canada can dial (800) 5-ALTERA; international customers can call (408) 894-7850 from a fax phone.

Electronic Mail

Customers can use electronic mail (e-mail) to send technical questions about devices and software to Altera Applications at **sos@altera.com**. Altera e-mail is checked regularly throughout the day and is given the same priority as telephone calls. However, since e-mail delivery through the Internet can be delayed, either the technical support hotline or fax should be used for urgent issues.

Bulletin Board Service

Altera maintains a 24-hour bulletin board service (BBS) for instant access to the latest Altera product information. On-line versions of Altera application notes and briefs, recent quarterly newsletters, and software utility programs are available from the BBS. The BBS can also be used to transfer files to and from the Altera Applications Department for technical support and review.

The telephone number for the BBS is (408) 954-0104. To connect to the BBS via modem, the following equipment and configuration is required:

- Bell Standard 212A, CCITT standard, or compatible modem
- Up to 14,400 baud rate
- 8 data bits, 1 stop bit, no parity

The following file transfer protocols are supported:

- ASCII (Non-Binary)
- Xmodem (Checksum)
- Xmodem (CRC)
- 1K-Xmodem
- Ymodem (Batch U/L and D/L)
- Zmodem (Batch U/L and D/L)
- Kermit

Altera FTP Site

Altera provides a 24-hour file transfer protocol (FTP) site for instant Internet access to the latest Altera product information. On-line versions of Altera application notes, application briefs, recent quarterly newsletters, and software utilities are available at **ftp.altera.com**. Customers can also use the FTP site to transfer design files to and from the Altera Applications Department for technical support and review.

CompuServe

Altera provides CompuServe support through the "Altera Forum." Customers can use the Altera Forum library to upload and download files, leave messages for other users or for Altera Applications, or hold real-time interactive conferences. CompuServe provides a free introductory membership to each Altera customer. To access the Altera Forum, customers can type `go altera` ↵ at the CompuServe command prompt.

World-Wide Web Site

Altera provides a world-wide web (WWW) site for instant access to Altera product information. The site provides an on-line hypertext environment that allows customers to browse through Altera product information, press releases, corporate profile, and employment opportunities. Contact the Altera Applications Department at (800) 800-EPLD for more information.

Training Courses

Altera provides a variety of training courses that teach customers innovative and efficient design techniques. With these courses, customers can discover the time-saving features of Altera's comprehensive MAX+PLUS II development system, explore the design features of Altera's device families, or simply learn more about Altera products.

Altera training courses are taught by Altera Application Engineers who work with Altera products every day. Small class sizes ensure that every student receives individual attention. Hands-on exercises with Altera devices and MAX+PLUS II software reinforce lecture topics to maximize learning.

Altera's training program is divided into multiple courses that focus on various aspects of the Altera design environment. Course topics range from introductory programmable logic design to advanced architecture and design labs. Training courses are offered on a regular basis at locations throughout the world. On-site training is also available. For more information about Altera's training courses, customers can contact their local Sales Representative or the Altera Training Administrator at (408) 894-7000.

Design Evaluations

Altera Application Engineers and Field Application Engineers can evaluate customer designs and recommend the most efficient design methods and the device(s) that will best fit customer needs. Altera will also estimate device performance. For more information, customers can contact their local Altera sales office.

On-Site Support

Altera Field Application Engineers are located around the world to provide on-site technical support. They are available to evaluate customer designs, demonstrate MAX+PLUS II software, and provide on-site training. Customers can contact their local Field Application Engineer by calling their local Altera sales office.

Notes:

Sales Offices, Distributors & Representatives

March 1995

Altera North American Regional Offices

NORTHERN CALIFORNIA
Altera Corporation
2610 Orchard Parkway
San Jose, CA 95134-2020
TEL: (408) 894-7900
FAX: (408) 428-0463

Altera Bay Area Sales
2290 North First Street, #212
San Jose, CA 95134
TEL: (408) 894-7900
FAX: (408) 428-0463

SOUTHERN CALIFORNIA
Altera Corporation
15375 Barranca Parkway
Suite B-201
Irvine, CA 92718
TEL: (714) 450-0262
FAX: (714) 450-0263

Altera Corporation
11500 West Olympic Boulevard
Suite 400
Los Angeles, CA 90064
TEL: (310) 312-4507
FAX: (310) 312-4508

COLORADO
Altera Corporation
Denver Technology Center
7900 East Union Avenue, #1100
Denver, CO 80237
TEL: (303) 694-5352
FAX: (303) 694-5351

GEORGIA
Altera Corporation
9755 Dogwood Road
Suite 350
Roswell, GA 30075
TEL: (404) 594-7621
FAX: (404) 518-9167

ILLINOIS
Altera Corporation
150 N. Martingale Road, Suite 838
Schaumburg, IL 60173
TEL: (708) 240-0313
FAX: (708) 240-0266

MARYLAND
Altera Corporation
5513 Twin Knolls Road, Suite 220
Columbia, MD 21045
TEL: (410) 992-0110
FAX: (410) 964-3364

MASSACHUSETTS
Altera Corporation
238 Littleton Road
Suite 204
Westford, MA 01886
TEL: (508) 392-1100
FAX: (508) 392-1157

NEW JERSEY
Altera Corporation
575 State Highway 28
Raritan, NJ 08869
TEL: (908) 526-9400
FAX: (908) 526-5471

NORTH CAROLINA
Altera Corporation
4601 Six Forks Road, Suite 500
Raleigh, NC 27609
TEL: (919) 787-3630
FAX: (919) 787-3599

OHIO
Altera Corporation
7784 Reynolds Road
Mentor, OH 44060
TEL: (216) 946-8211
FAX: (216) 946-9411

TEXAS
Altera Corporation
5080 Spectrum Drive, Suite 812W
Dallas, TX 75248
TEL: (214) 701-2330
FAX: (214) 701-2331

Altera Corporation
9430 Research Blvd.
Echelon IV, Suite 400
Austin, TX 78759
TEL: (512) 343-4542
FAX: (512) 418-1186

ONTARIO
Altera Corporation
300 March Road, Suite 601B
Kanata, Ontario K2K 2E2
Canada
TEL: (613) 599-3141
FAX: (613) 599-3143

Altera International Sales Offices

UNITED STATES
(CORPORATE HEADQUARTERS)
Altera Corporation
2610 Orchard Parkway
San Jose, CA 95134-2020
USA
TEL: (408) 894-7000
TLX: 888496
FAX: (408) 433-3943

UNITED KINGDOM
(EUROPEAN HEADQUARTERS)
Altera U.K. Limited
Solar House
Globe Park, Fieldhouse Lane
Marlow, Bucks SL7 ITB
England
TEL: (44) 1628 488-800
FAX: (44) 1628 890-078

FRANCE
Altera France
Le Mermoz-13
Avenue Morane Saulnier
78140 Velizy
France
TEL: (33) 1 34 63-0750
FAX: (33) 1 34 63-0751

GERMANY
Altera GmbH
Max-Planck-Straße 5
D-85716 Unterschleissheim
Germany
TEL: (49) 89/3218250
FAX: (49) 89/32182579

KOREA
Altera Korea
Sin Song Building, Suite 1501
25-4 Yoido-dong, Youngdeungpo-ku
Seoul
Korea
TEL: (82) 2-785-6895
FAX: (82) 2-785-6898

ITALY
Altera Italia
Corso Lombardia 75
Autoporto Pescarito
10099 San Mauro
Torinese (Torino)
Italy
TEL: (39) 11 223 8588
FAX: (39) 11 223 8589

JAPAN
Altera Japan Ltd.
Dai Tokyo Kasai Shinjuku Bldg.
3-25-3 Yoyogi Shibuya-ku
Tokyo 151
Japan
TEL: (81) 3-3375-2281
FAX: (81) 3-3375-2287

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U.S. Sales Representatives

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Huntsville, AL 35816
TEL: (205) 721-1788
FAX: (205) 721-1789

ARIZONA
Oasis Sales, Inc.
301 E. Bethany Home Road #A135
Phoenix, AZ 85012
TEL: (602) 277-2714
FAX: (602) 263-9352

ARKANSAS
Technical Marketing, Inc.
3320 Wiley Post Road
Carrollton, TX 75006
TEL: (214) 387-3601
FAX: (214) 387-3605

CALIFORNIA
Addem
1015 Chestnut Street #F2
Carlsbad, CA 92008
TEL: (619) 729-9216
FAX: (619) 729-6408

Altera Corporation
2610 Orchard Parkway
San Jose, CA 95134-2020
TEL: (408) 894-7900
FAX: (408) 428-0463

Infinity Sales
20 Corporate Park, Suite 100
Irvine, CA 92714
TEL: (714) 833-0300
FAX: (714) 833-0303

CALIFORNIA *(continued)*
Sierra Technical Sales
23566 Woodhaven Place
Auburn, CA 95602
TEL: (916) 268-3357
FAX: (916) 268-0192

COLORADO
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Englewood, CO 80111
TEL: (303) 721-9663
FAX: (303) 721-0195

CONNECTICUT
Datcom
One Evergreen Avenue
Hamden, CT 06518
TEL: (203) 288-7005
FAX: (203) 281-4233

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BGR Associates
Evesham Commons
525 Route 73, Suite 100
Marlton, NJ 08053
TEL: (609) 983-1020
FAX: (609) 983-1879

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Robert Electronic Sales
5525 Twin Knolls Road, Suite 325
Columbia, MD 21045
TEL: (410) 995-1900
FAX: (410) 964-3364

FLORIDA
Marathon Technical Associates
111 Granada Court
Orlando, FL 32803
TEL: (407) 872-5775
FAX: (407) 872-0535

Marathon Technical Associates
600 Bypass Drive, Suite 208
Clearwater, FL 34624
TEL: (813) 725-3199
FAX: (813) 726-5766

Marathon Technical Associates
4699 North Federal Highway, Suite 107
Pompano Beach, FL 33064
TEL: (305) 785-0072
FAX: (305) 782-7090

GEORGIA
EnVision, Inc.
3220 Pointe Parkway, Suite 1400
Norcross, GA 30092
TEL: (404) 840-1055
FAX: (404) 840-1048

IDAHO
Compass Marketing and Sales, Inc.
5 Triad Center, Suite 320
Salt Lake City, UT 84180
TEL: (801) 322-0391
FAX: (801) 322-0392

IDAHO *(continued)*
Phase II Technical Sales
550 Kirkland Way, Suite 100
Kirkland, WA 98033
TEL: (206) 828-8182
FAX: (206) 828-7472

ILLINOIS
AEM, Inc.
11520 St. Charles Rock Road, Suite 131
Bridgeton, MO 63044
TEL: (314) 298-9900
FAX: (314) 298-8660

Oasis Sales Corporation
1101 Tonne Road
Elk Grove Village, IL 60007
TEL: (708) 640-1850
FAX: (708) 640-9432

INDIANA
Electro Reps, Inc.
7240 Shadeland Station, Suite 275
Indianapolis, IN 46256
TEL: (317) 842-7202
FAX: (317) 841-0230

Electro Reps, Inc.
125 Airport North Office Park
Fort Wayne, IN 46825
TEL: (219) 489-8205
FAX: (219) 489-8408

IOWA
AEM, Inc.
4001 Shady Oak Drive
Marion, IA 52302
TEL: (319) 377-1129
FAX: (319) 377-1539

KANSAS
AEM, Inc.
9716 Rosehill Road
Lenexa, KS 66215
TEL: (913) 888-0022
FAX: (913) 888-4848

KENTUCKY
Electro Reps, Inc.
7240 Shadeland Station, Suite 275
Indianapolis, IN 46256
TEL: (317) 842-7202
FAX: (317) 841-0230

The Lyons Corporation
4812 Frederick Road, Suite 101
Dayton, OH 45414
TEL: (513) 278-0714
FAX: (513) 278-3609

LOUISIANA
Technical Marketing, Inc.
2901 Wilcrest Drive, Suite 139
Houston, TX 77042
TEL: (713) 783-4497
FAX: (713) 783-5307

U.S. Sales Representatives

(continued)

MAINE
Altera Corporation
238 Littleton Road, Suite 204
Westford, MA 01886
TEL: (508) 392-1100
FAX: (508) 392-1157

MARYLAND
Robert Electronic Sales
5525 Twin Knolls Road, Suite 325
Columbia, MD 21045
TEL: (410) 995-1900
FAX: (410) 964-3364

MASSACHUSETTS
Altera Corporation
238 Littleton Road, Suite 204
Westford, MA 01886
TEL: (508) 392-1100
FAX: (508) 392-1157

Datcom
One Evergreen Avenue
Hamden, CT 06518
TEL: (203) 288-7005
FAX: (203) 281-4233

MICHIGAN
Rathsburg Associates, Inc.
41100 Bridge Street
Novi, MI 48375
TEL: (810) 615-4000
FAX: (810) 615-4001

MINNESOTA
Cahill, Schmitz & Cahill, Inc.
315 N. Pierce
St. Paul, MN 55104
TEL: (612) 646-7217
FAX: (612) 646-4484

MISSISSIPPI
EnVision, Inc.
1009 Henderson Road, Suite 400B
Huntsville, AL 35816
TEL: (205) 721-1788
FAX: (205) 721-1789

MISSOURI
AEM, Inc.
11520 St. Charles Rock Road, Suite 131
Bridgeton, MO 63044
TEL: (314) 298-9900
FAX: (314) 298-8660

MONTANA
Compass Marketing and Sales, Inc.
5 Triad Center, Suite 320
Salt Lake City, UT 84180
TEL: (801) 322-0391
FAX: (801) 322-0392

NEBRASKA
AEM, Inc.
4001 Shady Oak Drive
Marion, IA 52302
TEL: (319) 377-1129
FAX: (319) 377-1539

NEVADA
Oasis Sales, Inc.
301 E. Bethany Home Road #A135
Phoenix, AZ 85012
TEL: (602) 277-2714
FAX: (602) 263-9352

Sierra Technical Sales
23566 Woodhaven Place
Auburn, CA 95602
TEL: (916) 268-3357
FAX: (916) 268-0192

NEW HAMPSHIRE
Altera Corporation
238 Littleton Road, Suite 204
Westford, MA 01886
TEL: (508) 392-1100
FAX: (508) 392-1157

NEW JERSEY
BGR Associates
Evesham Commons
525 Route 73, Suite 100
Marlton, NJ 08053
TEL: (609) 983-1020
FAX: (609) 983-1879

ERA, Inc.
354 Veterans Memorial Highway
Commack, NY 11725
TEL: (516) 543-0510
FAX: (516) 543-0758

NEW MEXICO
Nelco Electronix
3240 C Juan Tabo Boulevard NE
Albuquerque, NM 87111
TEL: (505) 293-1399
FAX: (505) 293-1011

NEW YORK
ERA, Inc.
354 Veterans Memorial Highway
Commack, NY 11725
TEL: (516) 543-0510
FAX: (516) 543-0758

Technology Sales, Inc.
920 Perinton Hills Office Park
Fairport, NY 14450
TEL: (716) 223-7500
FAX: (716) 223-5526

NORTH CAROLINA
EnVision, Inc.
3200 Wake Forest Road, Suite 205
Raleigh, NC 27609
TEL: (919) 878-3080
FAX: (919) 878-3090

NORTH DAKOTA
Cahill, Schmitz & Cahill, Inc.
315 North Pierce Road
St. Paul, MN 55104
TEL: (612) 646-7217
FAX: (612) 646-4484

OHIO
The Lyons Corporation
4812 Frederick Road, Suite 101
Dayton, OH 45414
TEL: (513) 278-0714
FAX: (513) 278-3609

The Lyons Corporation
4615 W. Streetsboro Road
Richfield, OH 44286
TEL: (216) 659-9224
FAX: (216) 659-9227

The Lyons Corporation
248 N. State Street
Westerville, OH 43081
TEL: (614) 895-1447
FAX: (513) 278-3609

OKLAHOMA
Technical Marketing, Inc.
3320 Wiley Post Road
Carrollton, TX 75006
TEL: (214) 387-3601
FAX: (214) 387-3605

OREGON
Phase II Technical Sales
4900 SW Griffith Drive, Suite 110
Beaverton, OR 97005
TEL: (503) 643-6455
FAX: (503) 626-7442

PENNSYLVANIA
BGR Associates
Evesham Commons
525 Route 73, Suite 100
Marlton, NJ 08053
TEL: (609) 983-1020
FAX: (609) 983-1879

The Lyons Corporation
248 N. State Street
Westerville, OH 43081
TEL: (614) 895-1447
FAX: (513) 278-3609

RHODE ISLAND
Altera Corporation
238 Littleton Road, Suite 204
Westford, MA 01886
TEL: (508) 392-1100
FAX: (508) 392-1157

SOUTH CAROLINA
EnVision, Inc.
113 Stonegate Drive
Columbia, SC 29223
TEL: (803) 699-3360
FAX: (803) 699-0377

SOUTH DAKOTA
Cahill, Schmitz & Cahill, Inc.
315 North Pierce Road
St. Paul, MN 55104
TEL: (612) 646-7217
FAX: (612) 646-4484

TENNESSEE
EnVision, Inc.
8120 Sawyer Brown Road, Suite 105
Nashville, TN 37221
TEL: (615) 622-7666
FAX: (615) 622-7652

TEXAS
Technical Marketing, Inc.
3701 Executive Center Drive #205
Austin, TX 78731
TEL: (512) 343-6976
FAX: (512) 343-7986

Technical Marketing, Inc.
3320 Wiley Post Road
Carrollton, TX 75006
TEL: (214) 387-3601
FAX: (214) 387-3605

Technical Marketing, Inc.
2901 Wilcrest Drive, Suite 139
Houston, TX 77042
TEL: (713) 783-4497
FAX: (713) 783-5307

UTAH
Compass Marketing and Sales, Inc.
5 Triad Center, Suite 320
Salt Lake City, UT 84180
TEL: (801) 322-0391
FAX: (801) 322-0392

VERMONT
Altera Corporation
238 Littleton Road, Suite 204
Westford, MA 01886
TEL: (508) 392-1100
FAX: (508) 392-1157

VIRGINIA
Robert Electronic Sales
5525 Twin Knolls Road, Suite 325
Columbia, MD 21045
TEL: (410) 995-1900
FAX: (410) 964-3364

WASHINGTON
Phase II Technical Sales
550 Kirkland Way
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TEL: (604) 294-2000
FAX: (604) 294-4585

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Mississauga, Ontario L4Z 3E6
Canada
TEL: (905) 507-6400
FAX: (905) 507-6444

ONTARIO *(continued)*
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Kanata, Ontario K2K 2E2
Canada
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FAX: (613) 564-0087

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FAX: (514) 745-5858

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1077 Buenos Aires
Argentina
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FAX: (54) 1-476-2551

AUSTRALIA
Veltek Pty. Ltd.
18 Harker St.
Burwood, Victoria 3125
Australia
TEL: (61) 3-808-7511
FAX: (61) 3-808-5473

AUSTRIA
Eurodis Electronics GmbH
A-1232 Wien
Lamezanstraße 10
Austria
TEL: (43) 1-610620
TLX: (847) 134404 (HIT)
FAX: (43) 1-61062151

BRAZIL
União Digital Ltda.
Rua Georgia 69
04559-010
São Paulo - SP
Brazil
TEL: (55) 11 533-0967
FAX: (55) 11 533-6780

BELGIUM
D&D Electronics
Vlle Olympiadelaan 93
B-2020 Antwerpen
Belgium
TEL: (32) 3-827-7934
TLX: (846) 73121 (DDELEC BU)
FAX: (32) 3-828-7254

CHINA
CIDC
No. 1, Gao Jia Yuan
Dong Zhi Men Wai, Chao Yang Qu
Beijing 100015
People's Republic of China
TEL: (86) 1-436-0987
FAX: (86) 1-436-4487

Lestina International, Ltd.
Room 2301, Tower 1
14 Wang Hua Road
Guangzhou 510053
People's Republic of China
TEL: (86) 20-380-7307
FAX: (86) 20-380-7307

Lestina International, Ltd.
Room 20404 Friendship Hotel
No. 3 Bai Shi Qiao Road
Bejing 100873
People's Republic of China
TEL: (86) 1-849-9430 (ext. 20404)
FAX: (86) 1-849-9430

CHINA *(continued)*
Lestina International, Ltd.
No. 3-1 Fuxing Bridge, Houzai Door
Nanjing 210016
People's Republic of China
TEL: (86) 25-449-1384
FAX: (86) 25-449-1384

DENMARK
E.V. Johanssen Elektronik
Titangade 15
DK-2200 Koebenhavn N
Denmark
TEL: (45) 31 83 90 22
TLX: (855) 16522 (EVICAS DK)
FAX: (45) 31 83 92 22

Rep Delco Sweden AB
Kemistvägen 10
Box 516, S-183 25 Täby
TEL: (45) 31 839-022
FAX: (45) 35 821-205

FINLAND
Bexab Finland OY
Asemakuja 2A
Fin-02770 Espoo
Finland
TEL: (358) 0-502-3200
FAX: (358) 0-502-3294

FRANCE
Arrow Electronique S.A.
73-79, Rue des Solets
Silic 585
94663 Rungis Cédex
France
TEL: (33) 1 49 784978
FAX: (33) 1 49 780596

Tekelec Airtronic SA
Cité des Bruyères
Rue Carle Vernet
92310 Sèvres
France
TEL: (33) 1 46 23 24 25
TLX: (842) 634018 (TKLEC AF)
FAX: (33) 1 45 07 21 91

GERMANY
Avnet E2000 GmbH
Elektronische Bauelemente
Stahlgruberring 12
D-81829 München
Germany
TEL: (49) 89/45110-01
TLX: (841) 522561 (ELEC D)
FAX: (49) 89/45110-129

Jermyn GmbH
Im Dachsstüeck 9
65549 Limburg
Germany
TEL: (49) 64 31 508 0
FAX: (49) 64 31 508 289

GERMANY *(continued)*
SASCO GmbH
Hermann-Oberth-Straße 16
D-85640 Putzbrunn
Germany
TEL: (49) 89/46110
FAX: (49) 89/4611270

GREECE
Pouliadis Associates Corporation
Aristotelous Street 3
Sygrou Avenue 150
Athens 17671
Greece
TEL: (30) 1 924-2072
FAX: (30) 1 924-1066

HOLLAND
Koning en Hartman
1 Energieweg
2627 AP Delft
The Netherlands
TEL: (31) 15 609-906
FAX: (31) 15 619-194

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Lestina International Ltd.
14/F Park Tower, 15 Austin Road
Tsimshatsui, Kowloon
Hong Kong
TEL: (852) 2735-1736
FAX: (852) 2730-5260

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Sritech Information Technology Ltd.
744/51, 2nd Floor, Chintal Plaza
33rd Cross, 10th Main
4th Block, Jayanagar
Bangalore 560 011
India
TEL: (91) 80-6-640-661
TLX: (953) 08458162 (SRIS IN)
FAX: (91) 80-6-633-508

ISRAEL
Eastronics, Ltd.
11 Rozanis Street
P.O. Box 39300
Tel-Aviv 61392
Israel
TEL: (972) 36 458-777
FAX: (972) 36 458-666

Newtronix Systems, Inc.
151 Fairchild Avenue
Plainview, NY 11803
USA
TEL: (516) 349-9890
FAX: (516) 349-9618

ITALY
Lasi Elettronica Div. Silverstar Ltd. S.P.A.
Viale Fulvio Testi, 280
20126 Milano
Italy
TEL: (39) 2 661 431
FAX: (39) 2 661 01385

International Distributors

(continued)

JAPAN
Altima Corporation
Hakusan High-Tech Park
1-22-2 Hakusan, Midori-Ku
Yokohama City 226
Japan
TEL: (81) 45-939-6113
FAX: (81) 45-939-6114

Altima Corporation
Astoro Shin-Osaka Daini Building 7F
6-1-3 Nishi-Nakagima
Yodogawa-ku Osaka City
Osaka 532
Japan
TEL: (81) 6-396-0817
FAX: (81) 6-307-7671

Paltek Corporation
1-3-3 Azamino-Minami
Aoba-Ku, Yokohama City
Kanagawa-Ken, 225
Japan
TEL: (81) 45-910-1381
TLX: (781) 02425205 (PALTEK J)
FAX: (81) 45-910-1390

Paltek Corporation
Recruit Shin Osaka Building
5-14-22 Nishi Nakamiga
Yodogawa-ku, Osaka City
Osaka 532
Japan
TEL: (81) 6-390-0818
FAX: (81) 6-303-3181

KOREA
MJL Korea, Ltd.
Hahntoo New Building, 19/F
27-1 Yeouido-Dong
Yungdeungpo-Ku
Seoul 150-010
Korea
TEL: (82) 2-767-2200
FAX: (82) 2-767-2221

Segyung Techell Company, Ltd.
Nonhyun Dansan Bldg.
270-45, Nonhyun-Dong, Kang-Nam-Gu
Seoul 135-012 Korea
TEL: (82) 2-515-7477
FAX: (82) 2-515-8889

LATIN AMERICA
Intectra, Inc.
2629 Terminal Blvd.
Mountain View, CA 94043
USA
TEL: (415) 967-8818
TLX: 345545 (INTECTRA MTNV)
FAX: (415) 967-8836

NETHERLANDS
Koning en Hartman
1 Energieweg
2627 AP Delft
Netherlands
TEL: (31) 15 609906
TLX: 38250 (KOHA NL)
FAX: (31) 15 619194

NORWAY
ScandComp Norway AS
Nils Hansens vei 3
N-0667 OSLO
TEL: (47) 2272 4045
FAX: (47) 2272-4059

RUSSIA
EFO, Ltd.
Chudnovskogo Str., 8-1-542
St. Petersburg
193318 Russia
TEL: (7) 812 247-0900
(7) 812 247-8158
FAX: (7) 812 247-5340

JSC "Gamma"
Nekrasova Str., 19
Vyborg
188900 Russia
TEL: (7) 812 78-25671
FAX: (7) 812 78-31509

New Technologies, Ltd.
20 Karl Marx Avenue
Novosibirsk
630099 Russia
TEL: (7) 383 2-460613
FAX: (7) 383 2-236973

"Tehno"
126 Pervomayskaya Str.
Moscow 105203
Russia
TEL: (7) 095 461-8775
FAX: (7) 095 965-1010
(7) 095 461-3514
(7) 095 965-1020
(7) 095 463-3537

SINGAPORE
Serial System Pte. Ltd.
11 Jalan Mesin
Standard Industrial Building #06-00
Singapore 1336
TEL: (65) 280-0200
FAX: (65) 286-1812

SPAIN
ATD Electronica, SA
Albasanz, 75
28037 Madrid
Spain
TEL: (34) 1-304-1534
FAX: (34) 1-327-2778

SOUTH AFRICA
Prime Source (Pty) Ltd.
3 Olympia Street
Marlboro, Sandton
P.O. Box 46169
Orange Grove 2119
Republic of South Africa
TEL: (27) 11-444-7237
FAX: (27) 11-444-7298

SWEDEN
Bexab Sweeden AB
P.O. Box 523
S-183 25 Taby
Sweden
TEL: (46) 8 630 8800
TLX: 149 32
FAX: (46) 8 732 7058

SWITZERLAND
Elbatex
Hardstraße 72
CH 5430 Wettingen
Switzerland
TEL: (41) 56 275-777
FAX: (41) 56 261-486

TAIWAN
Galaxy Far East Corp.
8F-6, 390 Sec. 1
Fu Hsing South Road
Taipei
Taiwan
People's Republic of China
TEL: (886) 2-705-7266
TLX: (785) 26110 (GALAXYER)
FAX: (886) 2-708-7901

THAILAND
Nu-Era Co. Ltd.
769/8 J.T. Building
Soisoonvijai 4/1
Rama 9 Road, Huaykwang
Bangkok 10310
Thailand
TEL: (66) 2-318-6453
FAX: (66) 2-318-6454

UKRAINE
Joint Stock Company
Kvazar-Micro Techno
Severo Syretskaya Str., 1
254136 Kiev
Ukraine
TEL: (7) 044 442-0046
(7) 044 442-9361
FAX: (7) 044 442-0046
(7) 044 442-9361

UNITED KINGDOM
Ambar-Cascom, Ltd.
The Gatehouse
Gatehouse Way
Aylesbury, Bucks
HP19 3DL
United Kingdom
TEL: (44) 1296 43-4141
FAX: (44) 1296 29-670

Thame Components, Ltd.
Thame Park Road
Thame
Oxon
OX9 3UQ
United Kingdom
TEL: (44) 1844 26-1188
FAX: (44) 1844 26-1681

Notes:

Glossary

March 1995

A

Altera Hardware Description Language (AHDL) Altera's design entry language. AHDL is completely integrated into MAX+PLUS II, and allows the designer to enter and edit Text Design Files (**.tdf**) with the MAX+PLUS II Text Editor or any standard text editor, then compile, simulate, and program projects within MAX+PLUS II. AHDL supports Boolean equation, state machine, conditional, and decode logic. AHDL also provides access to all Altera macrofunctions and LPMs.

array Clock A Clock signal that passes through the logic array of a device before arriving at the Clock input of a register.

Assembler The Compiler module that creates one or more Programmer Object Files (**.pof**), SRAM Object Files (**.sof**), and optional JEDEC Files (**.jed**) for programming Altera devices.

Assignment & Configuration File (.acf) An ASCII file that stores information about probe, resource, and device assignments for a hierarchy tree, as well as configuration information for the Compiler, Simulator, Timing Analyzer, and Programmer. All information that can affect output files containing design information for the current hierarchy tree is controlled by the ACF.

B

BBS Bulletin board service. An electronic bulletin board service that provides continuous access to up-to-date device and development tool information, electronic application notes and briefs, data sheet updates, customer newsletters, and software utility programs. The Altera BBS supports baud rates of 1200, 2400, 4800, 9600, and 14400.

BGA Ball-grid array. A device package offered by Altera. See *Altera Device Package Outlines* and *Ordering Information* in this data book for more information.

BitBlaster A cable that allows both PC and workstation users to configure a FLEX 8000 device in a prototype system. The BitBlaster also allows PC users to program a MAX 9000 device in-system. This capability functions independently from the MAX+PLUS II Programmer or any other programming hardware. The Altera BitBlaster connects a standard RS-232 serial port on a PC or workstation to a single target FLEX 8000 or MAX 9000 device in a prototype system.

C

carry chain A dedicated architectural feature of the FLEX 10K and FLEX 8000 families that provides a high-performance carry-forward function between logic elements. The carry-in signal from a lower-order bit moves forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This carry-forward function is ideal for adders, counters, and comparators.

cascade chain A dedicated architectural feature of the FLEX 10K and FLEX 8000 families that allows implementation of high-performance, wide fan-in functions. Adjacent LUTs can be used to compute portions of a function in parallel; the cascade chain serially

connects the intermediate values. The cascade chain is available only in FLEX 10K and FLEX 8000 devices.

CerDIP Ceramic dual in-line package. A device package offered by Altera. See *Altera Device Package Outlines* and *Ordering Information* in this data book for more information.

Classic An Altera device family based on Altera's original EPROM-based EPLD architecture. The devices discussed in this data book include the EP610, EP610I, EP910, EP910I, EP1810, EP22V10, and EP22V10E devices. Other Classic device family mambers include the EP220, EP224, EP312, EP324, and EP330 devices.

Compiler Netlist Extractor The MAX+PLUS II Compiler module that converts each design file in a project—created with the schematic, text, or waveform editors, or with industry-standard EDA software—to a single database format. The Compiler Netlist Extractor also checks each design file in a project for problems such as duplicate node names, missing inputs and outputs, and outputs that are tied together.

Configuration EPROM A serial EPROM supplied by Altera for configuring FLEX 10K and FLEX 8000 devices. This device family includes the EPC1064, EPC1064V, and EPC1213.

configuration scheme The method used to load data into a FLEX 8000 device. Six configuration schemes are available:

- Active serial (AS)
- Active parallel up (APU)
- Active parallel down (APD)
- Passive parallel asynchronous (PPA)
- Passive parallel synchronous (PPS)
- Passive serial (PS)

For complete information on FLEX 8000 configuration schemes, see *Application Note 33 (Configuring FLEX 8000 Devices)* and *Application Note 38 (Configuring Multiple FLEX 8000 Devices)*.

continuity checking A test for open circuits between device pins and programming adapter sockets. This test verifies that a device is properly seated in the socket of the adapter.

CQFP Ceramic quad flat pack. A device package offered by Altera. See *Altera Device Package Outlines* and *Ordering Information* in this data book for more information.

D

Database Builder The MAX+PLUS II Compiler module that builds a single, fully flattened database that integrates all files in a project hierarchy. It also examines the logical completeness and consistency of the project and checks for boundary connectivity and syntactical errors.

dedicated input pin A pin that can only be used as an input to the device.

Design Doctor The Compiler utility that checks each design file in a project for poor design practices that may cause reliability problems when the project is implemented in one or more devices.

development socket A prototyping socket for high-pin-count QFP packages.

device An Altera programmable logic device, including FLEX 10K, FLEX 8000, MAX 9000, MAX 7000, FLASHlogic, MAX 5000, Classic, and Configuration EPROM devices.

device family A group of Altera programmable logic devices with the same fundamental architecture. Altera device families are the FLEX 10K, FLEX 8000, MAX 9000, MAX 7000, FLASHlogic,

MAX 5000, Classic, and Configuration EPROM families.

DIP Dual in-line package. A device package offered by Altera. See *Altera Device Package Outlines* and *Ordering Information* in this data book for more information. Ceramic (CerDIP) and plastic (PDIP) versions are available.

E

EDIF Electronic Design Interchange Format. An industry-standard format for transmitting design data. An EDIF 2 0 0 or 3 0 0 netlist file can be generated from a schematic, VHDL, or Verilog HDL design that has been processed with an industry-standard synthesis tool and then imported into MAX+PLUS II as an EDIF Input File (**.edf**). The MAX+PLUS II Compiler can also generate one or more EDIF Output Files (**.edo**) in EDIF 2 0 0 or 3 0 0 format that contain functional and timing information for simulation with a standard EDIF simulator.

EDIF Input File (.edf) An EDIF version 2 0 0 or 3 0 0 netlist file generated by any industry-standard EDIF netlist writer.

EDIF Output File (.edo) An EDIF version 2 0 0 or 3 0 0 netlist file generated by the EDIF Netlist Writer module of the MAX+PLUS II Compiler.

EDIF Netlist Reader The Compiler module that creates one or more EDIF Output Files.

EDIF Netlist Writer The portion of the Compiler Netlist Extractor module that converts an one or more EDIF Input File (.edf) generated with other industry-standard CAE tools into a MAX+PLUS II-compatible format.

EEPROM Electrically erasable programmable read-only memory. A form of reprogrammable semiconductor memory whose contents can be erased by subjecting the device to appropriate electrical signals. See *Operating Requirements for Altera Devices* and *Configuration Elements & Reliability* in this data book for more information.

EPLD Erasable programmable logic device, i.e., an Altera device that is a member of the MAX 9000, MAX 7000, FLASHlogic, MAX 5000, or Classic family.

EPROM Erasable programmable read-only memory. A form of reprogrammable semiconductor memory, the contents of which can be erased by subjecting the device to ultraviolet light of the proper wavelength. See *Operating Requirements for Altera Devices* and *Configuration Elements & Reliability* in this data book for more information.

expander product term A single product term with an inverted output that feeds back into the Logic Array Block (LAB) of a MAX 9000, MAX 7000, or MAX 5000 device. An uncommitted expander product term that can be shared with other logic cells in the same LAB is called a shareable expander; a product term that has been shared in this manner is called a shared expander. In MAX 9000 and MAX 7000 devices, an expander product term borrowed from an adjacent logic cell in the same LAB is called a parallel expander.

external timing parameters Factory-tested, guaranteed worst-case values. Examples include t_{PD1}, t_{CO1}, and f_{CNT}. In this data book, external timing parameters are shown in bold type. In the *FLEX 8000 Programmable Logic Device Data Sheet*, external timing parameters are listed under "External Reference Timing Characteristics."

extraction tool A tool to extract QFP devices from QFP carriers. Extraction tools are available from Altera for 100-pin QFPs, 160- to 208-pin QFPs, 240-pin QFPs, and 304-pin QFPs. Refer to the *QFP Carrier & Development Socket Data Sheet* in this data book for information.

F

family-specific macrofunction A macrofunction provided by Altera that contains logic optimized for the architecture of a specific device family. The functionality of a family-specific macrofunction is always the same, regardless of the device family for which it is designed. However, primitives and nodes used within the macrofunction file can vary among families to take advantage of different device architectures, providing higher performance and more efficient implementation.

FastTrack Interconnect Dedicated connection paths that span the entire width and height of a FLEX 8000 or MAX 9000 device. These connection paths allow signals to travel between all Logic Array Blocks (LABs) in a device.

Fit File (.fit) An ASCII text file that records the pin, buried logic cell, chip, and device assignments for a MAX+PLUS II project. All external pin connections for a single-device project, which are needed for simulation and functional testing, are also recorded.

Fitter The MAX+PLUS II Compiler module that fits a project into one or more devices. The Fitter selects appropriate interconnection paths, as well as the pin and logic cell assignments. It also creates a Report File (**.rpt**) and Fit File (**.fit**) for the project.

FLASH A form of reprogrammable semiconductor memory, the contents of which can be erased by subjecting the device to appropriate electrical signals. See *Configuration Elements & Reliability* in this data book for more information.

FLASHlogic An Altera device family featuring SRAM-based devices with shadow EPROM or FLASH configuration elements. This family includes the EPX740, EPX780, EPX880, and EPX8160 devices.

FLEX Download Cable A cable used to download SRAM Object File (**.sof**) data in a passive serial (PS) configuration scheme to a FLEX 10K or FLEX 8000 device in-system. FLEX 10K and FLEX 8000 devices can be configured with the FLEX Download Cable to allow functional testing and prototyping on the circuit board.

FLEX 8000 An Altera device family based on Flexible Logic Element MatriX architecture. This SRAM-based family offers high-performance, register-intensive, high-gate-count devices. This family includes the EPF8282, EPF8282A, EPF8282V, EPF8282AV, EPF8452, EPF8452A, EPF8636A, EPF8820, EPF8820A, EPF81188, EPF81188A, EPF81500, and EPF81500A devices.

FLEX 10K An Altera device family based on the second-generation, Flexible Logic Element MatriX architecture. This SRAM-based family offers high-performance, register-intensive, high-gate-count devices, and is the programmable logic industry's first embedded-array device family. This family includes the EPF10K10, EPF10K20, EPF10K30, EPF10K40, EPF10K50, EPF10K70, and EPF10K100 devices.

flipflop An edge-triggered, clocked storage unit that stores a single bit of data. A low-to-high transition on the Clock signal changes the output of the flipflop based on the value of the data input(s). This value is maintained until the next low-to-high transition of the Clock, or until the flipflop is preset or cleared. Depending on the architecture of the device family, a register can be programmed as a level-sensitive flow-through latch or as an edge-triggered D, T, JK, or SR flipflop.

functional simulation A MAX+PLUS II Simulator mode that uses a functional Simulator Netlist File (**.snf**) to simulate the logical performance of a project without timing information.

Functional SNF Extractor The MAX+PLUS II Compiler module that creates the functional Simulator Netlist File (**.snf**) required for functional simulation.

G

Graphic Design File (.gdf) A binary file, created with the Graphic Editor, that contains a logic schematic. You can also save an OrCAD Schematic File as a GDF.

global Clear A signal from a dedicated input pin that does not pass through the logic array before arriving at the Clear input of a register. In FLEX 8000 devices, a global Clear can come from any of the dedicated inputs. MAX 9000 and MAX 7000 devices have input pins that can be used either as global Clear sources or dedicated inputs to the device.

global Clock A signal from a dedicated input pin that does not pass through the logic array before arriving at the Clock input of a register. In FLEX 8000 devices, a global Clock can come from any of the four dedicated input pins. MAX 9000, MAX 7000, MAX 5000, and EP1810 devices have input pins that can be used either as global Clock sources or dedicated inputs to the device. EP910 and EP610 devices have dedicated Clock input pins.

H

Hexadecimal (Intel-Format) File (.hex) A hexadecimal file in the Intel Hex format that stores configuration data for one or more FLEX 8000 devices that are configured from a parallel data source.

I

Include File (.inc) An ASCII text file that can be imported into a TDF with an AHDL Include Statement.

interconnect timing parameters Internal timing parameters for the interconnect in FLEX 8000 devices.

internal timing parameters Worst-case delays based on external timing parameters. Internal timing parameters cannot be measured explicitly, and should be used only for estimating device performance. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance. Examples include t_{LAD}, t_{CGEN}, and t_{CLR}. In this data book, internal timing parameters are shown in italics. In FLEX 8000 device data sheets, internal timing parameters are listed under "Internal Timing Characteristics," rather than "Internal Timing Parameters."

I/O cell A register that exists on the periphery of a FLEX 8000, FLEX 8000M, or MAX 9000 device, or a fast input-type logic cell that is associated with an I/O pin in a MAX 7000E or MAX 7000S device. I/O cells permit short set-up time. I/O cells are also known as I/O elements in FLEX 8000 devices.

I/O Cell Register A logic option that specifies that you wish to implement a register in an I/O cell on a FLEX 8000, FLEX 8000M, MAX 9000, MAX 7000S, or MAX 7000E device. This logic option can be applied to individual logic functions. However, it cannot be incorporated into a logic synthesis style or applied to an entire project. The MAX+PLUS II **Global Project Logic Synthesis** command includes an *Automatic I/O Cell Registers* option to allow the MAX+PLUS II Compiler to automatically implement appropriate logic functions in I/O cell registers.

J

JEDEC File (.jed) An ASCII file that contains programming information. JEDEC Files provide an industry-standard format for transferring information between a data

preparation system and a logic device programmer. The MAX+PLUS II Programmer can optionally save programming data in JEDEC File format and use a JEDEC File to program the following Classic Altera devices only: EP610, EP610I, EP910, EP910I, EP1810, and EP22V10 devices. The PLDshell Plus Compiler generates JEDEC Files for all FLASHlogic and Classic devices.

JED2JTAG A software utility used in conjunction with PLDshell Plus. JED2JTAG is used to download JEDEC Files to one or more FLASHlogic devices via the FLASHlogic Download Cable.

JLCC Ceramic J-lead chip carrier. A device package offered by Altera. See *Altera Device Package Outlines* and *Ordering Information* in this data book for more information.

JTAG Joint Test Action Group. A set of specifications that enables a designer to perform board- and device-level functional verification of a board during production.

JTAG boundary-scan testing Testing that isolates a device's internal circuitry from its I/O circuitry. This testing is made possible by the Joint Test Action Group (JTAG) boundary-scan test (BST) architecture that is available in FLEX 10K, FLEX 8000, MAX 9000, MAX 7000S, and FLASHlogic devices. Boundary-scan testing offers efficient PC board testing, providing an electronic substitute for the traditional "bed of nails" test fixture.

L

Library Mapping File (.lmf) An ASCII text file that maps cells in EDIF Input Files or symbols in OrCAD Schematic Files to equivalent MAX+PLUS II primitives and macrofunctions.

library of parameterized modules (LPM) An architecture-independent library of logic functions. The LPM standard is built upon and follows the syntax of the EDIF 3 0 0 standard. LPM functions support architecture-independent design entry for all Altera devices. The MAX+PLUS II Compiler includes built-in compilation support for LPM functions.

linked simulation A MAX+PLUS II Simulator mode that uses a linked Simulator Netlist File (**.snf**) to simulate the logical performance of a project consisting of multiple, linked individual projects. A linked simulation uses the timing and/or functional netlist information from the combined SNFs of these individual projects.

Linked SNF Extractor The MAX+PLUS II Compiler module that creates the linked Simulator Netlist File (**.snf**) required for multi-project simulation.

Logic Array Block (LAB) A physically grouped set of logic resources in an Altera device. The LAB consists of a logic cell array and, in some device families, an expander product term array. Any signal that is available to any one logic cell in the LAB is available to the entire LAB. In FLEX 8000 and MAX 9000 devices, the LAB is fed by row interconnect paths and a dedicated input bus. In MAX 7000, FLASHlogic, and MAX 5000 devices, the LAB is fed by a Programmable Interconnect Array (PIA) and a dedicated input bus. In Classic devices, the logic in the LAB shares a global Clock signal. The LAB is fed by a global bus and a dedicated input bus. (In the EP1810, an LAB is called a quadrant.)

LPM *See* library of parameterized modules (LPM).

logic cell The generic term for the basic building block of an Altera general-purpose logic device. In EPLDs (MAX 9000, MAX 7000, FLASHlogic, MAX 5000, and Classic devices), the logic cell is called a macrocell. In FLEX 10K and FLEX 8000 devices, the logic cell is called a logic element.

logic element (LE) A basic building block of an Altera FLEX 10K or FLEX 8000 device. A logic element consists of a look-up table (LUT)—i.e., a function generator that quickly computes any function of four variables—and a programmable register to support sequential functions. The register can be programmed to emulate a flow-through latch or a D, T, JK, or SR flipflop, or it can be bypassed entirely for combinatorial logic. The register can feed other logic elements or feed back to the logic element itself. Some logic elements feed output or bidirectional I/O pins on the device.

logic element timing parameters Internal timing parameters for the logic elements in FLEX 8000 devices.

Logic Programmer card The LP6 expansion card required to run the MAX+PLUS II Programmer and program Altera devices from a PC.

Logic Synthesizer The Compiler module that uses several algorithms to minimize gate count, remove redundant logic, and utilize the device architecture as efficiently as possible.

look-up table (LUT) A function that generates outputs based on inputs and a set of stored data. The logic element of FLEX 8000 devices includes a four-input LUT that can be configured to emulate any logical function of four inputs.

M

macrocell The basic building block in Altera MAX 9000, MAX 7000, FLASHlogic, MAX 5000, and Classic devices. A macrocell consists of two parts: combinatorial logic and a programmable register. The combinatorial logic allows a wide variety of logic functions. Depending on the architecture of the device family, the register can be programmed to emulate a flow-through latch; a D, T, JK, or SR flipflop; or it can be bypassed entirely for pure combinatorial logic. The register can feed other macrocells or feed back to its own macrocell. Some macrocells feed output or bidirectional I/O pins on the device. Macrocells in FLEX 10K and FLEX 8000 devices are called logic elements.

macrofunction A high-level building block used together with gate and flipflop primitives in MAX+PLUS II design files, or, in general, a lower-level design file in a MAX+PLUS II hierarchical project.

Master Programming Unit (MPU) A logic device programming box. The MPU works with zero-insertion-force sockets and individual adapters to program and test Altera devices. The PL-MPU base unit and adapters with the prefix "PLM" support both device programming and device testing. The PLE3-12A unit and other adapters (i.e., adapters with the prefix "PLE" and the PLAD3-12 adapter) support device programming only.

MAX 5000 An Altera device family based on the first generation of Multiple Array MatriX architecture. This EPROM-based device family includes EPM5032, EPM5032A, EPM5064, EPM5064A, EPM5128, EPM5128A, EPM5130, EPM5130A, EPM5192, and EPM5192A devices.

MAX 7000 An Altera device family based on the second generation of Multiple Array MatriX architecture. Enhanced MAX 7000E devices offer up to six pin- or logic-driven Output Enable signals, fast input setup times, and two global Clocks with optional inversion. MAX 7000S devices feature ISP and JTAG BST circuitry. These EEPROM-based devices include EPM7032, EPM7032S, EPM7032V, EPM7064, EPM7064S, EPM7096, EPM7096S, EPM7128E, EPM7128S, EPM7160E, EPM7160S, EPM7192E, EPM7192S, EPM7256E, and EPM7256S devices.

MAX 9000 An Altera device family based on enhanced, third generation of Multiple Array MatriX architecture. These EEPROM-based

devices include EPM9320, EPM9400, EPM9480, and EPM9560 devices.

MAX+PLUS II Altera's Multiple Array MatriX Programmable Logic User System. MAX+PLUS II is a set of computer programs and hardware products that support design and implementation of custom logic circuits with FLEX 10K, FLEX 8000, MAX 9000, MAX 7000, FLASHlogic, MAX 5000, and Classic devices.

MPLD Mask-Programmed Logic Device, i.e., a custom Altera device created by converting a design originally created for an Altera device. Altera can convert customer designs into MPLDs, which are cost-effective alternatives for high-volume production.

O

OrCAD Library File (.lib) A binary file that specifies how OrCAD symbols should be displayed in an OrCAD Schematic File.

OrCAD Schematic File (.sch) A binary file, created with the OrCAD Draft schematic editor, that contains a logic schematic. You can open and edit an OrCAD Schematic File in the Graphic Editor, and save the edited file as either a GDF or an OrCAD Schematic File. You can also compile a project containing OrCAD Schematic Files directly with the MAX+PLUS II Compiler.

P

parallel expander An expander product term that is borrowed from an adjacent logic cell in the same MAX 9000 or MAX 7000 Logic Array Block (LAB). Parallel Expanders is also a logic option that can be applied to a logic function to allow it to borrow such parallel expanders. This option can reduce the number of expander product terms required in a project and increase the speed of the project. However, the project may use additional logic cells, and may be more difficult to fit.

Partitioner The Compiler module that partitions the logic in a project among multiple devices from the same device family. Partitioning occurs if you have created two or more chips in the project's design files or if the project cannot fit into a single device.

Passive Parallel Asynchronous (PPA) A configuration scheme in which a CPU loads the FLEX 8000 device via a common data bus. This configuration scheme is used for a system in which multiple devices require initialization. In this scheme, the FLEX 8000 device accepts a parallel byte of input data, and then serializes that byte using an internal synchronization Clock. Intelligent handshaking between the CPU and the FLEX 8000 device allows the CPU to configure multiple FLEX 8000 devices simultaneously. MAX+PLUS II can generate Tabular Text Files (**.ttf**) that contain the data for configuring FLEX 8000 devices in a PPA configuration scheme.

PCI *See* peripheral component interconnect (PCI).

PDIP Plastic dual in-line package. A device package offered by Altera. See *Altera Device Package Outlines* and *Ordering Information* in this data book for more information.

PENGN A utility used in conjunction with PLDshell Plus. PENGN is used to download logic designs to FLASHlogic devices via the FLASHlogic Download Cable.

peripheral component interconnect (PCI) An industry-established, high-speed bus standard for 32- and 64-bit applications.

peripheral register A register that exists on the periphery of a FLEX 8000 device. Peripheral Register is also a logic option that specifies that

a register should be implemented in a peripheral register.

PGA Ceramic pin-grid array. A device package offered by Altera. See *Altera Device Package Outlines* and *Ordering Information* in this data book for more information.

PIA *See* Programmable Interconnect Array.

PLAD3-12 An adapter that plugs into the Master Programming Unit (MPU). It allows the designer to use adapters with the prefix "PLE" with the PLE3-12A programming unit.

PLCC Plastic J-lead chip carrier. A device package offered by Altera. See *Altera Device Package Outlines* and *Ordering Information* in this data book for more information.

PLDshell Plus Altera software used to design and implement custom logic circuits for all FLASHlogic and Classic devices.

Programmable Interconnect Array (PIA) The portion of a MAX 7000, FLASHlogic, or MAX 5000 device that connects signals between different Logic Array Blocks (LABs).

Programmer Object File (.pof) A binary file generated by the Compiler's Assembler module. It contains the data used by the MAX+PLUS II Programmer to program an Altera device.

PQFP Plastic quad flat pack. A device package offered by Altera. See *Altera Device Package Outlines* and *Ordering Information* in this data book for more information.

product term Two or more factors in a Boolean expression combined with an AND operator constitute a product term, where "product" means "logic product."

programming file A file containing data for programming Altera devices. Both the MAX+PLUS II Compiler and Programmer can generate programming files. The following programming file formats are available in MAX+PLUS II:

- Hexadecimal (Intel-Format) File (**.hex**)
- JEDEC File (**.jed**)
- Programmer Object File (**.pof**)
- Serial Bitstream File (**.sbf**)
- SRAM Object File (**.sof**)
- Tabular Text File (**.ttf**)

POFs, SOFs, and JEDEC Files are used to program devices with the MAX+PLUS II Programmer. SBFs are used to configure FLEX 8000 devices from a system prompt with the BitBlaster. Hex Files and TTFs are used to configure FLEX 8000 devices by other means. JEDEC Files generated by A+PLUS software can also be used to program Classic devices. The Programmer can save data read from an examined device in POF or JEDEC File format.

project A project consists of all files that are associated with a particular design, including all subdesign files and related ancillary files created by the user or by the MAX+PLUS II software. The project name is the same as the name of the top-level design file in the project. MAX+PLUS II performs compilation, simulation, timing analysis, and programming on only one project at a time.

Q

QFP Quad flat pack. A device package offered by Altera. See *Altera Device Package Outlines* and *Ordering Information* in this data book for more information. Available in ceramic (CQFP), plastic (PQFP), power (RQFP), and thin (TQFP) versions.

R

register *See* flipflop.

removal tool *See* extraction tool.

Report File (.rpt) An ASCII test file generated by the Compiler's Fitter module that shows how device resources are used by the project.

RQFP Power quad flat pack. A device package offered by Altera. See *Altera Device Package Outlines* and *Ordering Information* in this data book for more information.

S

Security Bit A bit that prevents an Altera device from being interrogated or inadvertently reprogrammed. It can be turned on or off for each device in a project, or for the entire project.

shared expanders and **shareable expanders** A feature of MAX 9000, MAX 7000, and MAX 5000 device architecture that allows logic cells to use uncommitted product terms within the same Logic Array Block (LAB). A product term that can be shared in this manner is called a shareable expander; a product term that is shared in this manner is called a shared expander. The MAX+PLUS II Compiler automatically allocates shareable expanders when a project is compiled. A shared expander can also be allocated with an EXP primitive.

Simulator Netlist File (.snf) A binary file generated by the MAX+PLUS II Compiler that is used for functional simulation and/or timing simulation and timing analysis.

SOIC Plastic small-outline integrated circuit. A device package offered by Altera. See *Altera Device Package Outlines* and *Ordering Information* in this data book for more information.

SRAM Static random access memory. A read-write memory that stores data in integrated flipflops. See *Configuration Elements & Reliability* in this data book for more information.

SRAM Object File (.sof) A binary file generated by MAX+PLUS II that contains the data for configuring an Altera FLEX 8000 device via the FLEX Download Cable.

Symbol File (.sym) A binary file containing a primitive symbol or a symbol that represents a design file with the same filename.

T

Tabular Text File (.ttf) An ASCII text file in tabular format that supports the passive parallel synchronous (PPS) and passive parallel asynchronous (PPA) configuration schemes for configuring FLEX 8000 devices.

Text Design File (.tdf) An ASCII text file created with the MAX+PLUS II Text Editor or another standard text editor. The TDF contains design logic that is defined with the Altera Hardware Description Language (AHDL).

Text Design Export File (.tdx) An ASCII text file generated by the MAX+PLUS II Compiler that contains the AHDL equivalent of a Xilinx Netlist Format File (**.xnf**).

timing simulation A MAX+PLUS II Simulator mode that uses a timing Simulator Netlist File (**.snf**) to simulate the logical and timing performance of a project. Since the timing SNF is generated after logic synthesis, partitioning, and fitting are performed, only the nodes that have not been removed by logic optimization are available for simulation.

Timing SNF Extractor The Compiler module that creates the timing Simulator Netlist File (**.snf**), which contains the functional and timing data for the fully optimized project. This file is used for timing simulation and timing analysis. The Compiler's EDIF Netlist Writer module also uses timing SNFs to generate EDIF Output Files (**.edo**).

TQFP Thin quad flat pack. A device package offered by Altera. See *Altera Device Package*

Outlines and *Ordering Information* in this data book for more information.

Turbo Bit A control bit for choosing speed and power characteristics of Altera MAX 9000, MAX 7000, and Classic devices. If the Turbo Bit is on, the speed increases; if it is off, the power consumed decreases. The Turbo Bit may be turned on or off in a design file or in the Compiler. In MAX 9000 and MAX 7000 devices, it applies to individual logic cells within a device. In Classic devices, the Turbo Bit applies to the entire device.

U

user I/O The total number of I/O pins and dedicated inputs on a device.

V

Verilog HDL A hardware description language from Cadence. You can create a Verilog HDL description with the MAX+PLUS II Text Editor or any standard text editor and compile it directly with MAX+PLUS II. You can also generate an EDIF 2 0 0 or 3 0 0 netlist file from a Verilog HDL design that has been processed with a Verilog synthesis tool, then import the file into MAX+PLUS II as an EDIF Input File (**.edf**). The MAX+PLUS II Compiler can also generate a Verilog Output File (**.vo**).

Verilog Netlist Writer The Compiler module that creates one or more Verilog Output Files.

Verilog Output File (.vo) A Verilog Hardware Description Language (HDL) standard netlist file that is generated by the Verilog Netlist Writer module of the Compiler. A Verilog Output File contains functional and timing information for simulation with a standard Verilog simulator.

VHDL Very High Speed Integrated Circuit (VHSIC) Hardware Description Language. You can create a VHDL Design File (**.vhd**) with the MAX+PLUS II Text Editor or any standard text editor and compile it directly with MAX+PLUS II. You can also generate an EDIF 2 0 0 or 3 0 0 netlist file from a VHDL design that has been processed with a VHDL synthesis tool, then import the file into MAX+PLUS II as an EDIF Input File (**.edf**). The MAX+PLUS II Compiler can also generate a VHDL Output File (**.vho**).

VHDL Design File (.vhd) An ASCII text file created with the MAX+PLUS II Text Editor or another standard text editor. The VHDL Design File contains design logic that is defined with VHDL.

VHDL Netlist Writer The Compiler module that creates one or more VHDL Output Files.

VHDL Output File (.vho) A VHDL standard netlist file that is generated by the VHDL Netlist Writer module of the Compiler. A VHDL Output File contains functional and timing information for simulation with a standard VHDL simulator.

W

Waveform Design File (.wdf) A binary file created with the Waveform Editor, which contains design logic that is defined by a combination of waveforms.

X

Xilinx Netlist Format (.xnf) A netlist format used by Xilinx development tools. MAX+PLUS II can compile a Xilinx Netlist Format (**.xnf**) file created by the Xilinx LCA2XNF software.

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Altera Corporation
2610 Orchard Parkway
San Jose, CA 95134-2020
Telephone: (408) 894-7000
Fax: (408) 944-0952

Altera European Headquarters
Solar House
Globe Park
Fieldhouse Lane
Marlow
Bucks SL7 1TB, England
Telephone: 0628 488800
Fax: 0628 890078

Altera Japan Ltd.
Dai Tokyo Kasai Shinjuku Bldg.
3-25-3 Yoyogi, Shibuya-ku
Tokyo 151, Japan
Telephone: 03 3375-2281
Fax: 03 3375-2287